A circuit scheme to control current surge for RFID-NVM pumps

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Abstract: This paper presents a new circuit scheme to control the current surge in the boosting phase of an radio frequency idenfication–nonvolative memory pump. By introducing a circuit block consisting of a current reference and a current mirror, the new circuit scheme can keep the period-average current of the pump constantly below the desired level, for example, 2.5 μA. Therefore, it can prevent the rectified supply of the RFID tag IC from collapsing in the boosting phase of the pump. The presented scheme could effectively reduce the voltage drop on the rectified supply from more than 50% to even zero, but could cost less area. Moreover, an analytical expression to calculate the boosting time of a pump in the new scheme is developed.

Key words: charge pump; current surge; NVM; pump; RFID
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1. Introduction

Radio frequency identification (RFID) has become very popular in most fields of our society, such as supply chains and bus cards. Many different kinds of RFID tags have been developed. Due to low cost requirements, most tags are passive ones without an embedded battery. Usually, a passive tag is remotely powered by the electromagnetic field of a reader, and the power received is very small, especially for UHF RFID tags[1].

Nonvolatile memories (NVM) store information in RFID tag ICs. NVM writing operations need a high voltage VPP larger than the rectified supply VDD of the tag ICs. VPP might be generated by an on-chip pump, or a so-called charge pump. Almost every pump in modern NVM circuits derives from one Dickson charge pump[2]. However, such a pump draws over ten times the current in the boosting phase than in its steady state[3, 4]. Because of the limited power, such a current surge on the period-average current of the pump can easily collapse the rectified supply and then cause the chip to malfunction. Therefore, the writing distance of the tag should be largely reduced. This phenomenon is a big problem in today's low-power tag design.

To address the problem mentioned above, a pump using a slowly varying clock instead of a square wave and a pump with a current surge control scheme have been reported[3, 4]. Additionally, a method controlling the clock frequency of the pump can also be adopted to solve this problem[5]. But the slowly varying clock is unable to guarantee complete charging of the capacitors and will cause efficiency loss in the steady state of a pump. Actually, the schemes which control the amplitude or frequency of the driving clock and then make the pump boost step by step can maintain the efficiency in steady state and lower the period-average current in the boosting phase. But it is difficult to decide how long each step should be in the boosting phase in such schemes. An improper estimate of the step length will result in a longer boosting time or a ripple that still greatly affects the rectified supply. Moreover, control of the clock amplitude needs several large resistors, which waste the area of the tag IC.

In this study we propose a new circuit scheme to solve the mentioned issues. Instead of discretely controlling the clock amplitude or frequency, a circuit consisting of a current reference and a current mirror is introduced to control the current surge of RFID-NVM pumps in the boosting phase. This scheme can set a desired current value that the period-average current will never exceed.

2. System architecture

The system architecture of a conventional RFID tag is illustrated in Fig. 1. The antenna, rectifier, DC limiter and capacitor $C_{\rm bypass}$ generate the rectified supply VDD from the received RF power. VDD drives the NVM array, the high voltage generation block, and other blocks such as analog circuits and the digital controller in the RFID tag IC. The high voltage generation block, including a clock driver and a pump, is used to generate the high voltage VPP for NVM writing operations. As shown in Fig. 1, in a conventional high voltage generation block the power supplies of the clock driver and the pump are connected directly to the rectified supply VDD.

In order to charge capacitors the pump draws a great larger current in the boosting phase than in the steady state. Thus a current surge would occur and last for a relatively long time, resulting in the collapse of the rectified supply VDD. A large

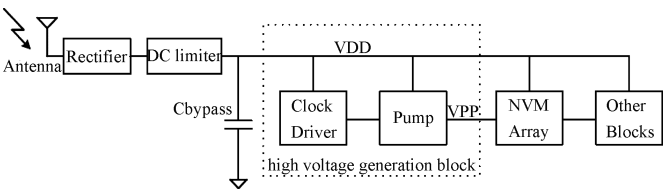

Fig. 1. System architecture schematic of an RFID tag with a conventioanl high voltage generation block.

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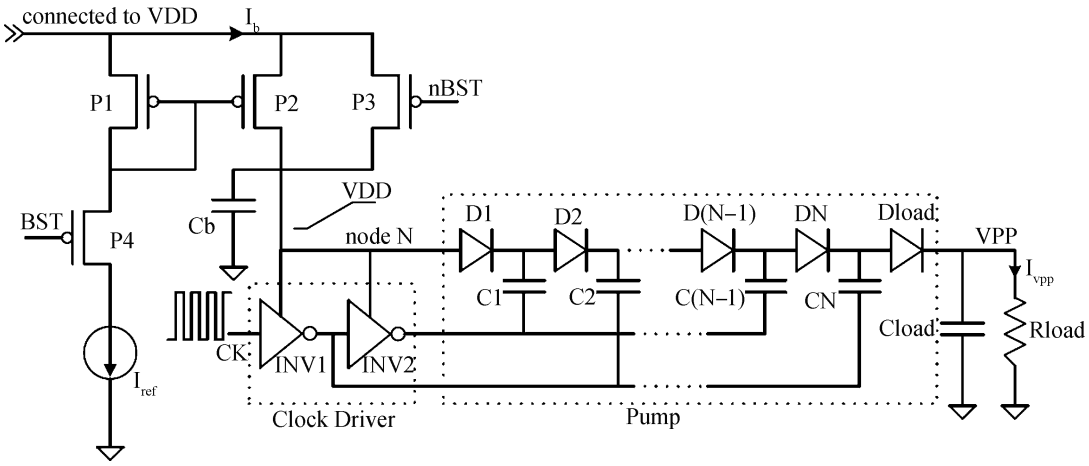

Fig. 2. Schematic of the propsed new circuit scheme.

VDD drop would cause the tag IC to reset itself or malfunction.

3. Proposed scheme to control current surge

Figure 2 shows the proposed circuit scheme to suppress the current surge of RFID-NVM pumps in the boosting phase. The inverters, INV1 and INV2, form the Dclock driver shown in Fig. 1. Diodes, D_i ($i = 1, 2, \ldots, N$) and D_{load}, and capacitors, C_i ($i = 1, 2, \ldots, N$) and C_{load}, make up a Dickson pump, helping to demonstrate the proposed scheme. If necessary, the Dickson pump can be replaced by any other pump. The resistor R_{load} represents the NVM array and auxiliary circuits of the pump. The PMOS transistors P1 and P2 form a current mirror. This current mirror and the current reference I_{ref} are used together to limit the total current I_b, drawn by the clock driver and the pump. PMOS transistors P3 and P4 are used as switches. If the control signal BST is "0", this scheme works in current surge control mode. If BST is "1", the transistor P4 will be cut off and P3 will be turned on. Then the current reference and the current mirror do not work, and the node N will be connected directly to V_{DD} by transistor P3. This means that the proposed scheme works as a conventional high voltage generation block as shown in Fig. 1. BST and nBST are a pair of opposite signals to control the proposed scheme, which can be generated by the control logic of EEPROM. When the proposed scheme works in the current surge control mode, transistor P3 is cut off and I_b is limited only by I_{ref} . In other words, the total transient current drawn by the clock driver and the pump is determined by I_{ref} , and the current surge in the boosting phase will not occur. C_b is a bypass capacitor, and it can be seen that the voltage on the capacitor rises slowly to V_{DD} in the boosting phase.

Generating I_{ref} is not a difficult task in an RFID tag IC because voltage or current reference is also required by analog circuits and has been built up. The existing reference can be shared with the proposed scheme to generate I_{ref} . To control the current surge a circuit to discretely control the amplitude of the driving clock has been proposed[4]. In that scheme three large resistors, 100 kΩ, are used to limit the current drawn from V_{DD} by the clock driver and the pump. But large resistors occupy a large area in the tag IC. However, in our proposed scheme no resistor is needed, so lots of area can be saved. Generally, an N-well resistor has the largest sheet resistance compared to other types. The sheet resistance of an N-well resistor is about 1000 Ω/□ in the SMIC 0.18 μm EEPROM process, and the minimum width for an N-well resistor is 2.1 μm. It is known that resistors occupy a major amount of area if they exist in circuits, so at least 1200 μm^2 of chip area can be saved in our proposed scheme. If the minimum N-well resistor width for is not used, or another type of resistor is used, more chip area will be needed in the scheme in Ref. [4].

3.1. Period-average current of pumps

In order to quantify the current surge caused by the pump in the boosting phase, we define a concept of a period-average current I_{avg}, based on I_b in Fig. 2 by Eq. (1). I_{avg} means the average current drawn by the clock driver and the pump during one period of the driving clock CK. T_{CK} stands for the driving clock period, and n stands for the clock period number.

$$I_{avg}(nT_{CK}) = \frac{1}{T_{CK}} \int_{(n-1)T_{CK}}^{nT_{CK}} I_b \mathrm{d}t. \quad (1)$$

For a conventional high voltage generation block, I_{avg} has a large peak value that lasts for a long time, for example, above 40 μA for more than 3 μs. But a pump might need only 3 μA after it has reached its steady state. The rectified supply VDD can not provide such a large I_{avg} in the boosting phase, even with a large bypass capacitor C_{bypass}, for example 100 pF. This is the reason why the current surge occurs in the boosting phase of the pump.

However, in the proposed circuit scheme I_{avg} is limited not to exceed the current capability of the rectified supply by I_{ref}. Therefore, the current surge can be avoided, and the rectified supply will constantly maintain a stable level, but not collapse. In the method with discretely control of the amplitude of the driving clock, there might still be some unwanted ripple in the rectified supply.

3.2. Boosting time estimation

We have developed a theoretical method to calculate the boosting time of the pump in Fig. 2. In the Dickson charge pump in Fig. 2 the forward bias voltage of the diodes D_i ($i = 1, 2, \ldots, N$) and D_{load} is V_T, and the value of the capacitors C_i ($i = 1, 2, \ldots, N$) equals C_{pump}. It is assumed that at the beginning

of the boosting phase, the charge on each capacitor C_i and C_{load} is zero, and that Q_i ($i = 1, 2, \ldots, N$) represents the charge on each capacitor C_i at the end of the boosting phase. Q_{load} means the total charge that has been stored on C_{load} and consumed by R_{load} in the boosting phase. Since the charge consumed by the clock driver driving each capacitor C_i equals the total charge transferred from this capacitor to the next capacitor[6], the total charge Q_{tot}, drawn by the clock driver and the pump from the rectified supply in the boosting phase, can be calculated by Eq. (2).

$$Q_{tot} = Q_1 + 2Q_2 + \cdots + NQ_N + (N+1)Q_{load}. \quad (2)$$

If parasitic capacitors can be ignored, VPP can be obtained as

$$V_{PP} = (N+1)(VDD - V_T) - \frac{NI_{vpp}}{C_{pump} f_{CK}}. \quad (3)$$

In Eq. (3) f_{CK} stands for the frequency of the driving clock and I_{vpp} is the current flowing though R_{load}. I_{vpp} can be expressed as

$$I_{vpp} = \frac{V_{PP}}{R_{load}}. \quad (4)$$

The charge Q_i on the capacitor C_i can be approximated by

$$Q_i = i(VDD - V_T)C_{pump} - \frac{(i-1)I_{vpp}}{f_{CK}}. \quad (5)$$

In the proposed scheme the output VPP of the pump nearly increases linearly in the boosting phase, thus Q_{load} can be expressed as Eq. (6) if we assume that the boosting time is equal to t_{boost}.

$$Q_{load} = V_{PP}C_{load} + \frac{1}{2}I_{vpp}t_{boost}. \quad (6)$$

In the boosting phase the total current consumed by the clock driver and the pump can always be limited to I_{ref} in the proposed scheme, so the boosting time can be estimated by

$$t_{boost} = \frac{Q_{tot}}{I_{ref}}. \quad (7)$$

Taking Eqs.(2)–(6) into Eq. (7), the boosting time can be figured out as

$$t_{boost} = \frac{V_{eq}C_{eq}}{I_{ref} - \dfrac{V_{eq}}{2R_{load}}}. \quad (8)$$

In Eq. (8),

$$V_{eq} = (N+1)^2(V_{DD} - V_T) \quad (9)$$

and

$$C_{eq} = \frac{N(2N+1)}{6(N+1)}C_{pump} + \frac{N(N+2)}{6(N+1)}\frac{1}{f_{CK}R_{load}} + C_{load}. \quad (10)$$

where V_{eq} is an equivalence voltage determined by the stage number N of the pump and the forward bias voltage V_T of the diodes. Three items, C_{pump}, R_{load} and C_{load}, contribute to the equivalence capacitor C_{eq}. Due to the parasitic capacitors and leakage current in the pump, the boosting time calculated from Eq. (8) deviates a little from the real value. But it also can be seen that t_{boost} is approximately inversely proportional to I_{ref}. Thus a good understanding of t_{boost} can be obtained by Eq. (8).

Table 1. Design parameters.

Parameter	Value
V_{DD}	2 V
C_{bypass}	100 pF
I_{ref}	2.5 μA
C_{pump}	3 pF
C_{load}	8 pF
R_{load}	100 MΩ
f_{CK}	2 MHz
N	8

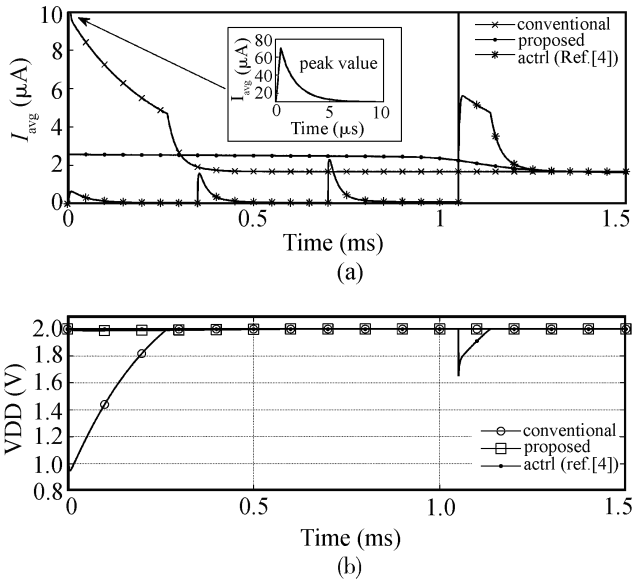

Fig. 3. Comparisons of (a) the period-average current and (b) the rectified supply, VDD.

4. Verification and simulation

In order to verify the proposed circuit scheme, a set of simulations have been run with SPECTRE, using SMIC 0.18 μm EEPROM process design kits (PDK). All of our simulations are based on this PDK. Some of the design parameters we chose are shown in Table 1. Three circuit schemes were built up and compared with each other. One is the conventional high voltage generation circuit shown in Fig. 1, the second is the amplitude control method[4], and the third is the proposed scheme shown in Fig. 2. Auxiliary circuits such as the rectifier, reference and NVM array are described by their behavior models. The pump and the proposed scheme are on the transistor level.

Figure 3(a) shows the period-average current of the three schemes defined by Eq. (1). The conventional scheme has a large peak value, even up to 70 μA, and the large I_{avg} lasts more than 10 μs. Within 0.3 ms it also draws a much larger current than the other two. Thus, as shown in Fig. 3(b), in the conventional scheme the rectified supply has a voltage drop that is more than 50% of VDD, and this is enough to cause VDD to collapse. In the amplitude control method, "actrl" in Fig. 3(a), there still is an unwanted large ripple at the last step in both I_{avg} and VDD. However, in the proposed scheme there is no obvious ripple in either I_{avg} or VDD in the whole boosting phase. Also, after the pump has reached its steady state, the

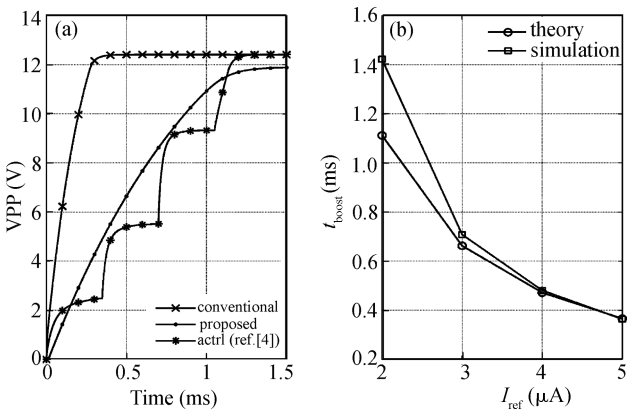

Fig. 4. (a) Output of the pump, VPP. (b) Boosting time in the proposed scheme.

current reference will be cut off to set the proposed scheme into a conventional scheme. Then, no extra current will be drawn, so the total current drawn by the clock driver and the pump can be kept below 2.5 μA at any time.

Figure 4(a) shows the boosting time of the pump in the three schemes and the waveform of VPP. The conventional scheme has a shorter boosting time, but this is not critical in RFID NVM applications because there is lots of time for NVM writing operations due to the RFID system protocols. Also, we have simulated the boosting time versus the value of $I_{\rm ref}$, and then compared it with the theoretical one calculated by Eq. (8) in Fig. 4(b). It can be seen that Equation (8) can estimate the boosting time of the proposed scheme well, and the error is less than 10%. This error might be due to the secondary effects of transistors and leakage current.

5. Conclusion

A new circuit scheme has been proposed to control the current surge occurring in a conventional scheme. The simulation results indicate that the proposed scheme is able to effectively limit the period-average current drawn by the clock driver and the pump in the boosting phase to the desired level, for example 2.5 μA in our simulation, which can be any level if necessary. With less area loss, the voltage drop on the rectified supply VDD in RFID tag ICs can be reduced from more than 50% to about zero, which can effectively prevent the RFID tag IC from resetting itself or malfunctioning. Moreover, we have developed analytical expressions to calculate the boosting time of the proposed scheme, which has an error of less than 10% compared with the simulation result.

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