A novel SOI MOSFET electrostatic field sensor

Chen Xin'an(陈新安)† and Huang Qing'an(黄庆安)

(Key Laboratory of MEMS of Ministry of Education, Southeast University, Nanjing 210096, China)

Abstract: A novel low temperature solid state electric field sensor is demonstrated as a promising sensor. The sensor is a type of constant voltage Wheatstone bridge whose resistors are four direct gate SOI MOSFET devices. It is demonstrated in theory that the output voltage signal is proportional to the electric field E, the temperature drift is about zero when the temperature is in the range from 200 to 400 K, and the doping concentration is in the range from 1×10^{14} to 1×10^{16} cm^{-3}. The experiment results indicate that the resolution of the sensor is about 3.27 mV for a 1000 V/m electric field at 300 K, and the voltage drift by an amount is about 47 V/m field signal when the degree temperature is in the range from 300 to 370 K, which is much smaller than the current drift of a single MOSFET which is about 10000 V/m field signal.

Key words: electrostatic field sensor; low temperature drift; Wheatstone bridge
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1. Introduction

Electrostatic field sensors are widely used in aviation, spaceflight, national defense, weather, electric power and other fields. They have been the subject of research over the past sixty years. Numerous types of electrostatic field sensors have been developed, including mechanical sensors[1−4] and MEMS sensors[5−7]. MEMS electrostatic field sensors have developed rapidly in the past ten years. However, these electrostatic field sensors all have moving parts, such as moving shuttling. So, these electrostatic field sensors are relatively expensive, sensitive to mechanical damage and not easy to integrate with IC. The MOSFET has found many applications in the measurement of electrostatic fields[8−10]. MOSFET electrostatic field sensors have no moving parts and generally require less operating power, so the solid state electrostatic field sensors should become one of the most important sensors. However, little advancement has been made in the past twenty years because the sensors are significantly affected by the ambient temperature. The current signal was observed to drift up to a 10000 V/m field signal per degree Celsius of ambient temperature change[10]. So the solid state electrostatic field sensors can only be used to measure large electric field, such as 1000 kV/m electric field. If the solid state electrostatic field sensors are used to measure low electric field in ambient temperature, the temperature drift must be eliminated or reduced.

In this paper, a novel solid state electrostatic field sensor is presented, which has low temperature drift. The sensor is a type of constant voltage Wheatstone bridge whose resistors are four direct gate SOI MOSFET devices. For a single SOI MOSFET device, the main reason for temperature drift is that the carrier mobility changes as the temperature changes. But for two direct gate SOI MOSFET devices in series, the output voltage signal does not change with temperature because the carrier mobility changes at the same time. It is demonstrated in theory that the output voltage signal is proportional to the electric field E and the temperature drift is about zero. The experiment results indicate that the resolution is about 3.05 mV for 1000 V/m electric field at 300 K and the voltage signal drift is about 47 V/m.

2. Theory

2.1. Direct gate SOI MOSFET device

The structure of the direct gate MOSFET device used for the measurement of the electric field is shown in Fig. 1. The SOI MOSFET device was fabricated on an SOI substrate, whose four sides of the channel are insulated by oxide layers. The gate oxide layer is absent from the metalized gate electrode. So the gate oxide layer and channel beneath were exposed directly to the external field. The electric field was subject to appropriate boundary conditions at the air-oxide interface, and penetrated to the silicon surface beneath, where partial silicon was depleted to form the depletion layer. Thus, the silicon layer between the depletion layer and the oxide layer of SOI substrate is the channel of the partial depletion MOSFET. The thickness of the depletion layer changes with the electric field, so the channel thickness and the channel resistance change with the electric field. In the paper, P-type silicon is selected for the oxide positive charge, which induces a

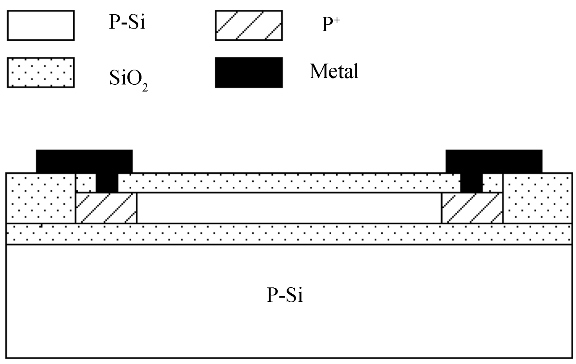

Fig. 1. Schematic representation of an SOI direct gate MOSFET device.

† Corresponding author. Email: chenxinan02@lzu.cn

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depletion layer or space charge region near the P-type silicon surface and an accumulation layer at the N-type silicon surface. We assume channel length to be L, channel width to be W, channel thickness to be d and the carrier concentration to be n_p.

The electric field E vertical to the semiconductor silicon surface induces a space charge region near the surface. According to the Gauss Law, the amount of charge per unit area of the induced space charge region Q_s is proportional to the electric field E applied to the channel surface:

$$Q_s = \varepsilon_s \varepsilon_0 E, \tag{1}$$

where ε_s is the permittivity of the semiconductor and ε_0 is the permittivity of the free space.

The channel is doped uniformly, in which doping density is N_a. When the temperature is in the range from 200 to 400 K and the doping density N_a is in the range from 1×10^{14} to 1×10^{16} cm^{-3}, the doping impurities can all be activated and n_i is negligibly small compared to the doping density N_a. So, the carrier concentration n_p is equal to the doping density N_a at ambient temperature. If the abrupt depletion approximation is valid, the depletion layer thickness x_d can be extracted:

$$x_d = \frac{Q_s}{qN_a} = \frac{\varepsilon_s \varepsilon_0 E}{qN_a} = \frac{\varepsilon_s \varepsilon_0 E}{qn_p}, \tag{2}$$

where q is the electronic charge. The effective channel thickness x is the original channel thickness d minus the depletion layer thickness x_d:

$$x = d - x_d = d - \frac{\varepsilon_s \varepsilon_0 E}{qN_a}. \tag{3}$$

So, the resistance R of the SOI MOSFET device is expressed by:

$$R = \rho \frac{L}{xW} = \frac{L}{qn_p\mu_p(d - x_d)W} = \frac{L}{qdn_p\mu_p W - \varepsilon_s \varepsilon_0 E \mu_p W}, \tag{4}$$

where L is the channel length, W is the channel width, and μ_p is the carrier mobility. It can be seen that the effective channel thickness reduces and the channel resistance increases with the increase of the electric field E. But the channel resistance is sensitive to temperature because the carrier mobility μ_p changes with temperature. Moreover, the change of the carrier mobility μ_p with temperature is one of the semiconductor characteristics. So, for a single SOI MOSFET device, the temperature drift cannot be eliminated or reduced.

2.2. Low temperature drift electrostatic field sensor

The low temperature drift electrostatic field sensor is a type of constant voltage Wheatstone bridge as shown in Fig. 2, whose resistors are four of the same SOI MOSFET devices as shown in Fig. 1. The SOI MOSFET devices 1 and 3 are used to measure the external electric field, whose resistance R_1 changes with the electric field.

$$R_1 = \frac{L}{qdn_p\mu_p W - \varepsilon_s \varepsilon_0 E \mu_p W}. \tag{5}$$

In order to screen the external electric field, the SOI MOSFET devices 2 and 4 are mounted in a metal header package, so the electric field applied to the channel surface is equal to zero. Substituting the electric field $E = 0$ into Eq. (4), the resistance R_2 is achieved:

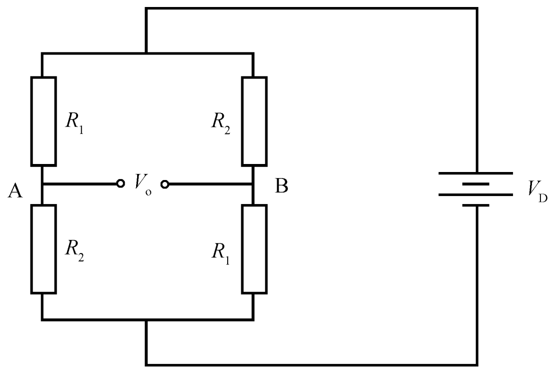

Fig. 2. Wheatstone bridge with four SOI MOSFET resistors.

$$R_2 = \frac{L}{qdn_p\mu_p W}. \tag{6}$$

The output voltage of the electrostatic field sensor V_o is the potential difference between point B and point A:

$$V_o = V_B - V_A = \frac{R_1}{R_2 + R_1}V_D - \frac{R_2}{R_2 + R_1}V_D$$

$$= \frac{\varepsilon_s \varepsilon_0 E \mu_p \frac{W}{L}}{2qdn_p\mu_p\frac{W}{L} - \varepsilon_s \varepsilon_0 E \mu_p \frac{W}{L}} V_D. \tag{7}$$

If the electric field is not larger than 20000 V/m, the depletion layer thickness is largely less than the channel thickness d, so

$$qdn_p\mu_p\frac{W}{L} \gg \varepsilon_s \varepsilon_0 E \mu_p \frac{W}{L}. \tag{8}$$

The output voltage V_o of the electrostatic field sensors can be rewritten as:

$$V_o \approx \frac{\varepsilon_s \varepsilon_0 E \mu_p \frac{W}{L}}{2qdn_p\mu_p\frac{W}{L}} V_D = \frac{\varepsilon_s \varepsilon_0 E}{2qdn_p} V_D. \tag{9}$$

In Eq. (9), there are three parameters, namely, the major carrier holes concentration n_p, the measured electric field E and the constant voltage V_D of the Wheatstone bridge. If the major hole concentration n_p and the constant voltage V_D are given, the output voltage V_o is proportional to the measured electric field E.

2.3. Temperature drift

Compared with Eq. (4), the effect of the temperature on the output signal for the major carrier hole mobility μ_p is counteracted, so the major carrier hole concentration n_p is the only parameter relative to the temperature. However, when the temperature is in the range from 200 to 400 K and the doping density N_a is in the range from 1×10^{14} to 1×10^{16} cm^{-3}, the doping impurity can all be activated, and n_i is negligibly small

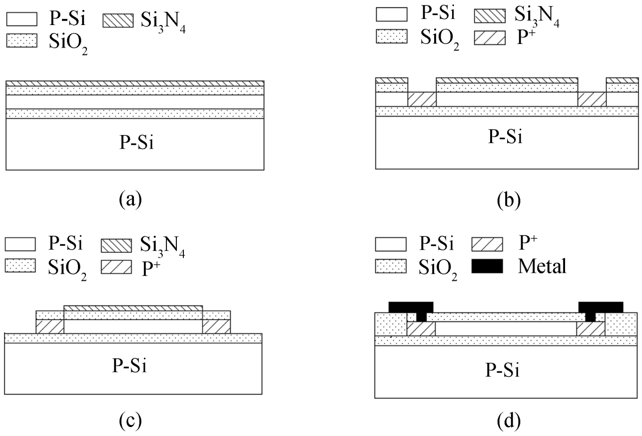

Fig. 3. Main process flows of the SOI MOSFET device.

compared to the doping density N_a. So, the carrier concentration n_p is equal to the doping density N_a.

$$\frac{dn_p}{dT} = 0. \tag{10}$$

So, the temperature drift of the sensor is:

$$\frac{dV_o}{dT} = \frac{d}{dT}\left(\frac{\varepsilon_s\varepsilon_0 E}{2qdn_p}V_D\right) = -\frac{\varepsilon_s\varepsilon_0 E}{2qdn_p^2}V_D \times \frac{dn_p}{dT} = 0. \tag{11}$$

In theory, the sensor has very low temperature drift, which is much smaller than the direct gate MOSFET sensor with ambient temperature drift by an amount up to a 10 kV/m field signal per degree Celsius of ambient temperature[10].

3. Main process flow

To prove the low temperature drift of the novel electrostatic field sensor, the SOI MOSFET devices are fabricated by using the P-type SIMOX SOI wafer doped 1×10^{15} cm^{-3}. The thickness of the P-type Si layer on the oxide is about 600 nm, and that of the oxide layer is about 100 nm. The main process flows of the SOI MOSFET device are as follows:

(a) The P-type SIMOX SOI wafer was cleaned and oxygenated in dry oxygen to form an approximately 100-nm gate oxide layer. Then a 200-nm nitride layer was deposited on the gate oxide layer, as shown in Fig. 3(a).

(b) The nitride and gate oxide were etched to form the windows of the source and drain region of the MOSFET. Then the boron is implanted to form the source and drain regions, the dose of which is about 5×10^{14} cm^{-2} for the heavy diffusion, as shown in Fig. 3(b).

(c) The silicon on both sides of the channel and the outsides of the source and drain regions was etched and oxygenated to form the oxide isolation region, as shown in Fig. 3(c).

(d) Then the nitride layer was removed and another layer oxide was deposited.

(e) Finally, a metal layer was deposited to form the contact lines, as shown in Fig. 3(d).

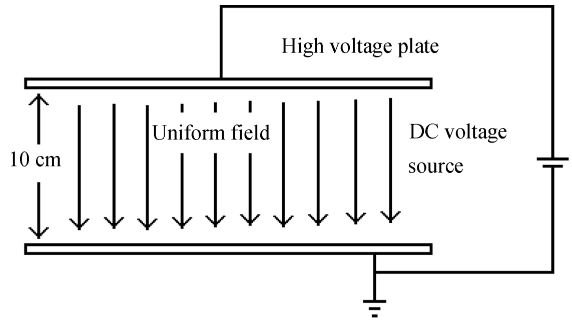

Fig. 4. Configuration of the uniform field.

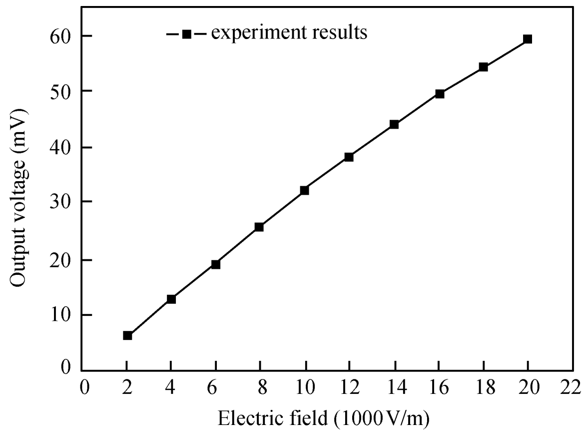

Fig. 5. Experiment results of output voltage versus the electric field.

4. Analysis of experiment results

4.1. Experiment results of output voltage versus the measured electric field

The electrostatic field sensors fabricated in terms of the above process flows were measured under a constant temperature condition. For the SOI MOSFET device used in the experiment, the main parameters are a channel width of 10 μm, a channel length of 5 μm, a channel thickness of 0.6 μm and a carrier concentration of about 1×10^{15} cm^{-3}. The voltage of the constant voltage Wheatstone bridge V_D is 5 V. The electric field is in the range from 2 to 20 kV/m, which is created by a DC voltage source and two conducting plates as shown in Fig. 4. The space and the DC voltage between two conducting plates respectively are about 10 cm and in the range from 200 to 2000 V.

The plot of output voltage versus applied electric field E is shown in Fig. 5. The experiment results indicate that the output voltage is proportional to the electric field E and changes with about 3.27 mV for 1 kV/m electric field at 300 K.

4.2. Experiment results of temperature drift

The temperature drift is measured when the electric field E is equal to 5 kV/m, as shown in Fig. 6. The temperature changes from 300 to 370 K, the output voltage increases with temperature at a ratio of 1.52 mV/10 K, namely, the voltage drift by amount is up to 47 V/m electric field signal per degree temperature. The temperature drift is much smaller than a single MOSFET whose temperature drift is about 10 kV/(m·K). In theory, the temperature drift should be zero. The measured

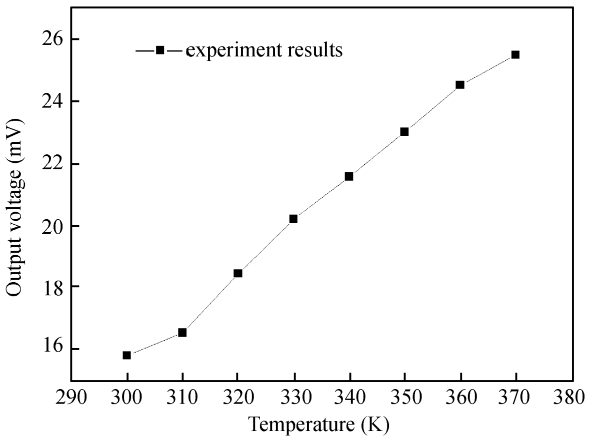

Fig. 6. Experiment results of output voltage versus temperature.

temperature drift may be relative to the moving of the oxide charges[10]. In the paper, to decrease the oxide charge, the nitride was deposited on the gate oxide before the boron implantation process.

5. Conclusion

In this paper, a novel low temperature solid state electric field sensor was demonstrated as a promising sensor. The sensor is a type of constant voltage Wheatstone bridge whose resistors are four direct gate SOI MOSFET devices. The experiment results indicate that the resolution is about 3.27 mV for 1 kV/m electric field at 300 K, and the temperature drift is about 1.52 mV when the temperature increases by 10 K, namely, the signal voltage drift with ambient temperature by an amount is about 47 V/m field signal per degree temperature from 300 to 370 K, which is much smaller than the current signal drift with ambient temperature by an amount up to about 10 kV/m field signal. The results of this research suggest that the novel solid state electric field sensor can be used at ambient temperature.

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