Tunable current mirror and its application in LNA*

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Abstract: A novel topology of current mirror (CM) with tunable output current is proposed. Two methods for output current tuning are presented. The first one utilizes an analog input voltage for linear current output, and the second one has an N-bit digital input signal for 2^N un-continuous current outputs. A linearization method for low noise amplifier (LNA) is proposed and realized with this tunable CM. As the provider of the bias current, the CM has brought the LNA a lower NF (noise figure) and a higher IIP3 (input-referred third-order intercept point) compared with a conventional one. The experimental results show that the LNA achieves 1.47 dB NF and +19.83 dBm IIP3 at 860 MHz.

Key words: current mirror; tunable; LNA; bias current; linearization

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1. Introduction

Recently, the realization of analog signal processing based on current-mode circuit has received considerable attention. Current mirrors (CMs) based on BJT or MOSFET devices are important building blocks for current-mode circuit design.

The tunable CMs are required widely in applications such as current-mode amplifying[1] and filtering[2]. Also, some related techniques have been reported in the past few years. For example, Somdunyakanok proposed an accurate tunable CM based on translinear type-A in 2008[3]. Another accurate wide swing CM using the npn-NMOS cascade instead of the NMOS–NMOS cascade was presented by Yang in 2008[4]. A programmable CM composed of DGMOSFET has been introduced by Hamed in 2007[1]. Guvenc has proposed a tunable linear CM composed with both BJT and MOSFET in 2008[5]. It can be seen that accurate current output has been accomplished but complexity was suffered.

In this paper, a novel tunable CM composed of 3 BJTs is proposed and implemented. It has the advantages of simplicity, wide tuning range and convenience in use. The accuracy of this CM is high enough for most applications, such as biasing, amplifying, and so on. The output of this CM can be controlled either by an analog voltage or an N-bit digital signal (N+2 BJTs needed). It is thought that the proposed structure would be applied in a wide variety of areas.

This tunable CM has been adopted as the provider of bias current in an LNA design for a lower NF (noise figure) and a higher IIP3 (input-referred third-order intercept point). Therefore, the LNA achieves a larger dynamic range with the method of tuning bias current according to the strength of the received signal.

Experiments were carried out for both CM and LNA. Simulation and measurement results are both very consistent with the theoretical analysis.

2. Conventional current mirror

A conventional classic schematic of CM is shown in Fig. 1.

In order to simplify the analysis of CM, the Early effect of BJT is ignored, which will bring little error into the analysis result. According to Kirchhoff's law and the theories of BJT, $I_{\rm OUT}$ can be calculated as:

$$I_{\rm OUT} = \frac{V_{\rm CC} - V_{\rm BE1}}{(R_1 + R_{\rm REF})\left(1 + \dfrac{1}{\beta}\right)\dfrac{R_2}{R_1} + \dfrac{R_{\rm REF}}{\beta}}, \tag{1}$$

where β is the ratio of collector current to base current.

In the engineering, by setting the value of $V_{\rm BE1}$ to 0.6 V and assuming β infinite, Equation (1) can be simplified into:

$$I_{\rm OUT} = \frac{R_1}{R_2}\frac{V_{\rm CC} - V_{\rm BE1}}{R_1 + R_{\rm REF}} = \frac{R_1}{R_2}\frac{V_{\rm CC} - 0.6}{R_1 + R_{\rm REF}}. \tag{2}$$

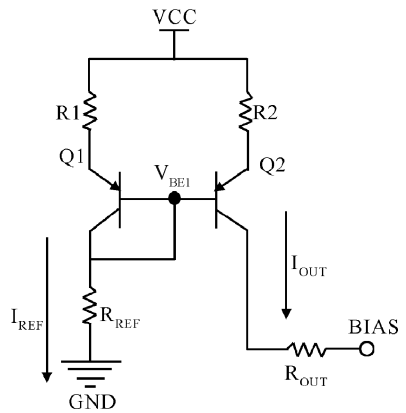

Fig. 1. Schematic of a conventional CM.

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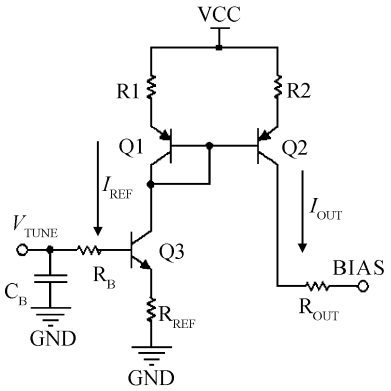


Fig. 2. Schematic of a tunable cm with output current controlled by an analog voltage.

3. Tunable current mirror

For an adjustable output current, we make R_{REF} (in Fig. 1) a variable resistor. It is obvious that I_{OUT} will change when R_{REF} is tuned.

To avoid overheating the transistors in the tunable CM, a resistor (R_{OUT}) is adopted to limit the maximum of I_{OUT}.

In the following sections, two methods for tuning the output current are introduced and realized, where one utilizes an analog voltage, and the other adopts an N-bit digital signal.

3.1. CM with output current controlled by an analog voltage

Figure 2 gives the schematic of a tunable CM with an analog input voltage (V_{TUNE}) for output current controlling. Q3 is a transistor acting as a variable resistor controlled by V_{TUNE}. When V_{TUNE} grows high, the resistor between the collector and emitter of Q3 will decrease, then I_{REF} and I_{OUT} will both increase.

It can be proved that I_{OUT} is almost a linear function of V_{TUNE} when Q3 works in the linear region. According to Kirchhoff's voltage law, Equation (3) is easy to get by analyzing the base circuit of Q3.

$$V_{\mathrm{TUNE}} - V_{\mathrm{BE3}} - I_{\mathrm{B3}}R_{\mathrm{B}} - I_{\mathrm{E3}}R_{\mathrm{REF}} = 0. \tag{3}$$

Based on the theory of BJT, when Q3 works within the linear region, I_{B3} can be derived as:

$$I_{\mathrm{B3}} = \frac{I_{\mathrm{REF}}}{\beta} = \frac{R_2 I_{\mathrm{OUT}}}{R_1 \beta}. \tag{4}$$

Then, I_{OUT} can be deduced from Eqs. (3) and (4) as:

$$I_{\mathrm{OUT}} = (V_{\mathrm{TUNE}} - V_{\mathrm{th}})\frac{R_1\beta}{R_2[R_{\mathrm{B}} + (\beta+1)R_{\mathrm{REF}}]}, \tag{5}$$

where V_{th} is the threshold voltage of a transistor.

According to Eq. (5), it can be concluded that I_{OUT} and V_{TUNE} have a linear relationship when Q3 is in linear region.

Furthermore, Q3 can be replaced by a PNP transistor for a negative ratio of I_{OUT} and V_{TUNE}.

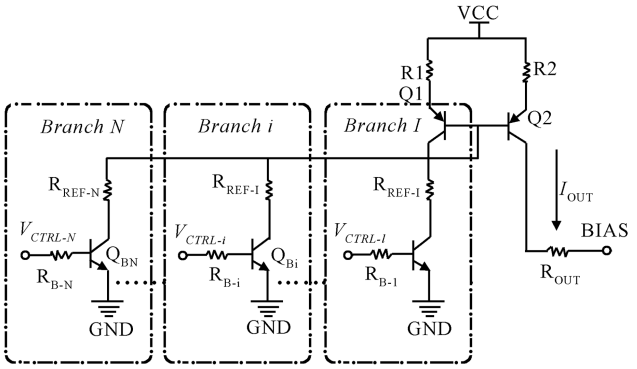


Fig. 3. Schematic of a tunable CM with output current controlled by N-bit digital signal.

3.2. CM with output current controlled by N-bit digital signal

Figure 3 shows the schematic of a tunable CM with an N-bit digital input signal. In Fig. 3, every controlling signal ($V_{\mathrm{CTRL}\text{-}i}$) is added to the base of BJT (QBi) in each branch. And a resistor $R_{\mathrm{REF}\text{-}i}$ which determines the weight of each branch is adopted in series with QBi.

It is seen that QB-i will operate in the saturation region when $V_{\mathrm{CTRL}\text{-}i}$ is high ($\mathrm{bit}_i = 1$), and in the cut off region when $V_{\mathrm{CTRL}\text{-}i}$ is low ($\mathrm{bit}_i = 0$). Assuming that the equivalent resistor between the collector and emitter of QB-i ($R_{\mathrm{CE}\text{-}i}$) is much smaller than $R_{\mathrm{REF}\text{-}i}$ when QB-i is in the saturation region, and that $R_{\mathrm{CE}\text{-}i}$ is much greater than $R_{\mathrm{REF}\text{-}i}$ when QB-i is in the cut off region. Then the equivalent resistor of each branch ($R_{\mathrm{SUB}\text{-}i}$) can be expressed as:

$$R_{\mathrm{SUB}\text{-}i} = \begin{cases} R_{\mathrm{REF}\text{-}i} & \mathrm{bit}_i = 1, \\ \infty, & \mathrm{bit}_i = 0. \end{cases} \tag{6}$$

Based on Eq. (2), I_{OUT} can be calculated as:

$$I_{\mathrm{OUT}} = \frac{R_1}{R_2}\frac{V_{\mathrm{CC}} - V_{\mathrm{BE1}}}{R_1 + R_{\mathrm{SUB}\text{-}1}//R_{\mathrm{SUB}\text{-}2}//\cdots//R_{\mathrm{SUB}\text{-}N}}. \tag{7}$$

If the value of R_1 is designed much smaller than $R_{\mathrm{REF}\text{-}1}//R_{\mathrm{REF}\text{-}2}//\cdots//R_{\mathrm{REF}\text{-}N}$, then Equation (7) can be simplified into:

$$I_{\mathrm{OUT}} = \frac{R_1}{R_2}(V_{\mathrm{CC}} - V_{\mathrm{BE1}})\left(\frac{\mathrm{bit}_1}{R_{\mathrm{REF}\text{-}1}} + \frac{\mathrm{bit}_2}{R_{\mathrm{REF}\text{-}2}} + \cdots + \frac{\mathrm{bit}_N}{R_{\mathrm{REF}\text{-}N}}\right). \tag{8}$$

And Equation (8) can also be expressed in vector format as:

$$I_{\mathrm{OUT}} = \frac{R_1}{R_2}(V_{\mathrm{CC}} - V_{\mathrm{BE1}})\,[\mathrm{bit}_1 \;\; \mathrm{bit}_2 \;\; \cdots \;\; \mathrm{bit}_N] \times \begin{bmatrix} \frac{1}{R_{\mathrm{REF}\text{-}1}} & \frac{1}{R_{\mathrm{REF}\text{-}2}} & \cdots & \frac{1}{R_{\mathrm{REF}\text{-}N}} \end{bmatrix}^T. \tag{9}$$

In addition, the values of $R_{\mathrm{REF}\text{-}i}$ can be designed and put into a particular array, correspondingly, the different values of I_{OUT} will be organized in a special series. For example, we can get I_{OUT} in arithmetic progression if $R_{\mathrm{REF}\text{-}i}$ satisfies $R_{\mathrm{REF}\text{-}(i-1)} = 2R_{\mathrm{REF}\text{-}i}$.

Furthermore, QB-i can be a PNP BJT or a MOSFET.

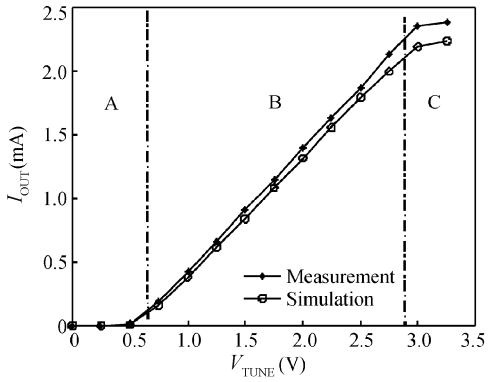


Fig. 4. Curves of I_{OUT} versus V_{TUNE} in the tunable CM.

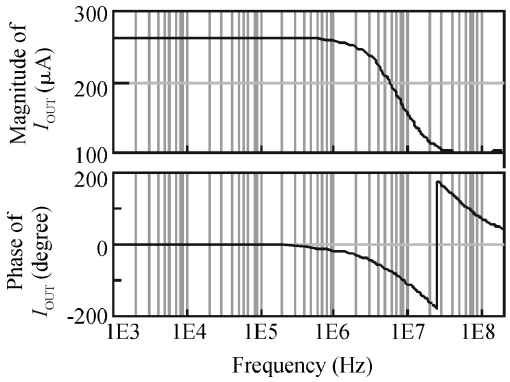
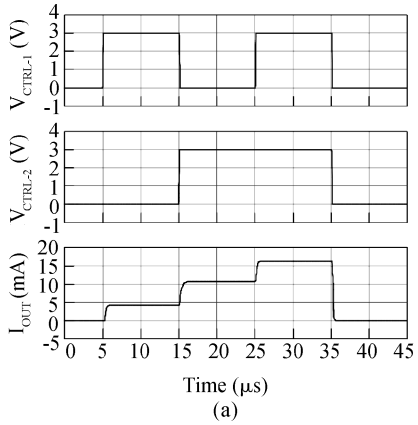


Fig. 5. AC performance of the tunable CM.



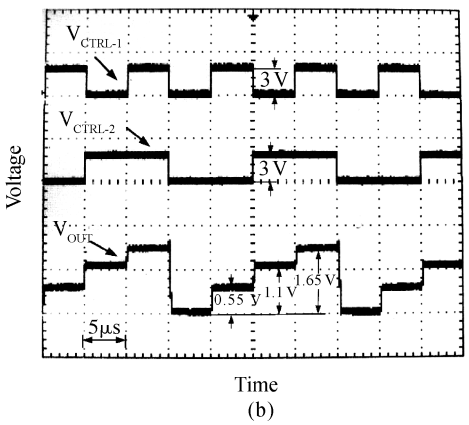


Fig. 6. Output current of the CM control by 2-bit digital signal: (a) Simulation result; (b) Measurement result: the photo of waveform on oscilloscope screen. V_{OUT}: Voltage over R_{OUT}, Representing I_{OUT}. (R_{OUT} = 100 Ω).

3.3. Simulation and experiment results of the tunable CM

3.3.1. Tunable CM controlled by an analog voltage

To verify the theoretical analysis results above, the schematic in part 3.1 (Fig. 2) was simulated first, and then experiments were carried out on a PCB board.

Firstly, the DC characteristic was simulated and tested. The results are given in Fig. 4.

We observed that the curve of I_{OUT} versus V_{TUNE} could be divided into 3 sections (sections A, B and C). In section A, Q3 is cut off, and R_{CE3} is so large that I_{OUT} is limited in a very low value. In section B, Q3 is operating within the linear region. I_{OUT} increases as a linear function of V_{TUNE} which verifies the conclusion in part 3.1. In section C, I_{OUT} is limited by the resistor in the OUTPUT branch.

Secondly, AC simulation was carried out. The simulation result is shown in Fig. 5. The frequency range of linear operation of this CM is up to 1 MHz which is sufficient for application in bias current. And the top boundary of the operation frequency can be reduced by increasing the resistance of R_B or R_{OUT}.

3.3.2. Tunable CM controlled by *N*-bit digital signal

Simulation and experiment were both performed for the tunable CM with a 2-bit digital control signal, where R_{REF-i} was designed as $R_{REF-1} = 2R_{REF-2}$. Figure 6(a) gives the simulation results, including the waveform of the control voltage (V_{CTRL-1}, V_{CTRL-2}) and output current (I_{OUT}). Figure 6(b) gives measurement results where V_{OUT} (the voltage of R_{OUT}) can represent I_{OUT} by dividing R_{OUT} (100 Ω).

4. Application of tunable CM in LNA

LNA, which is located in the front of a receiver, has a great influence on the receiver's performance. Nowadays, although more and more LNA is integrated in CMOS technology, the discrete low noise BJT is still in use for extremely low noise, high linearity and high frequency.

Given the IIP3 and NF, one can define another important property of LNA called the spurious-free dynamic range (SFDR). The SFDR is commonly used to determine the input power range in which the received signal can be detected in the presence of noise and amplified without nonlinear interference[6, 7]. The value of SFDR can be obtained from IIP3 and NF through:

$$\mathrm{SFDR(dB)} = \frac{2}{3}[\mathrm{IIP3(dBm)} - \mathrm{NF(dB)} - 10\lg B(\mathrm{Hz}) + 174], \tag{10}$$

where B is the channel bandwidth.

According to Eq. (10), a large SFDR can be achieved by low NF and high IIP3. But it is known that low NF and high IIP3 are hard to achieve simultaneously. We noticed that bias current had a big influence on the parameters of BJT, including NF and IIP3. Lowest NF (NF_{OPT}) could be obtained as colle-

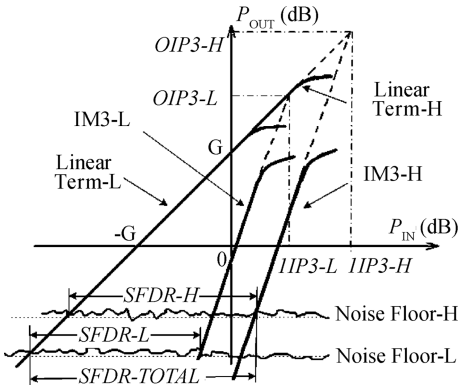


Fig. 7. Expanding SFDR with low and high bias current. G: Power gain of LNA.

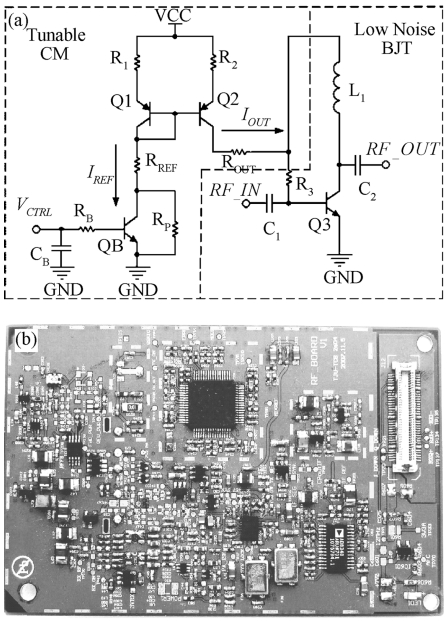


Fig. 8. (a) Schematic of an LNA with tunable CM circuit; (b) PCB of the RF front-end of the receiver.

ctor current density is around 38 μA/unit_area[8]. And according to BJT's Volterra model[9], IIP3 increases as collector current grows.

Then we proposed a method, adjusting the LNA's bias current according to the strength of received signal, to harmonize the contradiction between low NF and high IIP3 in the narrow bandwidth wireless system. In detail, when receiving weak signal, the receiver can adjust the bias current to obtain NF_{OPT} for high sensitivity. On the other hand, high IIP3 is achieved by increasing bias current for dealing with strong received signal. Figure 7 shows the SFDR of LNA with low and high bias currents. The parameters' names ending up with '-L' and '-H' represent low and high bias current, respectively. The expanded SFDR (SFDR-TOTAL) is the union of SFDR-L and SFDR-H. Therefore, the SFDR is expanded with the tunable bias current.

The complete schematic of the designed LNA is shown in Fig. 8(a). This LNA has been successfully applied in a narrowband wireless receiver. Figure 8 (b) shows the photo of the RF front-end PCB of the receiver. The frequency band of receiving signal is at 860 MHz. And the requirements of the LNA are: Gain > 8 dB, IIP3 > 18 dBm, NF < 1.5 dB.

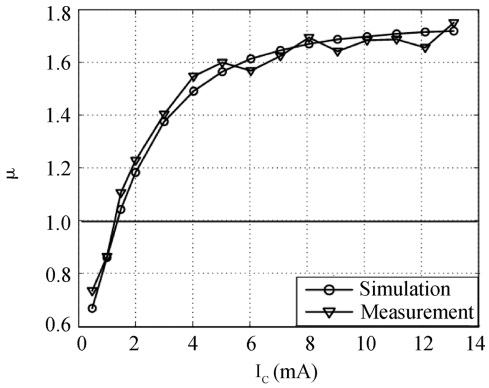


Fig. 9. Measurement and simulation results of μ criterion.

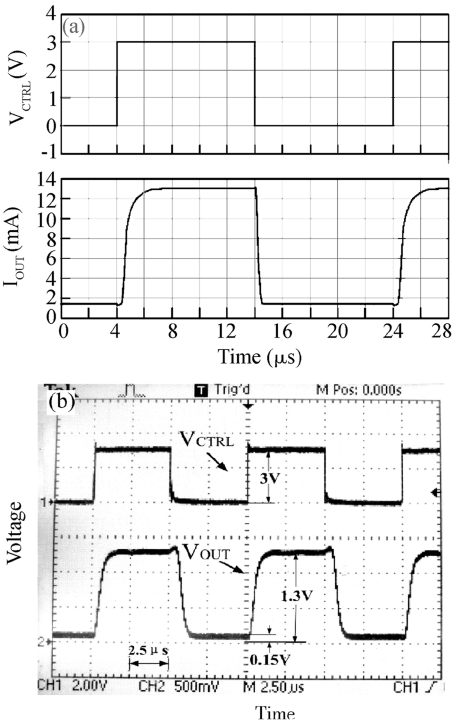


Fig. 10. Waveform of I_{OUT} as V_{CTRL} changes: (a) Simulation result; (b) Measurement result: the photo of waveform on oscilloscope screen. V_{OUT}: Voltage over R_{OUT}, Representing I_{OUT}. (R_{OUT} = 100 Ω).

As the provider of bias current, a simple and convenient CM is preferred rather than an accurate one. Here, the digital control method introduced in part 3.2 was adopted. 1-bit controlling signal (V_{CTRL}) divides the output of CM into two values. 1 and 0 of V_{CTRL} result in high and low bias currents, respectively. Since the required minimum of bias current is above zero, R_P was utilized as the determination of minimum output current of the CM.

The stability of the BJT should be examined before deciding the range of the bias current. The μ criterion was utilized to examine the stability. Figure 9 shows the curve of μ value versus bias current. It is obvious that the LNA is stable ($\mu > 1$) when bias current is greater than 1.5 mA. Considering the required NF, IIP3 and convenience of network matching, the range of bias current is set from 1.5 to 13 mA.

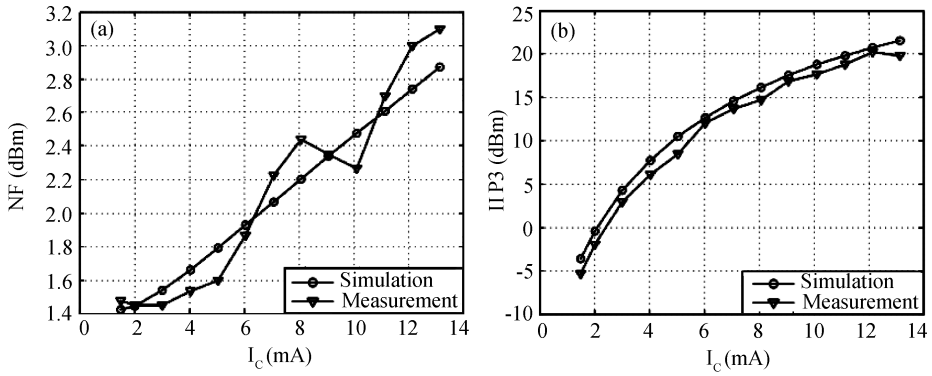


Fig. 11. Measurement and simulation results of LNA: (a) NF versus bias current; (b) IIP3 versus bias current.

Table 1. Comparison of LNAs' performance.

	Freq. (MHz)	Gain (dB)	IIP3 (dBm)	NF (dB)
This work	860	9	19.83	1.47
Bias current at 5 mA	860	9.1	8.51	1.62
Ref. [10]	800–2100	14.5	16	2.6
Ref. [11]	869–896	16.2	8	1.2
Ref. [12]	900	17	–5.1	3.4

Then the performance of the CM is investigated. Figure 10(a) gives simulation results, including the waveform of the $V_{\rm CTRL}$ and $I_{\rm OUT}$. Figure 10(b) gives the measurement result where the voltage of $R_{\rm OUT}$ ($V_{\rm OUT}$) is tested. Since $I_{\rm OUT}$ flows through the $R_{\rm OUT}$, $V_{\rm OUT}$ can represent $I_{\rm OUT}$. It is due to the parasitic capacitance that there is a little while between shifting edges of $V_{\rm CTRL}$ and $I_{\rm OUT}$. $I_{\rm OUT}$ becomes steady in 5 μs after $V_{\rm CTRL}$ changes and the steady low and high values of the $I_{\rm OUT}$ meet the design specifications.

The NF and IIP3 of the LNA are measured. Figure 11 gives the NF and IIP3 values of the LNA.

In contrast, another experiment where the LNA's bias current was set still to 5 mA was also performed. Table 1 gives performance comparison between these two experiment and some other LNAs reported recently.

According to the measurement results, the LNA with tunable bias current satisfy the required specifications. Compared with an LNA with a constant bias current (5 mA), this adjustable LNA has obvious advantages, e.g. the NF is improved by 0.15 dB and IIP3 is increased by 11.32 dB.

5. Conclusion

The CM circuits proposed in this paper have tunable output current. There are two ways to tune the current. While one method utilizes an analog voltage source which has an almost linear relationship with the output current, the other one makes use of an N-bit digital signal input which divides the output current into 2^N values. The CM has the advantages of simplicity and convenience in use.

The tunable CM has been applied as the bias current of the LNA in a wireless receiver. As the bias current is tunable, the LNA can achieve a lower NF and a higher IIP3 than a conventional one. Then a larger dynamic range is achieved with the method of tuning the bias current according to the strength of the received signal.

The experimental results of the CM and LNA are both very consistent with the theoretical analysis.

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