A 4 W K-band GaAs MMIC power amplifier with 22 dB gain

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Abstract: A 4 W K-band AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) monolithic microwave integrated circuit (MMIC) high power amplifier (PA) is reported. This amplifier is designed to fully match for a 50 Ω input and output impedance based on the 0.15 μm power PHEMT process. Under the condition of 5.6 V and 2.6 A DC bias, the amplifier has achieved a 22 dB small-signal gain, better than a 13 dB input return loss, and 36 dBm saturation power with 25% PAE from 19 to 22 GHz.

Key words: K-band; power amplifier; MMIC; PHEMT
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1. Introduction

Low cost, light weight, high yield, and good reliability are the key parameters for the successful development of modern communication applications. After several decades of development, the GaAs pseudomorphic high electron mobility transistor (PHEMT) has emerged as a high performance, low cost, and manufacturable device. Not only does it exhibit excellent noise properties, but it is also the premier power device for frequencies ranging from low microwaves through millimeter waves[1−7]. Accordingly, it is the ideal device for applications that require high performance, including digital point-to-point radio, future cellular, LMDS, and satellite communication.

Compared to hybrid pre-matched FET mini-modules which are delivered in hermetic sealed ceramic packages[8], the availability of power PHEMT processes capable of handing very high power densities now gives the opportunity to synthesize all matching, biasing, and DC block circuits in a monolithic die, with obvious advantages in terms of cost, space, reliability, and performance reproducibility. Since the overall power of a module is determined primarily by the power amplifier, every effort must be made to maximize the power of the amplifier. Recently, K-band MMIC power amplifiers have been reported[9−11] and widely used as commercial components[12, 13]; however, they present the performances with lower power, lower gain or lower power added efficiency (PAE).

In this paper, we present a 4 W MMIC power amplifier, which is designed to fully match for a 50 Ω input and output impedance without any external circuit. Under the condition of 5.6 V and 2.6 A DC bias, the amplifier delivers 36 dBm (4 W) saturated output power, 22 dB small-signal gain with 25% PAE from 19 to 22 GHz.

2. Process selection

The MMIC power amplifier described in this paper is fabricated in foundry using the 0.15 μm power PHEMT process. The advanced 6-inch process with the epitaxy design provides excellent low noise and high power performance with good temperature stability and reliability. Table 1 provides typical FET characteristics of the foundry's 0.15 μm power PHEMT process.

The power PHEMT process utilizes a 4 mil thick substrate and slot via under every source for high gain and improved thermal properties thus allowing the CW operation. Also air bridges with minimal interconnect capacitance, 400 pF/mm^2 MIM SiN capacitors and 50 Ω/□ TaN resistors are provided.

3. Circuit design

The proposed power amplifier consists of three stages. The periphery of the 1st FETs is 1.2 mm (two 600 μm FETs combined) and the unit gate width is 75 μm. The periphery of the 2nd stage FETs is 3.2 mm (four 800 μm FETs combined) and the unit gate width is 100 μm. The periphery of the last stage FETs is 6.4 mm (eight 800 μm FETs combined) and the unit gate width is 100 μm. The PHEMT periphery ratio between the output stage FETs and the 2nd ones is 2 : 1, which ensures the output power of the 2nd stage FETs is large enough to drive the output stage FETs into saturation over process variation.

The schematic diagram and the corresponding photograph of the fabricated MMIC for the completed power amplifier are shown in Figs. 1 and 2, respectively. The dimension of the chip is 4.25 × 4 mm^2. The design is achieved by adopting proper

Table 1. Typical FET characteristics.

Symbol	Parameter	Typical value
f_t	Transition frequency	85 GHz
I_{max}	Maximum drain current	650 mA/mm
I_{dss}	Saturated drain current	500 mA/mm
g_m	Transconductance	495 mS/mm
V_{DG}	Breakdown voltage	10 V
V_{PO}	Pinch-off voltage	−1.0 V
R_{on}	Ohmic contact resistance	0.2 Ω·mm

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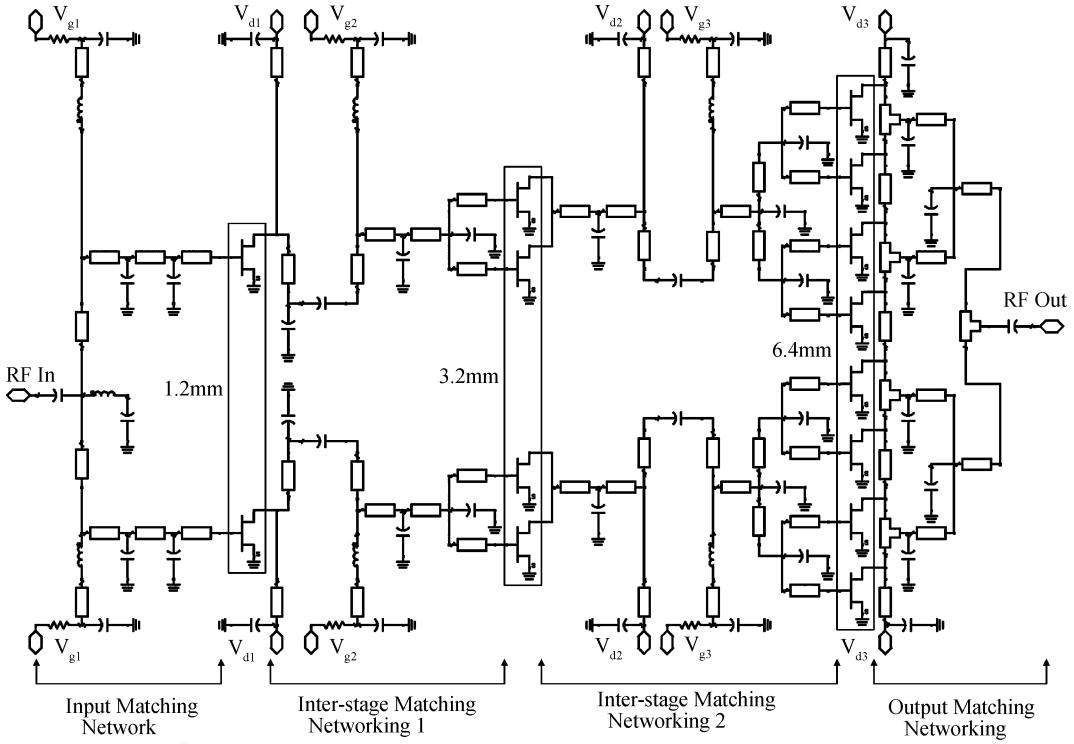

Fig. 1. Schematic diagram of the PHEMT MMIC power amplifier.

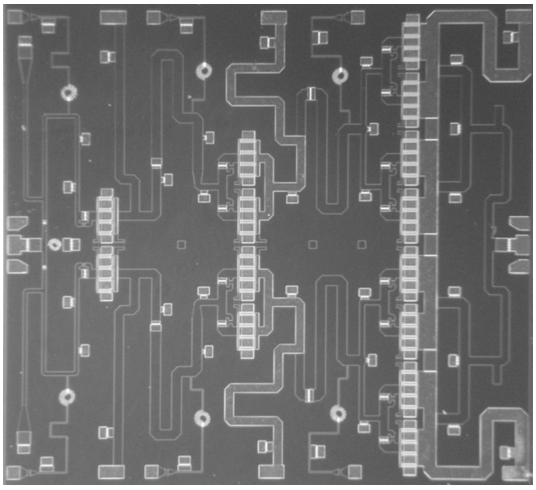

Fig. 2. Photograph of the fabricated PHEMT MMIC power amplifier.

matching topology and using both lumped elements and distributed elements[14].

To design the power amplifier, the output matching network, which transfers maximum output power from the FETs to the 50 Ω system, is designed first. The computer load pull simulation of the nonlinear model using Agilent's ADS is performed to determine power and efficiency load contours, and then the required optimized large signal load impedance Z_{opt} is obtained.

The topology of the power matching network is a bus–bar combiner[15] which forms an impedance transformer. The most obvious advantage of this type of combiner is the ease of providing the high DC current to all the output devices from either side of the chip, and this direct bus–bar connection between devices usually eliminates all odd-mode oscillations. A special care is dedicated to minimize the combiner loss since it influences the output power directly.

The inter-stage network between the 2nd stage FETs and the output stage FETs is also designed for the aforementioned maximum power load. In this case, the power splitting loss has to be minimized.

Recognizing that problems may arise due to inadequate bias line isolation, several decoupling structures are developed with increasing current handling capability. Gate and drain bias networks are $\lambda/4$ high impedance lines followed by MIM capacitors with slot vias placed closely to maintain high isolation at K-band.

In order to suppress instabilities, the odd-mode clamping resistors are incorporated in both the gate and drain sides to prevent odd-mode oscillations, and series TaN resistors are used in the gates bias network to prevent low-frequency oscillations. Then the circuit stability is further evaluated by the simulation of K and Δ factors[16, 17].

Electromagnetic simulations using Agilent's Momentum are performed to improve the design of tuning circuits. The areas of the chip that are most impacted by electromagnetic simulation do not simulate well using standard microstrip elements and therefore they are adjusted significantly in the E/M simulation results. The shunt tuning capacitors also require adjustment in the E/M simulation.

4. Measurement results

The amplifier is mounted on a carrier for plate with two thick film microstrips which are mounted beside the input and output pads of the MMIC for SMA jack transition. These transitions are then connected to the MMIC using two wire bonds

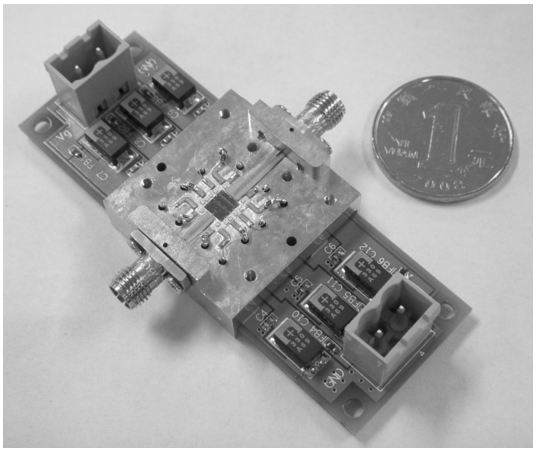

Fig. 3. The assembly module of MMIC power amplifier.

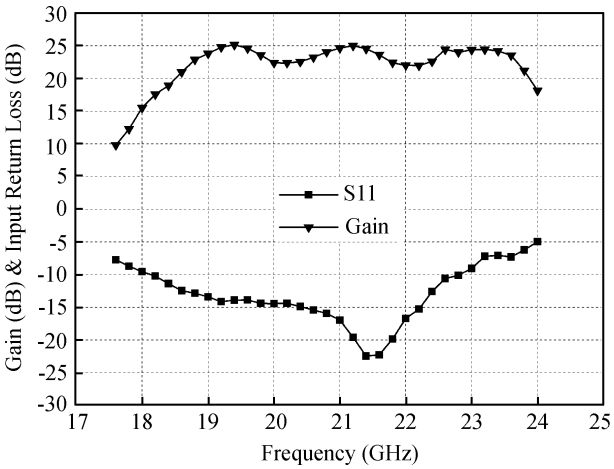

Fig. 4. Small signal gain and input return loss versus frequency.

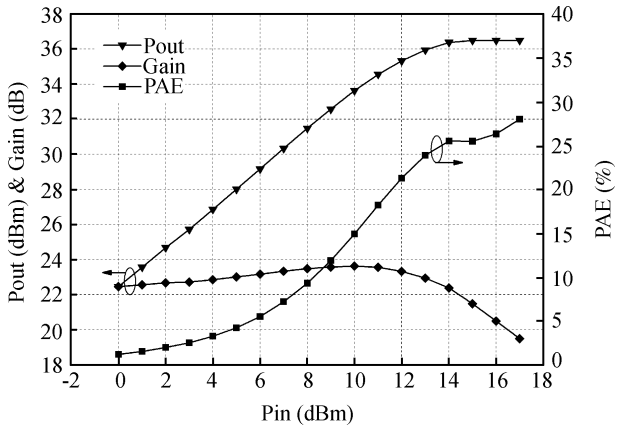

Fig. 5. Measured P_{out}, gain and PAE of the power amplifier versus input power at 20 GHz.

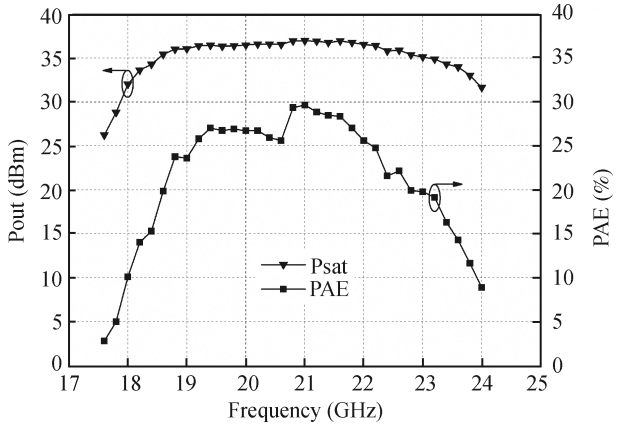

Fig. 6. Measured P_{out} and PAE of the power amplifier versus frequency with 16 dBm input power.

on the input and output. The reference plane for all measurements is de-embedded to the end of the transition microstrip. The assembly module is presented in Fig. 3. All measurements are carried out under pulse conditions of 100 μs pulse width and 10% of duty cycle. The bias conditions for the MMIC are $V_{\text{d}} = 5.6$ V, $V_{\text{g}} = -0.55$ V, and quiescent current $I_{\text{ds}} = 2.6$ A.

The measured small signal gain and input return loss versus frequency are shown in Fig. 4. The small signal gain is higher than 22 dB, and the input return loss is better than 13 dB from 19 to 22 GHz.

The measured power, gain and PAE of the power amplifier versus input power at 20 GHz are shown in Fig. 5. It can be observed that the saturated output power is 36.5 dBm with 28% PAE.

A typical frequency response of the power amplifier is shown in Fig. 6 for P_{out} and PAE with 16 dBm input power. As shown there, P_{out} is higher than 36 dBm and the PAE is higher than 20% from 19 to 22 GHz.

5. Conclusion

In summary, a K-band high-power PHEMT MMIC power amplifier has been designed and fabricated using the 0.15 μm power PHEMT process. At a drain voltage of 5.6 V, saturated output power of 36 dBm from 19 to 22 GHz has been obtained. In addition, excellent performance with a 22 dB small-signal gain, 25% PAE and better than 13 dB input return loss can be achieved.

The MMIC technology and compact design approach combined with extensive E/M simulation have made the K-Band MMIC power amplifier successful.

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