Threshold voltage adjustment of organic thin film transistor by introducing a polysilicon floating gate

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Abstract: The structure of organic thin film transistors (OTFTs) is optimized by introducing a floating gate into the gate dielectric to reduce the threshold voltage of OTFTs. Then the optimized device is simulated, and the simulation results show that the threshold voltage of optimized device is reduced by about 10 V. The reduction of the threshold voltage is helpful and useful for the application of OTFTs in many areas. In addition, this way of reducing the threshold voltage of OTFT is compatible with traditional silicon technology and can be used in manufacturing.

Key words: pentacene OTFT; device optimization; Pool–Frenkel mobility; simulation
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1. Introduction

Organic thin film transistors (OTFTs) have received considerable attention in the last two decades, owing to the possibility of producing low-cost, large-area, lightweight, and flexible devices[1−5]. Although the performance of OTFTs has obtained tremendous improvement owing to the application of pentacene in recent years[6−8], the high threshold voltage of OTFT is still a big challenge in the production of functional devices. For example, the threshold voltage is no less than –10 V in most OTFT devices, which is unacceptable and needs to be reduced for low-power operation[9, 10], especially in portable devices.

Several groups have focused on reducing the threshold voltage of OTFT by using self-assembled monolayers or a nanoparticle floating gate[11, 12], but their methods are too difficult and too expensive to be used in manufacture. In this paper, we propose a new structure for OTFTs introducing a poly-Si floating gate into the gate dielectric layer; the floating gate serves as a potential well (or trap) that collects and stores the hot- or tunneling-electron charges from the organic layer, and thus decreases the threshold voltage. We choose polysilicon as a floating gate material, because a polysilicon floating gate is compatible with traditional silicon technology. Furthermore, a potential well between the polysilicon floating gate and the SiO_2 is formed, and this potential well is so deep that once electrons get into the floating gate, they are trapped in the floating gate forever.

2. Device structures and model

Owing to the peculiar nature of the organic semiconductor materials, OTFTs are primarily operated as accumulation mode as opposed to the usual inversion mode of silicon MOSFETs[13, 14]. The mobility of the OTFT usually increases with the gate voltage, which is the evidence for hopping transport mechanism in organic semiconductors[13, 15]. Owing to the differences of its operation mode and the charge transport mechanism, the model used for silicon MOSFET must be modified in order to describe electrical characteristics of OTFTs. In this paper, the drift–diffusion model (DDM)[16] is modified which incorporates Pool–Frenkel carrier mobility[17], interface charges at interface between semiconductor and insulator, contact barrier and trap distribution at dielectric-semiconductor interface[15, 18]. The simulation predicts the electrical characteristics of a specified device by solving Poisson's equation and continuity equations given by Eqs. (1)–(3)[16, 19]:

$$\mathrm{div}(\varepsilon\nabla\psi) = q(n - p + n_\mathrm{t} - p_\mathrm{t}), \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\mathrm{div}\boldsymbol{J}_\mathrm{n} + G - R, \tag{2}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\mathrm{div}\boldsymbol{J}_\mathrm{p} + G - R, \tag{3}$$

where ψ is the electrostatic potential, ε is the permittivity of organic material, G is the generation rate, n_t and p_t are the densities of trapped electrons and holes respectively, $\boldsymbol{J}_\mathrm{n}$ and $\boldsymbol{J}_\mathrm{p}$ are the electron and hole current densities respectively, R is the electron and hole recombination rate expressed as $R = \frac{qnp}{\varepsilon}(\mu_\mathrm{n}(E) + \mu_\mathrm{p}(E))$[13, 20], and μ_n and μ_p are the electron and hole mobilities which are electric field dependent in most organic materials. In order to describe the field-effect mobility, Pool–Frenkel mobility model is applied to the simulation. This mobility model is presented as follows:

$$\mu(E) = \mu_0 \exp\left[-\frac{E_0}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\sqrt{E}\right], \tag{4}$$

where E_0 is activation energy, β is the Pool–Frenkel factor, γ is fitting parameter, and μ_0 is the low field mobility.

The electron and hole concentrations in organic materials are described as[21]:

$$n = N_\mathrm{LUMO} \exp\left[(F_\mathrm{n} - E_\mathrm{LUMO})/kT\right], \tag{5}$$

$$p = N_\mathrm{HOMO} \exp\left[(E_\mathrm{HOMO} - F_\mathrm{p})/kT\right], \tag{6}$$

where T is the device temperature, k is Boltzmann's constant, E_LUMO and E_HOMO are energy levels of the lowest unoccupied

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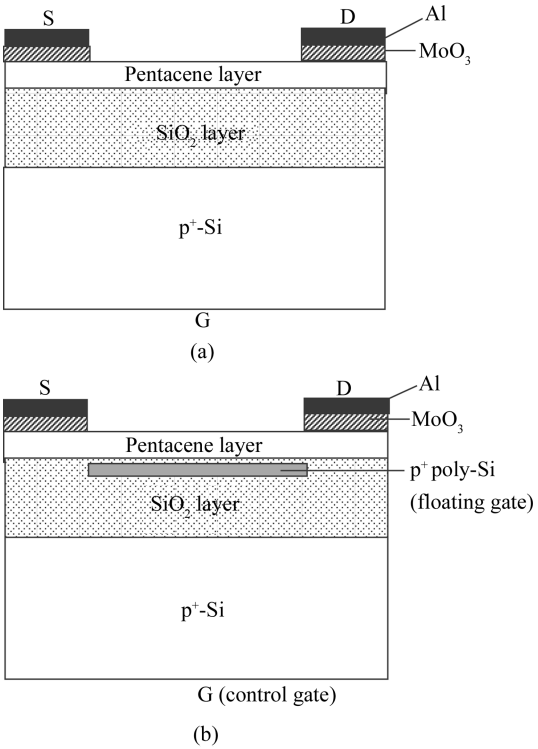

Fig. 1. Cross-section of (a) the conventional and (b) floating gate organic thin film transistor structures.

molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), F_p and F_n are quasi-Fermi levels for electrons and holes, and N_{LUMO} and N_{HOMO} are the densities of the states in LUMO and HOMO, respectively.

Many studies have shown that contact barriers, fixed charges and traps significantly affect the electrical characteristics of OTFT[18, 21]. In order to obtain accurate simulation results, the contacts are not considered as ohmic contacts, but as Schottky barriers of 0.3 eV and the fixed charge density at interface between semiconductor and insulator is 3×10^{10} cm^{-2}. At last, considering the effect of traps from structural defects in pentacene film and dielectric–semiconductor interface, we include the trap distribution into the simulations. An exponential distribution form is used for trap density and given as[21]:

$$g(E) = \frac{N_{TA}}{kT_t} \exp\left[(E - E_{LUMO})/kT_t\right], \qquad (7)$$

where $g(E)$ is trap density at energy E, T_t is the characteristic temperature of the exponential trap distribution, and N_{TA} is the total density of the traps. The effect of traps is incorporated into Poisson's equation to get accurate results[22, 23].

Figure 1(a) shows the schematic diagram of a conventional top-contacted pentacene OTFT structure. A heavily-doped p-type Si wafer is used as the gate electrode. The MoO_3 layer between the pentacene and Al layers is used to reduce the contact barrier and prevent aluminium from diffusing into pentacene[10, 24]. Figure 1(b) shows an optimized device structure introducing a polysilicon floating gate into the gate dielectric to decrease the threshold voltage.

The floating gate reduces threshold voltage in such a way: the floating gate serves as a potential well owing to the bandgap difference of Si and SiO_2 layer. Under relatively large control-gate and drain bias (both are positive relative to the source), electrons can get into the potential well by the Fowler–Nordheim mechanism or surmounting the energy barrier between Si and SiO_2 and the electrons in the well will stay there forever due to the large barrier height (about 3.2 eV). Then the electrons in the well produce an electric field in the neighborhood of the pentacene–SiO_2 interface by attracting the holes from pentacene to accumulate at the interface; this is equivalent to apply a certain-value negative bias to the control gate, therefore leading to a threshold voltage decrease. The more the electron charges in the well, the more the threshold voltage is decreased.

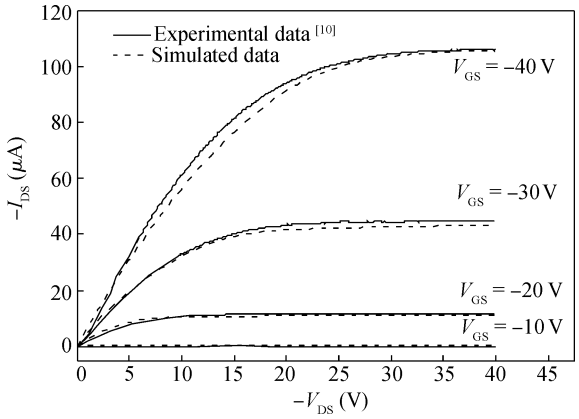

Fig. 2. Output characteristics of conventional pentacene OTFT.

3. Simulation results and discussions

Numerical simulations are performed for both optimized and conventional OTFTs using otherwise identical conditions (including structural and electrical parameters). In the simulations, the pentacene layer thickness is taken as 40 nm, and the length and width of the channel are 100 μm and 5 mm, respectively. The thickness of the floating gate is 40 nm, and the thicknesses of SiO_2 layers above the floating gate are 20 nm. The dielectric constant, bandgap, and electron affinity for pentacene are given by 4.0, 2.25 eV, and 2.49 eV, respectively[25, 26].

To verify the reliability and validity of the numerical model used, first we compare the simulation results with experimental data[10] for the conventional OTFT, as shown in Figs. 2 and 3. It is clear that the simulation data are in good agreement with the experimental data. It is also clear from Fig. 3 that the threshold voltage of the OTFT device is about 10 V, which is too large for practical applications.

Figures 4 and 5 show the simulation results, the output characteristic curves of the optimized pentacene OTFT and the transfer characteristics of OTFTs with and without the floating gate, respectively. Comparing the output characteristics of the two devices (Figs. 2 and 4), we note the great differences of the drain currents under the same gate biases (V_{GS}). These differences are due to the decrease of threshold voltage as a result of the floating gate.

The transfer characteristic shifts by about 10 V after optimization as shown in Fig. 5 and the threshold voltage decreases from -9.5 to -0.2 V when a floating gate is introduced into the

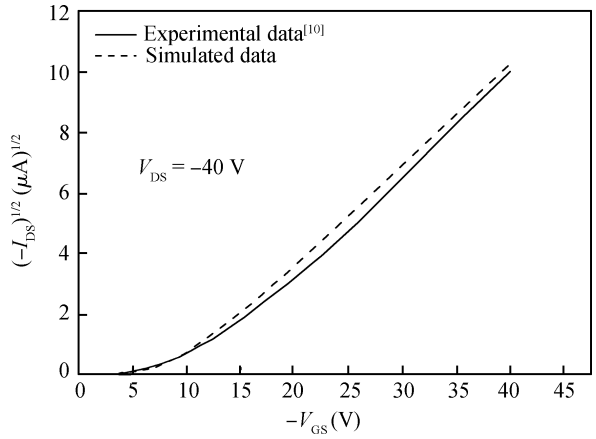

Fig. 3. Transfer characteristics of conventional pentacene OTFT.

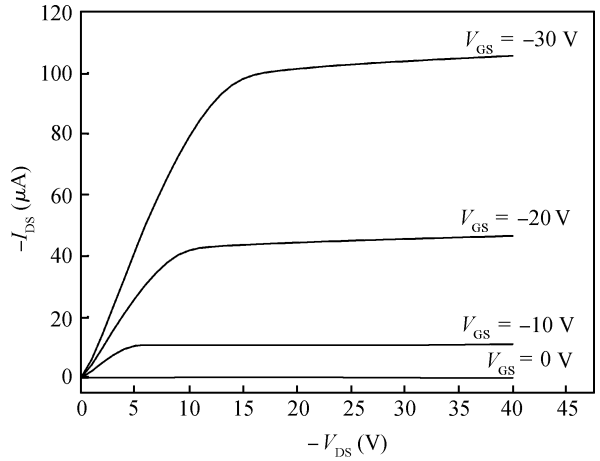

Fig. 4. Output characteristic curves of the optimized pentacene OTFT.

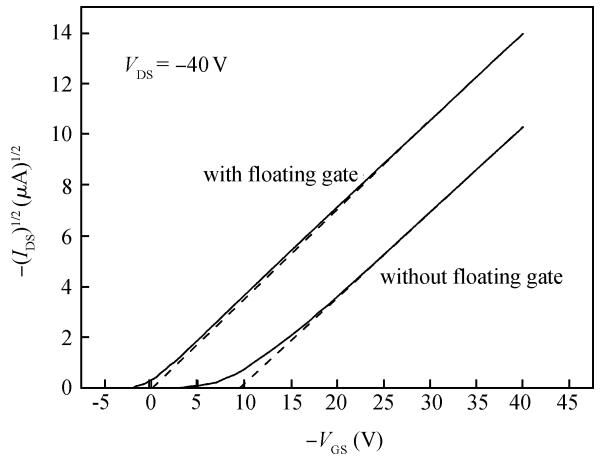

Fig. 5. Comparison of the transfer characteristics of OTFTs with and without floating gate.

device. The charges in the floating gate exert influence on the threshold voltage in a similar way the interface charges (Q_i) exert influence on the flat-band voltage (V_{FB}) of a MOS structure: the charges act a role similar to the interface charges in the MOS structure, thus the decrease of threshold voltage can

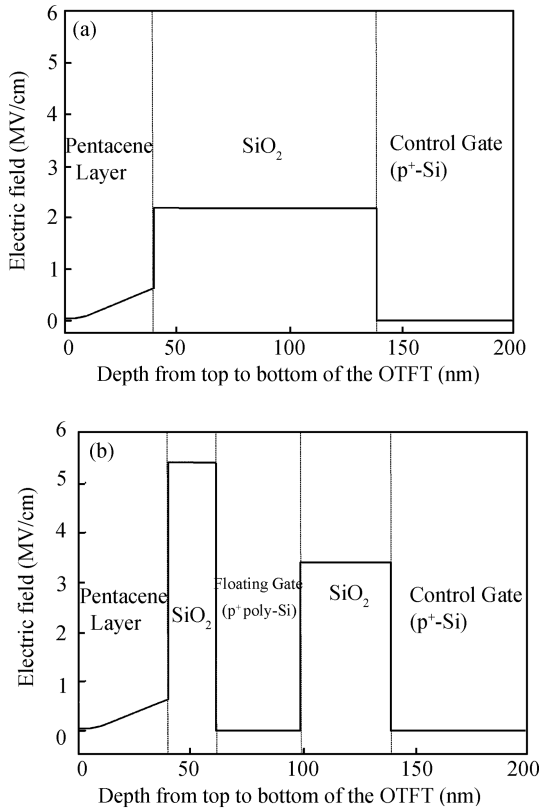

Fig. 6. Longitudinal electric field profile in the OTFTs (a) without a floating gate and (b) with a floating gate. Both the two plots are drawn in same scale at same biases $V_{GS} = 30$ V and $V_{DS} = 40$ V.

be explained by:

$$V_T = V_{T0} - \frac{Q_{FG}}{C_{FG-CG}} = V_{T0} - \frac{Q_{FG}}{\varepsilon_{ox}/d_{FG-CG}}, \qquad (8)$$

where V_T and V_{T0} is the threshold voltage of the OTFT with and without a floating gate respectively, Q_{FG} is the sheet charge density (assuming the thickness of the poly-Si is negligible), C_{FG-CG} is the capacitance per unit area of the SiO_2 layer between the floating and control gates, ε_{ox} is the dielectric constant of SiO_2, and d_{FG-CG} is the distance between the floating gate and the control gate. Note that all quantities in the equation have their absolute values.

The decrease can also be explained by Figs. 6(a) and 6(b) from the perspective of the electric field. Figures 6(a) and 6(b) show the longitudinal electric field profile in the OTFTs without a floating gate and with a floating gate respectively.

According to Maxwell Equations, the difference of electric fields at the interface between different materials results from charge density at the interface and it is given by

$$\varepsilon_0(E_1 - E_2) = \sigma, \qquad (9)$$

where ε_0 is the permittivity of vacuum, E_1 and E_2 are the electric field perpendicular to interface on both sides of interface, σ is the charge density at the interface. From Eq. (9), the more charges at interface produce the bigger difference of electric fields between different materials. As Figures 6(a) and 6(b) show, the difference of electric fields at the interface between pentacene and SiO_2 is much bigger in the optimized device

than that of the normal device, under the same gate voltage. This indicates that much more carriers accumulate in the region of the pentacene layer that is close to the SiO_2 layer in the optimized device, which can be explained by the fact that not only the gate voltage gives rise to the accumulation of carriers but also the charges on the floating gate can induce carriers in the active layer in the optimized device. So the threshold voltage can be reduced by electrostatic induction of the charges in the floating gate.

4. Conclusion

The threshold voltage of organic thin film transistor is studied in this paper. A polysilicon floating gate is introduced into the device structure to reduce the threshold voltage of OTFT. The threshold voltage is reduced by about 10 V after the optimization, which is explained from the perspectives of floating gate charge and of the electric field in this paper. The reduction of threshold voltage is helpful in lowering the device power consumption and useful in producing functional portable devices. In addition, this way of reducing threshold voltage is compatible with traditional silicon technology. This method of reducing threshold voltage can be used to produce low threshold voltage organic devices in manufacturing.

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