Wet etching characteristics of a HfSiON high-k dielectric in HF-based solutions*

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Abstract: The wet etching properties of a HfSiON high-k dielectric in HF-based solutions are investigated. HF-based solutions are the most promising wet chemistries for the removal of HfSiON, and etch selectivity of HF-based solutions can be improved by the addition of an acid and/or an alcohol to the HF solution. Due to densification during annealing, the etch rate of HfSiON annealed at 900 °C for 30 s is significantly reduced compared with as-deposited HfSiON in HF-based solutions. After the HfSiON film has been completely removed by HF-based solutions, it is not possible to etch the interfacial layer and the etched surface does not have a hydrophobic nature, since N diffuses to the interface layer or Si substrate formation of Si–N bonds that dissolves very slowly in HF-based solutions. Existing Si–N bonds at the interface between the new high-k dielectric deposit and the Si substrate may degrade the carrier mobility due to Coulomb scattering. In addition, we show that N_2 plasma treatment before wet etching is not very effective in increasing the wet etch rate for a thin HfSiON film in our case.

Key words: HfSiON; high-k; wet etching; interfacial layer
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1. Introduction

As MOSFET dimensions scale down to the 45 nm node and beyond, there is an urgent need to introduce high-k gate dielectrics and metal gate electrodes with appropriate work functions to reduce the gate direct tunneling leakage current and to eliminate the poly-Si gate depletion effect, the boron penetration effect and Fermi-level pinning[1]. However, the integration of metal gate/high-k dielectric stacks into the CMOS flow poses significant challenges. One of the biggest problems is the formation of two different metal/high-k stacks for N and PMOSFETs in different regions of the wafer. Samavedam *et al.* proposed a deposition-etch-deposition approach to integrate a dual metal gate with the same high-k dielectric for N and PMOSFETs[2]. However, the drawback of this scheme is that the high-k dielectric is exposed to metal wet etching, which can degrade the integrity of the high-k dielectric, and gate stack etching needs to accommodate differences in the thickness of the metal layers for N and PMOSFETs. In addition, recent reports indicate that the effective work function of a metal gate has a strong dependence on high-k film composition and different high-k films may be required for N and PMOSFETs[3]. Thus, the removal of high-k from N or PMOSFET regions after the first metal gate wet etch is a key process to achieve metal gate/high-k dielectric integration, since it not only obtains undamaged high-k by the same high-k film deposition but also obtains different high-k films for N and PMOSFETs by different high-k film depositions to achieve the target V_t.

Among the potential high-k material candidates, HfSiON seems to be one of the most promising alternative gate dielectrics due to its several merits, such as a relatively high dielectric constant, thermodynamic stability in direct contact with silicon, low leakage current, high crystallization temperatures, and good interface properties[4]. Although chlorine-based plasmas, such as Cl_2 or BCl_3, could selectively remove the HfSiON film, the etch selectivity of dry etching of HfSiON film to Si substrate is very low, which can result in significant consumption of Si substrate and high series resistance, affecting the device performance[5]. Therefore, a wet etch process, which has a large process margin for the 45 nm node layout design rule, is a good choice to remove HfSiON film from N or PMOSFET regions. In this paper, we study the wet etch properties of HfSiON film in HF-based solutions and the effects of post deposition annealing (PDA) on the etch rate of HfSiON high-k dielectric film. Moreover, the existing interfacial layer characteristics after HfSiON removal and the impact of N_2 plasma treatment before wet etching on the HfSiON etch rate are also addressed.

2. Experiment

After a standard clean process, the Si wafer was treated with an HF/IPA/H_2O solution to remove the contaminants on the surface and suppress the growth of natural oxide. The HfSiON film was then deposited onto the SiO_2 interfacial layer by co-sputtering of Hf and Si targets at room temperature in Ar/N_2 ambient. The work pressure was kept at 5×10^{-3} Torr. After deposition, post deposition annealing using rapid thermal annealing was performed in N_2 ambient at 900 °C for 30 s. Some HfSiON samples were treated by N_2 plasma before wet etching. The N_2 plasma treatment conditions, such as N_2 gas flow, pressure, source power, and treatment time were 100 sccm, 200 mTorr, 150 W, and 10 s, respectively. The thicknesses and etch rates of HfSiON films were measured by a multiwavelength ellipsometer. The chemical composition and bonding states of the samples were investigated by X-ray photoelectron spectroscopy (XPS) measurements with a monochromatic AlKα

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Table 1. Etch rates of HfSiON and SiO_2 in HF-based solutions.

Solution	HF/H_2O	$HF/HCl/H_2O$	HF/HCl/ alcohol
Volume ratio	1 : 99	1 : 10 : 89	1 : 10 : 89
HfSiON etch rate (nm/min)	6.1	8.8	11.9
SiO_2 etch rate (nm/min)	1.76	1.49	0.58

(1486.6 eV) X-ray incident. The binding energy (BE) was referenced to C1s at 284.5 eV.

3. Results and discussions

3.1. Wet etch etchants of HfSiON

The common acids and alkalis used for current CMOS fabrication, such as HCl, HNO_3, H_3PO_4, H_2SO_4, NH_4OH, SPM ($H_2SO_4 : H_2O_2 = 1 : 5$) and SC1 ($NH_4OH : H_2O_2 : H_2O = 1 : 1.1 : 5$) could not etch HfSiON or the etch rates of HfSiON film were below several Å/min. For example, the etch rates of HfSiON film annealed at 900 °C for 30 s in SC1 at 60 °C and SPM at 120 °C were only 0.13 Å/min and 2.9 Å/min. However, it was found that the etch rates of HfSiON film in dilute HF solution are significantly higher than other common acid and alkali solutions since HfF_4 is highly soluble in HF solution. Therefore, dilute HF solution was very effective for etching HfSiON high-k material.

Development of a wet etch etchant for selective removal of HfSiON material from N or PMOSFET regions is challenging work since the removal of HfSiON must be carried out with high selectivity to the gate electrode, the isolation dielectric, and the underlying silicon. Because dilute HF solution has a fast etch rate with HfSiON material and has high selectivity to the Si substrate, polycrystalline Si and some metal gates, such as TaN, the only limiting factor is the low selectivity to the exposed field oxides. In the HF solution, the generation of F^-, HF_2^- ionic species and HF, H_2F_2 molecular species is responsible for SiO_2 and HfSiON etching, respectively[6]. In order to obtain a high selectivity towards SiO_2 with HF-based solutions, the etchants must restrain the concentration of the F^-, HF_2^- ionic species and increase the concentration of the HF and H_2F_2 species. It was found that adding an acid and/or an alcohol to an aqueous HF solution can result in the increase of the relative concentration of HF and H_2F_2 species due to the reduced dissociation of the molecule. Table 1 shows the etch rates of HfSiON and SiO_2 in HF/H_2O (1 : 99), $HF/HCl/H_2O$ (1 : 10 : 89), and HF/HCl/alcohol (1 : 10 : 89) solutions. The etch selectivity of HfSiON to SiO_2 can be improved from 3.47 to 5.91 by the addition of 10% HCl to the 1% HF solution, and a selectivity of 20.5 : 1 is obtained by replacing water in the 1% HF solution with 10% HCl and 89% alcohol. So, adding an acid and/or an alcohol to the aqueous HF solution to control the active etch species could improve the selectivity of HfSiON to SiO_2 and satisfy the need for selective removal of HfSiON from the N or PMOSFET regions.

3.2. Effect of annealing on wet etching

As HF-based solutions are the most effective for etching HfSiON, HF/H_2O (1 : 99) is chosen to reveal the effect of annealing on the wet etching properties of HfSiON high-k dielectrics. Figure 1 shows the remaining thickness of as-deposited and annealed HfSiON film in HF/H_2O (1 : 99) as a function of etch time. Experimental results show that as-deposited films with thickness 60 Å can be removed by HF/H_2O (1 : 99) in only 10 s. However, after annealing at 900 °C for 30 s, the etch rates of the HfSiON film decreased sharply and required one minute to completely remove the HfSiON film. Crystallization and densification due to the annealing could be the main reasons responsible for the enhancement of the wet etching resistance of Hf-based high-k materials[7]. However, the previous experiment on HfSiON film annealed at 900 °C for 30 s by our group showed no crystalline structures[8], indicating that densification is the main reason responsible for the decrease of the etch rate. Moreover, for the annealed HfSiON films, the initial etch rate is low and the etch rate increases rapidly after dipping in HF/H_2O (1 : 99) for 20 s. The low initial etch rate may be because the surface of the relatively thick HfSiON film (6–7 nm) becomes more oxygen-rich compared with the bulk film due to substitution effects by residual oxygen in the chamber during the PDA process.

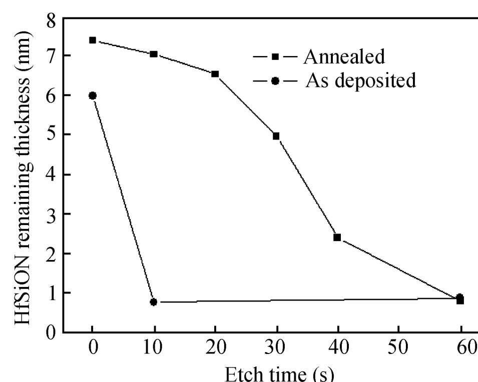


Fig. 1. Remaining thickness of HfSiON film, as-deposited and annealed at 900 °C for 30 s, as a function of etch time in HF/H_2O (1 : 99).

In addition, it was noted that the interfacial layer could not be etched and the etched surface did not have a hydrophobic nature after the HfSiON film was completely removed by the HF-based solution. Since HfN thin film was first sputtered on the ultrathin silicon oxide interface layer, a likely explanation for this could be the incorporation of nitrogen from the HfN film in the SiO_2 interfacial layer or Si substrate during the sputtering or PDA processes, forming Si–N bonds, which are known to be more resistant (their etch rate is 0.01 nm/min) to dilute HF solution[9]. Alternatively, the Hf element of the first-sputter HfN film could also have been incorporated in the oxide layer, converting it to Hf-rich film, which is also difficult to remove wet-chemically.

In order to clarify the Hf or N diffusion resulting in an interfacial layer which cannot be etched, XPS Hf4f, Si2p, and N1s core-level spectra for the 30 Å HfSiON annealed at 900 °C for 30 s and etched in $HF/HCl/H_2O$ (1 : 10 : 89) for 70 s are shown in Figs. 2 and 3. The etch time of 70 s ensures that there is enough time to remove the 30 Å HfSiON film completely. As shown in Fig. 2, no Hf signal was detected after wet etching in $HF/HCl/H_2O$ (1 : 10 : 89), indicating that the retardation of the interfacial layer etch was irrelevant to the Hf element. With

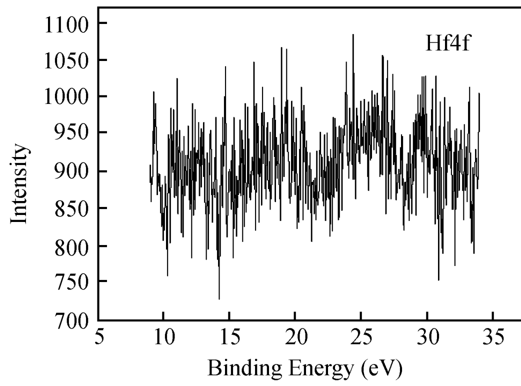
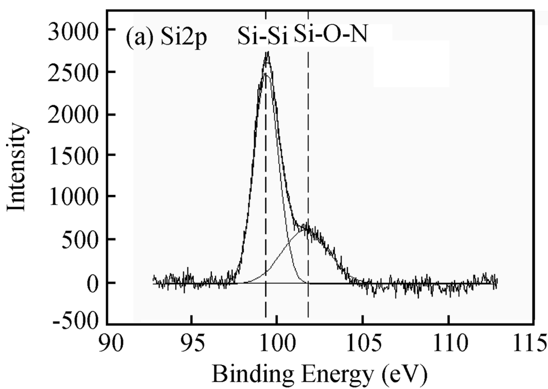


Fig. 2. Hf4f peaks from XPS for the annealed HfSiON (30 Å) after etching in HF/HCl/H_2O (1 : 10 : 89) for 70 s.



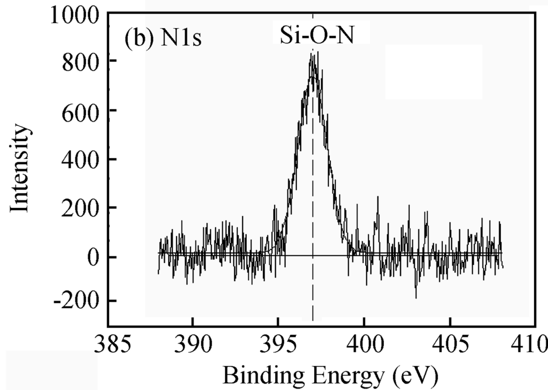
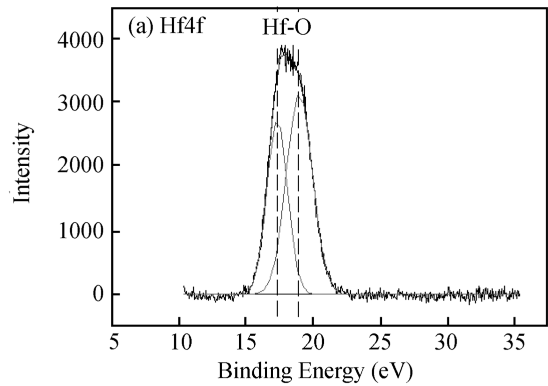


Fig. 3. (a) Si2p and (b) N1s XPS spectra for the annealed HfSiON (30 Å) after etching in 1% HF/10% HCl for 70 s.

regard to the Si2p core-level spectrum in Fig. 3(a), the main peak appears at 99.3 eV, which is the binding energy of bulk Si, and a shoulder at 101.7 eV indicates the formation of Si–O–N bonds in the interface layer. From the N1s core-level spectrum in Fig. 3(b), the dominant component is located around 397.8 eV, which corresponds to N atoms bonded with both Si and O[10]. From the above results, it can be concluded that the formation of Si–N bonds because of N diffusion to the interface layer or the Si substrate is responsible for the interfacial layer being almost impossible to etch. In addition, the existing Si–N bond at the interface may degrade the carrier mobility due to Coulomb scattering after the removal of HfSiON from the N or PMOSFET regions and new high-*k* material deposition.



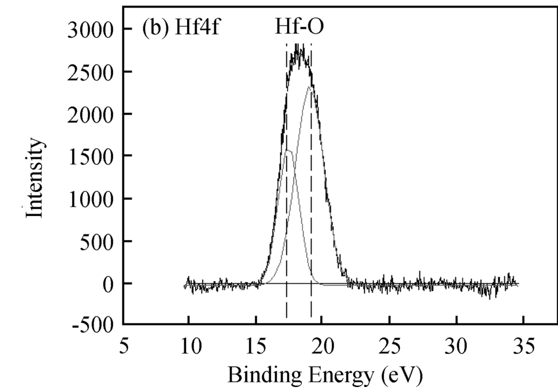


Fig. 4. XPS Hf4f core-level spectra for the 30 Å annealed HfSiON (a) before and (b) after N_2 plasma treatment.

3.3. Effects of N_2 plasma treatment on wet etching

It has been reported that N_2 plasma treatment is effective in removing crystallized HfO_2 films prior to wet removal by HF solution through the generation of a Hf–N bond that can easily be etched by HF solutions [11]. In order to investigate the effects of N_2 plasma treatment on the enhancement of the wet removal rate of HfSiON, N_2 plasma treatment was applied to the HfSiON annealed at 900 °C for 30 s before wet etching. For the 30 Å HfSiON film, our optimum N_2 plasma treatment conditions are that the N_2 gas flow is 100 sccm, pressure is 200 mTorr, source power is 150 W and treatment time is 10 s. Figure 4 shows the XPS Hf4f core-level spectra for the HfSiON films before and after N_2 plasma treatment under our optimum conditions. As shown in Fig. 4(a), the peak positions of Hf (4f7/2 and 4f5/2) without N_2 plasma treatment are located around 17.3 eV and 19.0 eV, which corresponds to the Hf–O bond in HfSiON[8]. However, the Hf peaks of the N_2 plasma treatment sample almost do not change, indicating that the incorporated N is not bonded to Hf. Namely, in our case, N_2 plasma treatment cannot chemically react with HfSiON film to form Hf–N bonds since the existence of Hf–N bonds will make the Hf peak position shift to a lower binding energy. The differences in the present experiment compared to the report of Chen *et al.*[11] may be caused by different high-*k* materials, the high-*k* material fabrication process and the N_2 plasma treatment equipment.

The Si2p photoelectron spectra for HfSiON film before and after N_2 plasma treatment are shown in Fig. 5. It can be observed that after N_2 plasma treatment, the high-binding-energy peak of the Si2p increased in intensity compared to the Si–Si

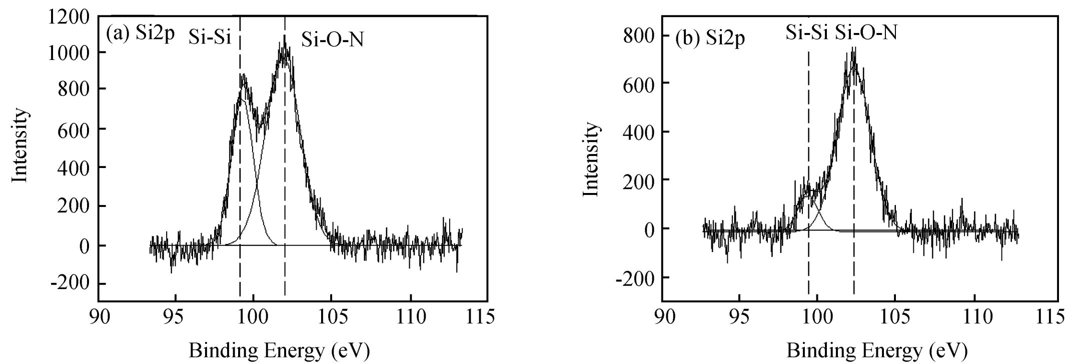


Fig. 5. XPS Si2p core-level spectra for the 30 Å annealed HfSiON (a) before and (b) after N_2 plasma treatment.

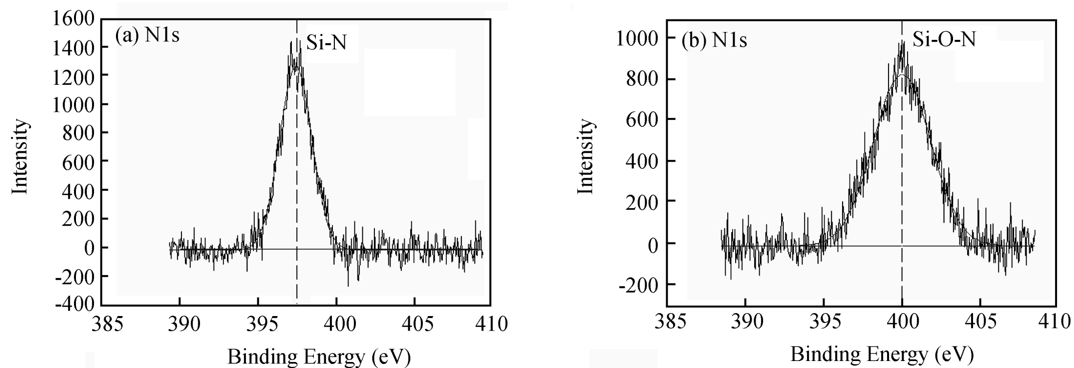


Fig. 6. XPS N1s core-level spectra for the 30 Å annealed HfSiON (a) before and (b) after N_2 plasma treatment.

bond, suggesting that the incorporated N tends to bond to Si, forming Si–N or Si–O–N bonds. The N1s photoelectron spectra before and after N_2 plasma treatment are shown in Fig. 6. As shown in Fig. 6(a), the dominant component located around 397.4 eV is assigned to the Si–N bond before N_2 plasma treatment in the HfSiON film. The width of the N1s spectrum in Fig. 6(b) become broader with N_2 plasma treatment and the peak energy position shifts by 2.7 eV toward a higher binding energy, indicating that the incorporated N was mostly chemically bonded as Si–O–N because the binding energy peaks of Si–N and N–O are 397.4 eV, 402.3 eV, respectively[12].

The wet etching rate of HfSiON in HF/HCl/H_2O (1 : 10 : 89) is 10.02 nm/min after N_2 plasma treatment. The reasons for the small enhancement in the etch rate of HfSiON by N_2 plasma treatment are as follows: first, N_2 plasma treatment does not generate Hf–N bonds that can increase the wet etch rate of HfSiON; second, N_2 plasma treatment introduces less physical damage than Ar ions due to its small mass; third, the energy or time of the N_2 plasma treatment was limited for the thin HfSiON (30 Å) in order to incorporate less N in the interface layer or Si substrate. So, N_2 plasma treatment is not very effective in increasing the wet etch rate in our case for the thin HfSiON (30 Å) dielectric used as MOSFET gate dielectrics of 45 nm node and beyond.

4. Conclusions

In conclusion, the wet etching properties of a HfSiON high-k dielectric in HF-based solutions have been studied. We have found that the etch rate of HfSiON is significantly reduced after PDA and high selectivity wet etching of HfSiON to field oxide could be achieved by controlling the active etch species in HF-based solutions. Also, the formation of Si–N bonds is responsible for the retardation of the interface layer removal and may reduce the carrier mobility due to Coulomb scattering after new metal gate/high-k dielectric stack formation. Moreover, N_2 plasma treatment is not very effective in increasing the wet etch rate for the thin HfSiON dielectric in our case.

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