Total ionizing dose effects and annealing behavior for domestic VDMOS devices

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Abstract: Total dose effects and annealing behavior of domestic n-channel VDMOS devices under different bias conditions were investigated. The dependences of typical electrical parameters such as threshold voltage, breakdown voltage, leakage current, and on-state resistance upon total dose were discussed. We also observed the relationships between these parameters and annealing time. The experiment results show that: the threshold voltage negatively shifts with the increasing of total dose and continues to decrease at the beginning of 100 °C annealing; the breakdown voltage under the drain bias voltage has passed through the pre-irradiation threshold voltage during annealing behaving with a "rebound" effect; there is a latent interface-trap buildup (LITB) phenomenon in the VDMOS devices; the leakage current is suppressed; and on-state resistance is almost kept constant during irradiation and annealing. Our experiment results are meaningful and important for further improvements in the design and processing.

Key words: VDMOS device; total dose effects; annealing; γ radiation
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1. Introduction

Due to their special structures, vertical double-diffusion metal oxide semiconductor (VDMOS) devices have high input impedance, low driven power, high switch speed, good hot stability, and particularly strong radiation-hardening ability. Meanwhile, they have negative temperature coefficients and do not have the so-called "second breakdown" as in normal transistors. With these advantages, VDMOS devices have been extensively applied to different fields, such as aerospace, military, and nuclear environments[1].

It is well known that there are a great of energetic charged particles, cosmic rays and solar flares in space. The performance of VDMOS devices will degrade in high-frequency switching power supplies, degrading the electrical parameters, decreasing the reliability, and causing even the function to fail. The change of the parameters not only depends on accumulating dose, but also on the bias condition of devices during irradiation.

Abroad, research on the radiation-hardening performance of VDMOS devices started quite early. In the 1980s, there were published papers on radiation effects about VDMOS devices. The space grade of VDMOS products with higher radiation-hardening performance has also been made abroad, while the most representative one is made by the USA IR Company, which can be subjected to 10^4 Gy(Si) irradiation. Similar research was relatively late in China, and less research on single chip circuits of power or devices has been done, even though we have made some achievements. For example, in 2004, the University of Electronic Science and Technology succeeded in producing radiation-hardening products which are equivalent to some type of devices of the IR Company. The radiation-hardening products have already been put into application. In 2007, they put forward a new structure of a partly longitudinal power MOSFET device which has buried oxygen: the PSOI (partial silicon on insulator) VDMOS[2,3].

In this paper, we have studied the total dose effects and annealing behavior of domestic VDMOS devices under different bias conditions. We also observed the variation of the threshold voltage, breakdown voltage, leakage current, and on-state resistance as a function of accumulating dose and annealing time. The experiment results show that threshold voltage negatively shifts with accumulating dose, but the value of shifts is within the prescriptive scope. During annealing, the threshold voltage is recovering. The breakdown voltage decreases a lot with accumulating dose and produces "breakdown variety" during 100 °C annealing. The leakage current has a slight increase; thus, it can be concluded that the problem of leakage current is significantly improved. During irradiation and annealing, the changing of on-state resistance is not significant. The results of our experiments are meaningful and important to further improvements in the design and processing of these kinds of domestic VDMOS devices.

2. Devices and experiments

The experimental samples are bar-gate n-channel VDMOS devices, as shown in Fig. 1, fabricated by the Institute of Microelectronics of the Chinese Academy of Sciences, using radiation-hardening technology. The breakdown sensitive point of testing samples is a PN junction that is located on the connection of the substrate and the P region[4]. The total dose experiment was carried out on a seventy thousand curie ^{60}Co γ

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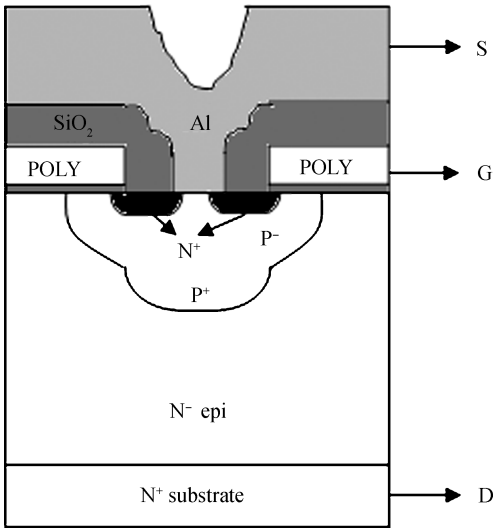

Fig. 1. Cross-section view of VDMOS structure[5].

radiation source. The dose rate was calibrated by a Fricke (ferrous sulfate) dosimeter. The devices were irradiated with ^{60}Co γ rays to a level of 3×10^3 Gy(Si), dose rate 1.01 Gy(Si)/s.

During irradiation and annealing, for 200 V testing samples, there were two bias conditions: #01 $V_{DS} = 160$ V, $V_{GS} = 0$ V; and #02 $V_{DS} = 0$ V, $V_{GS} = 12$ V. For 100 V testing samples, there also were two bias conditions: #03 $V_{DS} = 80$ V, $V_{GS} = 0$ V; and #4 $V_{DS} = 0$ V, $V_{GS} = 12$ V. Before and after irradiation, the threshold voltage, breakdown voltage, leakage current, and on-state resistance were measured by an HP 4142B semiconductor parametric analyzer.

We performed both total dose experiments and annealing experiments on domestic n-channel VDMOS devices. Firstly, the samples were irradiated at room temperature (25 °C) with ^{60}Co γ rays to a level of 3×10^3 Gy(Si) under dose rate 1.01×10^{-1} Gy(Si)/s. Then these irradiated samples were subjected to an annealing experiment for 24 h at 25 °C, following another 50% irradiation to a total dose of 1.5×10^3 Gy(Si) at the same dose rate. After that, they were left in an environmental chamber at 100 °C under the same bias condition with irradiation for 168 h. During irradiation and annealing, the electrical parameters were measured within 20 min.

3. Results and discussion

3.1. Experimental results

Figures 2 and 3 show the threshold voltage shift of the domestic n-channel VDMOS devices with different bias conditions as a function of total dose and annealing time respectively. The threshold voltage decreases with increasing total dose, as shown in Fig. 2. After annealing for 168 h at 100 °C it has almost recovered to the initial value. Similarly, we can also find the same results in Fig. 3. However, during 25 °C annealing, the threshold voltage of the sample #03 under the 80 V gate bias does not recover, but continues to shift negatively. At the beginning of 100 °C annealing, the threshold voltages of samples #02 and #04 do not recover immediately, but shift to a worse direction and then are gradually restored eventually.

Figures 4 and 5 show the breakdown voltage of the domestic n-channel VDMOS devices with conditions as a function of total dose and annealing time respectively. As can be seen from

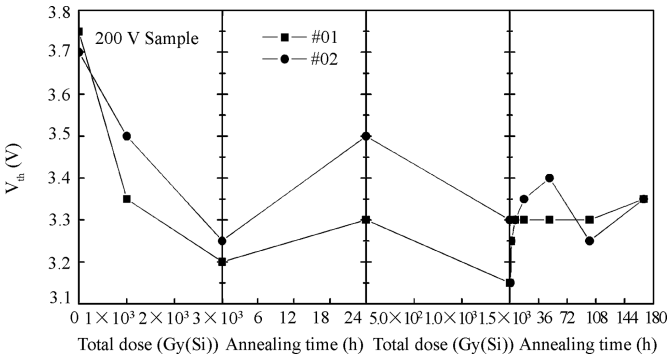

Fig. 2. Threshold voltage of devices #01, #02 versus total dose and annealing time.

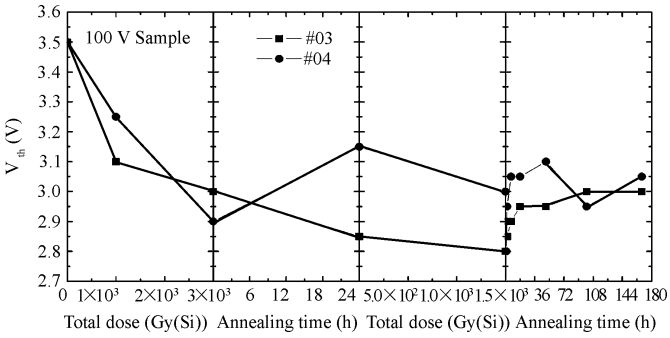

Fig. 3. Threshold voltage of devices #03, #04 versus total dose and annealing time.

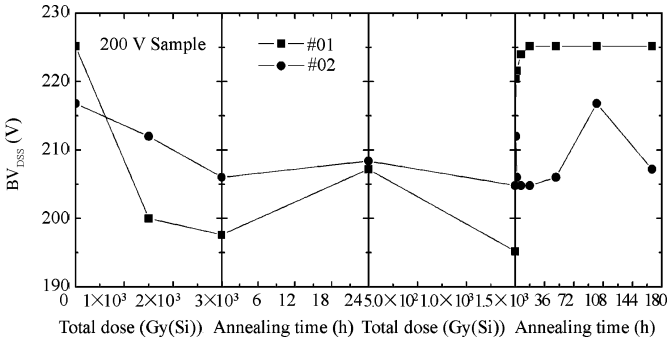

Fig. 4. Breakdown voltage of devices #01, #02 versus total dose and annealing time.

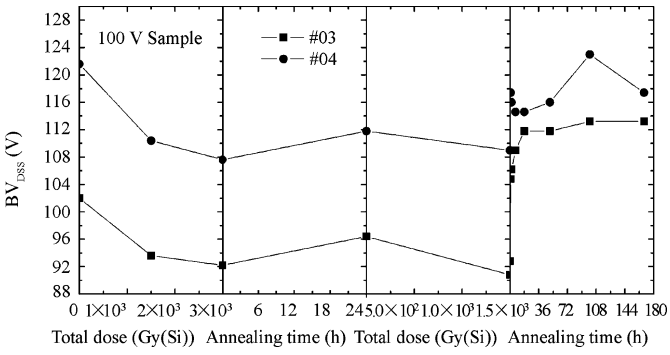

Fig. 5. Breakdown voltage of devices #03, #04 versus total dose and annealing time.

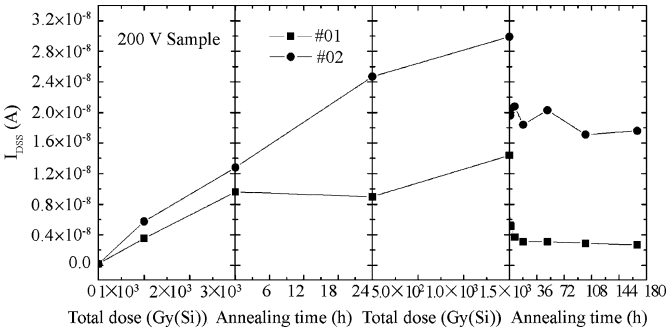

Fig. 6. Drain current of devices #01, #02 versus total dose and annealing time.

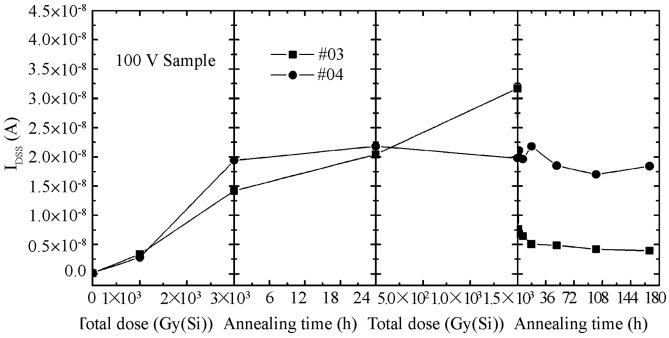

Fig. 7. Leakage current of devices #03, #04 versus total dose and annealing time.

Figs. 4 and 5, the breakdown voltage decreases with increasing total dose and it shows various extents of recovery after annealing. But under high bias voltage during 100 °C annealing, the breakdown voltage represents a so-called "breakdown variety" phenomenon. This kind of phenomenon is obvious, particularly in the #03 sample.

Figures 6 and 7 show the curves of leakage current versus total dose and annealing time at different temperatures. The leakage current increases with the increase of total dose. The VDMOS devices show various extents of latent damage during 25 °C annealing and recover very easily during 100 °C annealing. Thus, it suggests that the problems of leakage current have been significantly improved. The changing of on-state resistance is not obvious during irradiation and annealing, as shown in Fig. 8.

3.2. Discussion

The threshold voltage shift of domestic n-channel VDMOS devices results from the creation of both oxide-trapped charges and interface traps during irradiation[4], as Figures 2 and 3 show. The threshold voltage shift can be expressed as:

$$\Delta V_{\mathrm{T}} = \Delta Q_{\mathrm{ot}}/C_{\mathrm{ox}} + \Delta Q_{\mathrm{it}}/C_{\mathrm{ox}} = \Delta V_{\mathrm{ot}} + \Delta V_{\mathrm{it}}, \quad (1)$$

where ΔV_{T} is the overall threshold voltage shift with respect to the pre-irradiation value, ΔV_{ot} is the voltage shift induced by oxide-trapped charges (electrons and holes), and ΔV_{it} is the voltage shift induced by interface trap generation.

Because the oxide layer is thick, the quantities of accumulated positive oxide-trapped charges are much greater. Thus, compared with interface traps, the oxide-trapped charges have

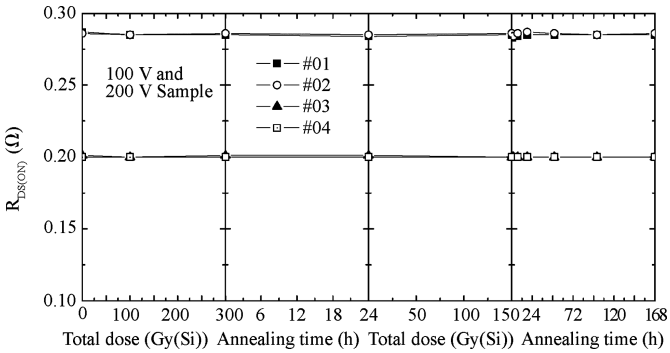

Fig. 8. On-state resistance of devices #01, #02, #03 and #04 versus total dose and annealing time.

a greater influence on breakdown voltage, and they will induce continuous negative threshold voltage shift in VDMOS devices during irradiation. During annealing (25 °C and 100 °C) the threshold voltage shows various extents of recovery due to the annealing of trapped holes. As we know, there are two models of radiation-induced trapped hole annealing: one is the tunneling model and the other is the thermal emission model. The tunneling model is very weakly temperature dependent, and is not able to explain the large effect of temperature on trapped hole annealing observed for some samples, for instance, VDMOS samples. However, compared with the tunneling model, the thermal emission is strongly temperature dependent and can accurately account for the observed thermal effects[4]. In our experiment, the bias conditions of VDMOS devices during annealing are not changed, while the temperature is changed between 25 and 100 °C. Therefore, we use the thermal emission model to explain the annealing of radiation-induced trapped holes in this article. It is based on the thermal emission of holes from traps which are distributed in energy in the oxide. From this model we also know that the annealing process of radiation-induced trapped holes is the thermal emission from hole-traps in the oxide to the valence band of the oxide. The emission probability of the thermal holes into the valence band of the oxide depends exponentially on the energy from the trap to SiO_2 valence band. From previous discussion[4], we know that $\Phi_{\mathrm{m}}(t)$ can be expressed as

$$\Phi_{\mathrm{m}}(t) = kT/q \ln AT^2 t, \quad (2)$$

where q is the electron charge, k is Boltzmann's constant, T is the absolute temperature, and A is a parameter which depends on the capture cross section of the trap and other physical parameters. During annealing, at any time holes which are closer to the valence band than $\Phi_{\mathrm{m}}(t)$ have already been emitted, while holes which are farther from the valence band than $\Phi_{\mathrm{m}}(t)$ still remain[6]. During 25 °C annealing, the energy of metastable state trapped holes of the shallow energy level is lower than Φ_{m}, causing the thermal emission of holes from traps in the oxide to the valence band of the oxide. When the holes are in the valence band, they migrate to the interface and into the silicon substrate, thereby leading to the recovery of threshold voltage. Meanwhile, due to the high energy, the trapped holes in the deep energy level will also be trapped. During 100 °C annealing, Φ_{m} increases with temperature，inducing the energy of the trapped holes in the deep energy level to be lower than

Φ_m. Thus, the radiation-induced trapped holes in the deep energy level continue to anneal because of the effect of thermal activation. The threshold voltage continues to recover during 100 °C annealing.

The threshold voltage does not recover at the beginning of 100 °C annealing and continues to decrease. We think that the primary factor in the changing of the threshold voltage is temperature. We know from Refs. [7, 8] that with the increase of temperature the threshold voltage reduces gradually. At the beginning of 100 °C annealing, the threshold voltage decreases because the temperature rises suddenly. The threshold voltage later recovers due to oxide positive charge annealing.

During 100 °C annealing, the threshold voltage alters suddenly from peak to bottom and later increases slowly (see Figs. 2 and 3), while the bias is kept at $V_{GS} = 12$ V. We think that it is caused by LITB[9−11]. With the increase of annealing time the interface trapped charges increase sharply and then decrease slowly. The temperature strongly affects LITB and at 25 °C the LITB is suppressed. Latent interface-trap buildup is a large sudden increase in interface traps during past-irradiation annealing. Radiation-induced interface traps have been extensively investigated, and several models have been proposed to explain their conventional generation. In this paper, we use the H-W model for latent interface-trap buildup[10, 11]. From this model, we know that the H_2 in structures adjacent to the gate oxide releases and diffuses to the gate oxide. H_2 is cracked at the positive charge centers (CC^+) in the oxide, in which H^+ is released.

$$H_2 + CC^+ \rightarrow CC\text{–}H + H^+. \quad (3)$$

According to previous investigations[11], we can know that the cracking reaction is very slow and that the most probable candidates for CC are the oxygen related hole traps, and not the E' centers. The cracking reaction could contribute to the rate of ΔN_{it} increase, once H_2 reaches the vicinity of the Si–SiO_2 interface, where the majority of charge centers CC^+ are located. Finally, under positive bias H^+ drifts to the Si–SiO_2 interface to form an interface trap and H_2.

$$\equiv Si_s\text{–}H + H^+ + e^- \rightarrow \equiv Si_s^{\cdot} + H_2. \quad (4)$$

H_2 diffuses back into the bulk of the oxide, where it is cracked at the remaining charge centers CC^+, and there is a repetitive sequence of H_2 cracking, H^+ drift and interface-trap formation reactions. Positive V_{GS} increases the number of H^+ reaching the interface and the probability for obtaining the electron from Si in reaction (4), and thus enhances the ΔN_{it} increase. We know also that room temperature "freezes" the changes in ΔN_{ot} and ΔN_{it}. However, LITB is observed several hours after the temperature is elevated. It confirms that the latent interface-trap generation is strongly thermally activated. We can also see the same results from Figs. 4 and 5; the breakdown voltage has suddenly increased at the beginning of 100 °C annealing and then decreased smoothly under $V_{GS} = 12$ V bias voltage.

From Figs. 4 and 5 we know the relationships between the breakdown voltage and total dose and annealing time. The breakdown voltage is one of the most important electrical parameters of VDMOS devices, and it represents the voltage tolerance ability of VDMOS devices. The breakdown voltage of these types of domestic VDMOS devices is a sensitive parameter, as emphasized in Ref. [5]. Also, while checking the performance of breakdown voltage, we should choose to irradiate under the drain bias condition. From Ref. [8], we have also known that the charges have more influence on the breakdown voltage of VDMOS devices which have a field limiting ring. During irradiation, the threshold voltage gradually drops with accumulating dose. We think that the primary reason is positive charge buildup in the surface on the N type substrate, producing induced charges between the main and ring junctions. Finally, the electric field of the P point increases[8], which leads to the voltage increasing between the main and ring junctions. The positive charges in the surface on the N type substrate cause the increase of the biggest electric field intensity and decrement of breakdown voltage.

During 100 °C annealing, the breakdown voltage recovers under the gate bias voltage, but when the annealing time is more than about 7 h it may pass through the pre-irradiation threshold voltage, behaving with a "rebound" effect. The rebound effect is of great practical concern for space environments because components are typically exposed to relatively low dose rates for very long mission lifetimes. We think that it is the so-called "breakdown variety". For example, the initial value of breakdown voltage of the sample #03 is 102 V and after 100 °C annealing it becomes 113 V, which can be seen in Fig. 5. The reason for this breakdown variation is that when the PN junction is in the state of avalanche breakdown, the carriers in the surface barrier can obtain abundant energy under strong electric field and become hot carriers, the energy of which is higher than that of room temperature. The holes can be injected into the Si–SiO_2 interface traps under the electric field, making the width of the barrier layer in the P region wider and the breakdown voltage higher. After breakdown, a large number of hot electron-hole pairs are produced again, which can further modulate the conductance of the P exhaust layer again, making the exhaust layer wider and the breakdown voltage higher again. During 100 °C annealing, on the one hand, the breakdown voltage recovers because of the annealing of oxide positive charges. On the other hand, the increasing of the interface traps near the Si/SiO_2 interface induces the increase of holes injected into interface traps because of the function of the electric field[6]. Finally, the value of the threshold voltage passes through the pre-irradiation threshold voltage.

As can be seen from Figs. 6 and 7, the variation of leakage current is within the prescriptive scope. It is concluded that the changing of leakage current is suppressed by the improvement of the device design and processing. But the leakage current under different bias voltages shows latent damage during 25 °C annealing. As seen from Fig. 8, the on-state resistance of domestic VDMOS devices under different bias voltages almost remains constant during irradiation and annealing.

4. Conclusions

We have studied the total dose effects and annealing behavior of domestic n-channel VDMOS devices. The results of our experiments are meaningful and important to further improvements in the device design and processing.

(1) The threshold voltage negatively shifts with accumulating dose during irradiation and continues to decrease at the

beginning of the high temperature annealing.

(2) During 100 °C annealing, under the drain bias voltage the breakdown voltage of this kind of domestic n-channel VDMOS device has recovered beyond the pre-irradiation voltage.

(3) During 100 °C annealing, under the gate bias voltage, the LITB phenomenon appears.

(4) Due to the improvement of technology and design, the leakage current of this kind of domestic VDMOS device is suppressed and on-state resistance is little changed during irradiation and annealing.

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