A 2.5-Gb/s fully-integrated, low-power clock and recovery circuit in 0.18-μm CMOS*

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Abstract: Based on the devised system-level design methodology, a 2.5-Gb/s monolithic bang-bang phase-locked clock and data recovery (CDR) circuit has been designed and fabricated in SMIC's 0.18-μm CMOS technology. The Pottbäcker phase frequency detector and a differential 4-stage inductorless ring VCO are adopted, where an additional current source is added to the VCO cell to improve the linearity of the VCO characteristic. The CDR has an active area of 340×440 μm^2, and consumes a power of only about 60 mW from a 1.8 V supply voltage, with an input sensitivity of less than 25 mV, and an output single-ended swing of more than 300 mV. It has a pull-in range of 800 MHz, and a phase noise of –111.54 dBc/Hz at 10 kHz offset. The CDR works reliably at any input data rate between 1.8 Gb/s and 2.6 Gb/s without any need for reference clock, off-chip tuning, or external components.

Key words: clock and data recovery; phase frequency detector; voltage-controlled oscillator; bang-bang; jitter

DOI: 10.1088/1674-4926/31/3/035007 **EEACC:** 1265

1. Introduction

With greater and greater demands on high-volume data transmission, more and more attention is being paid to both high-speed long-haul serial optical communications and short-haul parallel optical interconnections, which are gaining rapid development. In all communication systems, a clock and data recovery (CDR) circuit is a pivotal building block.

Owing to the diversity of the application environment and demands, the rapid development of IC fabrication processes, mainly CMOS, and the advancement of design techniques, various kinds of CDR have been emerging. However, by and large, continuous-mode CDRs can be classified into three groups[1]: filter-type[3–5], PLL-based[6–12], and phase-picking[13].

Among these, the PLL-based CDR, also called the tracking-type CDR, has been in wide use for gigabit data rates, because it has many advantages[14], such as low power, high integration, and automatic phase alignment.

This paper discusses the design and fabrication of a 2.5 Gb/s monolithic PLL-based CDR in SMIC's 0.18-μm CMOS technology. The system-level and circuit-level design methods are analyzed firstly. The measurement results are then given.

2. System-level design

Basically, the core of the CDR circuit comprises a phase detector (PD), a voltage to current conversion (V/I) circuit, a loop filter (LF), and a VCO[16]. Among these, the choice of the PD has a critical effect on the system structure, jitter characteristics, CDR design procedure, the phase alignment precision, even the means of data recovery (DR), and so on.

There exist two basic types of PD: bang-bang (binary, or early/late) versus linear. In contrast to their linear counterparts, bang-bang PDs have the unique advantages[14, 16–18] of inherent sampling phase alignment, adaptability to multi-phase sampling structures, operating at the highest speed at which a process can make a working flip-flop, avoiding the use of charge pumps owing to high gain, and so on, so a bang-bang PD is employed in this CDR, as shown in Fig. 1.

Unlike a linear PD which detects both the magnitude and the direction of the phase error, a bang-bang PD detects the direction only, so the classical linear control theory cannot be directly applied. Fortunately, due to realistic effects such as metastability and input jitter, the ideally binary characteristic of BBPDs in practice exhibits a finite slope across a narrow range of the input phase difference, where the slope rate, that is, the effective gain of the PD, is inversely proportional to input jitter amplitude[16, 18, 19]. Figure 1(a) indicates these effects on the bang-bang PD. Thus, small phase errors lead to linear operation whereas large phase errors introduce "slewing" in the loop[16].

For the sake of compactness, the topology[16, 20, 21] where the "bang-bang branch (proportional branch)" and "integral branch" are implicitly combined is chosen over the one[14, 17, 22] where a separate direct-drive path from the PD to the VCO is used.

As for the system-level design of a CDR, four jitter specifications[2, 11] are usually focused on: jitter transfer (JTRAN), jitter peaking (JPEAK), jitter tolerance (JTOL), and jitter generation (JGEN). According to Fig. 1(b), based on the large-signal piecewise-linear model of the bang-bang PD and relevant theories[16–18, 20–22], some analytical equations are derived to estimate JTRAN, JTOL, JGEN, as follows:

$$\mathrm{BW_{JTRAN}} \propto \Delta F_{\mathrm{bb}} \times \mathrm{DF}/\mathrm{JITTER_{PP}}, \quad (1)$$

$$\mathrm{BW_{JTOL}} \propto \Delta F_{\mathrm{bb}} \times \mathrm{DF}, \quad (2)$$

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z2a5) and the National Natural Science Foundation of China (No. 60806027).

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Received 7 September 2009, revised manuscript received 27 October 2009

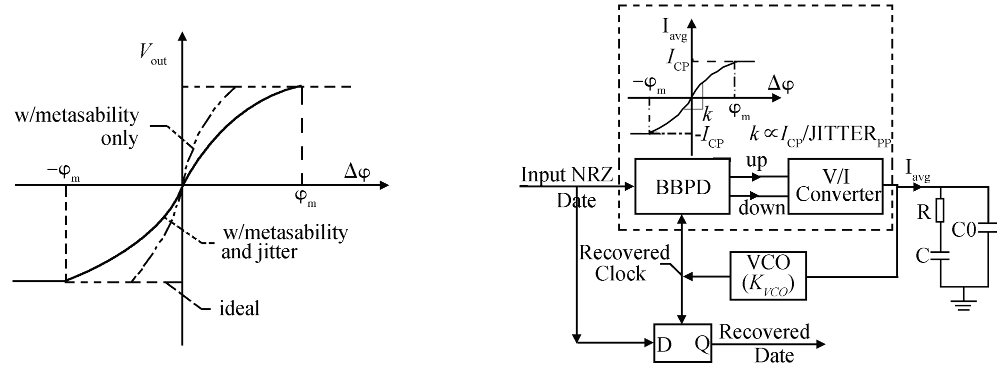


Fig. 1. (a) Phase transfer characteristic of a bang-bang PD that exhibits metastability and input jitter. (b) Basic bang-bang CDR architecture.

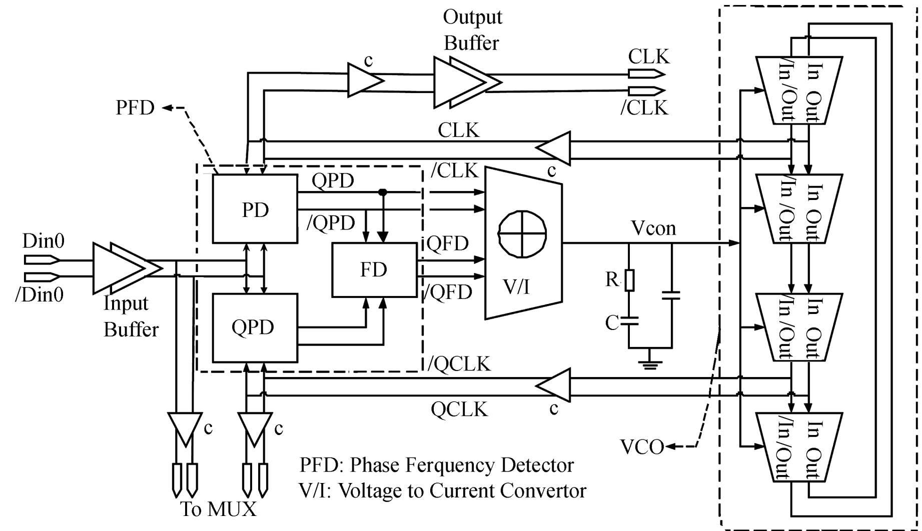


Fig. 2. Circuit block diagram of the adopted bang-bang CDR.

$$\mathrm{JG_{PP}} \propto m \times \Delta F_{\mathrm{bb}}, \quad (3)$$

$$\Delta F_{\mathrm{bb}} = I_{\mathrm{CP}} \times R \times K_{\mathrm{VCO}}, \quad (4)$$

$$\zeta \propto R \times C/m, \quad (5)$$

where $\mathrm{BW_{JTRAN}}$ is the closed-loop JTRAN bandwidth, $\mathrm{BW_{JTOL}}$ is the JTOL bandwidth, $\mathrm{JG_{PP}}$ is the peak-to-peak jitter generation, ΔF_{bb} is the bang-bang frequency step, ζ is the loop stability factor, $\mathrm{JITTER_{PP}}$ is the peak-to-peak input data jitter, DF is the transition density factor (0.5 for random data), m is the number of bit periods of latency around the loop, I_{CP} is the saturated current of the V/I converter, K_{VCO} is the VCO gain, R is the loop-filter resistor, and C is the loop-filter capacitor.

The desired overall target is as follows: low JTRAN bandwidth; small JPEAK; high JTOL bandwidth; and low JGEN[11]. So, from Eqs. (1)–(3), it can be found that a subtle trade-off between $\mathrm{BW_{JTRAN}}$, $\mathrm{BW_{JTOL}}$ and $\mathrm{JG_{PP}}$ must exist in determining ΔF_{bb}. For example, a larger ΔF_{bb} can improve the jitter tolerance but at the cost of degraded output jitter performance due to the increase of transferred and generated jitter.

As for JPEAK, it has been proven that the jitter transfer of bang-bang slew-limited CDR loops exhibits negligible peaking[16]. To ensure that the loop JTRAN function does not exhibit peaking, ζ should be made large enough so that the proportional loop dominates during slew limiting (slope overload)[22].

According to Eqs. (3) and (5), m should made as small as possible, because smaller latency, m, results in smaller jitter generation and enhances the stability of the loop. It also means that a ring VCO is preferable in the bang-bang CDR as compared to an LC VCO where the tuning delay is larger due to the usually higher Q-factor of the LC-tank[14, 18].

Additionally, owing to the narrow loop bandwidth, the capture range of a CDR does not usually exceed a few percent of the data rate, which cannot guarantee that the loop comes to lock without any aid under PVT variations[2]. So, some aided acquisition measures[8, 11, 20] must be employed, otherwise manual off-chip tuning[18, 22] is needed.

3. Circuit-level design

As shown in Fig. 2, a digital frequency and phase detector, known as a digital quadratic-correlator, is employed, which can make the loop have a small loop bandwidth, a wide pull-in range, and operate without the need for a local reference clock and off-chip tuning[2,12].

However, the PFD requires I/Q clocks. Mainly,

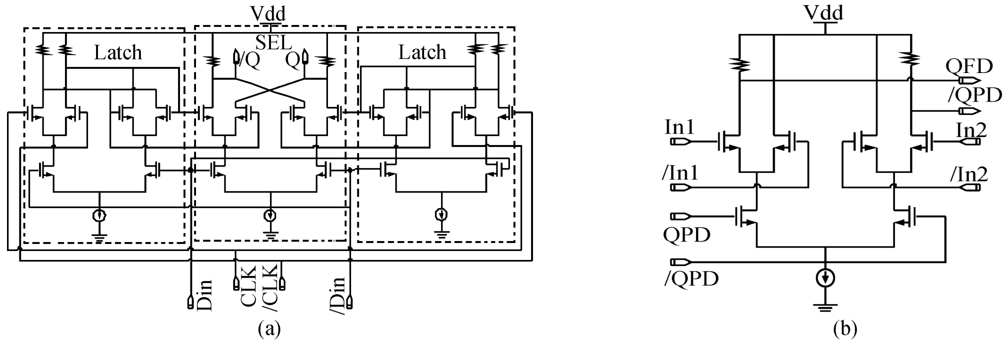


Fig. 3. Circuit diagram of (a) the PD and (b) tri-state selector.

there exist five methods to generate a quadrature clock[4, 8–10, 12, 15, 20, 22]: (1) VCO with a $\pi/2$ delay line; (2) Combination of VCO, polyphase-filter (or R–C C–R filter), and output (or limiters); (3) VCO at double frequency followed by /2 divider; (4) two cross-coupled LC VCOs; and (5) even-stage ring-like VCO. As a trade-off[15] between power consumption, area, operation frequency range, I/Q phase precision, phase noise, and so on, an even-stage inductorless ring VCO is selected.

At startup, the input data are compared with two I/Q clock signals, respectively, to produce two beat notes, which then are processed by the FD to deliver a frequency error signal. The generated error signal drives the VCO frequency towards the input data, relinquishing the control to the PD when the frequency error is sufficiently small. The PD then locks the VCO rise edge to the input data edge, and the VCO's down edge is used to retime the data in its center. In this circuit, the retiming is completed in a multiplexer (MUX).

3.1. Phase/frequency detector (PFD)[12]

It can be seen in Fig. 2 that the PFD is composed of a PD, a QPD and an FD. In fact, the PD, identical to the QPD, shown in Fig. 3(a), is a double-edge-triggered flip-flop (DETFF), which consists of two CML latches and a selector. The DETFF is chosen over a conventional DFF, because it can make use of both edges of the input data to offer more phase error correction information and improve the performance of the loop. The only difference in the FD compared to the PD is the selector which, as shown in Fig. 3(b), is modified to offer a ternary output.

When the frequency acquisition is completed, the FD remains in the third state in which both outputs are high-state. In this manner, the control of the FD over the loop is handed over to the PD, and then the track stage begins.

Another strong point of the PFD is that it can tolerate up to ±45° I/Q match error[12], which reduces the requirements on the VCO and raises the robustness of the CDR.

3.2. VCO

As indicated in Fig. 2, a 4-stage inductorless ring VCO is adopted to generate the desired I/Q clocks. Due to the wider loop bandwidth, an inferior phase noise performance can be tolerated, and its inherent wider tuning bandwidth is desired by the bang-bang CDR.

Figure 4 shows a VCO cell in which a current-folding technique is used to alleviate the conflict between the voltage head-

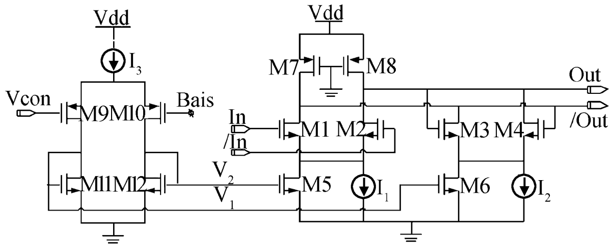


Fig. 4. Circuit diagram of the VCO cell.

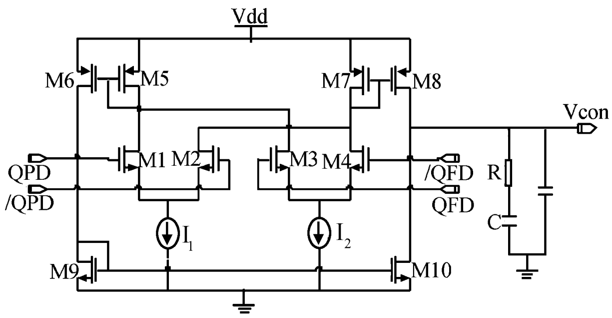
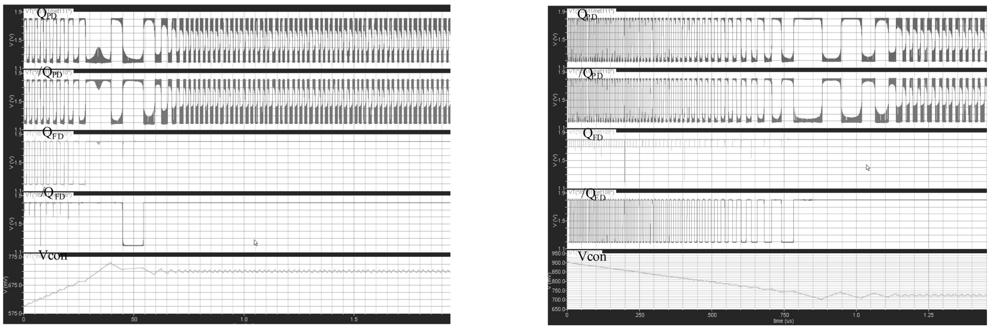


Fig. 5. Circuit diagram of V/I converter and loop filter.

room and the sensitivity of the VCO[2]. The terminal (Vcon) controls the delay of the cell, then the frequency of the VCO, by tuning the intensity of the cross-coupled transistor pair (M3 and M4). PMOS transistors, instead of resistors, are used as the loads, because the latter are hard to precisely control during fabrication. V_1 and V_2 differentially control the currents flowing through the differential pair (M1 and M2) and the cross-coupled transistor pair (M3 and M4) by M5 and M6, respectively, so the total current through loads (M7 and M8) almost remains constant, and then the output voltage swing suffers from less variation across the tuning range. Two current sources (I_1 and I_2) are added to prevent ceasing of the oscillation and improve the linearity of the VCO characteristic, respectively. In fact, the gate lengths of transistors such as M3, M4, M6, M9, M11 and M12 are finely lengthened for the sake of tuning linearity.

There are two reasons why a differential topology is adopted: one is the requirement for differential circuits throughout the CDR and the various advantages they have; another is the better duty cycle they can produce compared to a single-ended one, where the duty cycle has a critical effect on



(a) (b)

Fig. 6. Some characteristic simulation waveforms for the CDR. (a) $f_{\rm int}$ < 2.5 GHz. (b) $f_{\rm int}$ > 2.5 GHz.

the performance of the CDR.

3.3. V/I converter and loop filter (LF)

Figure 5 shows the implementation of the V/I converter and loop filter. Actually, the V/I converter is an adder with a single-ended high-impedance output, where both the phase error signal and the frequency error signal from the PD and the FD are applied to two input ports, respectively, and an output signal is generated to tune the VCO by the loop filter. In order to reduce the channel-length modulation of M8 and M10, both the gate lengths and widths of the transistors are increased to minimize these effects.

The loop filter is entirely passive, consisting only of resistors and capacitors. The inherent low phase offset from the high gain of the bang-bang PD allows this simple filter, which consumes less power and provides better loop stability, since no higher order poles exist, as when an op-amp is used[6].

Due to the low capacitance density of the MIM capacitor of less than 1 pF/μm^2, NMOS transistors, about 8 pF/μm^2, are used as capacitors, especially for the large capacitor C, shown in Fig. 5.

4. Simulation analysis

Figure 6 shows some characteristic simulation waveforms for the CDR when $f_{\rm int}$ < 2.5 GHz and $f_{\rm int}$ > 2.5 GHz ($f_{\rm int}$ is the initial frequency of the VCO). In both Figs. 6(a) and 6(b), and referring to Fig. 2, it can be seen that the top two waveforms ($Q_{\rm PD}$ and /$Q_{\rm PD}$) are the PD output; the third and fourth ($Q_{\rm FD}$ and /$Q_{\rm FD}$) are the FD output; the bottom one is the tuning voltage of the VCO.

According to Fig. 6, just as mentioned in the above sections, during the acquisition stage the FD works, and during the tracking stage both the FD outputs ($Q_{\rm FD}$ and /$Q_{\rm FD}$) remain high when only the PD operates.

5. Experimental results

The chip was designed and fabricated in SMIC 0.18 μm CMOS technology. As shown in Fig. 7, the whole IC occupies an area of 670 × 760 μm^2, with a CDR core area of 340 × 440 μm^2.

The performance of the CDR was evaluated on-wafer by a Cascade probe station. Mainly, an Advantest D3186 pulse pattern generator, an Agilent 86100A Infinium DCA wide-bandwidth oscilloscope, and an E4440a digital spectrum analyzer were employed.

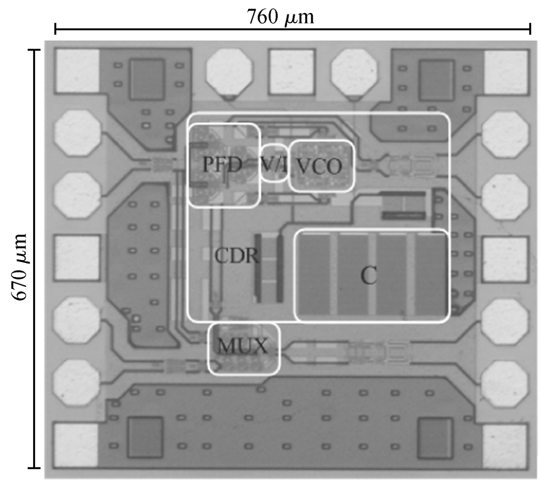


Fig. 7. Chip photograph of the whole IC.

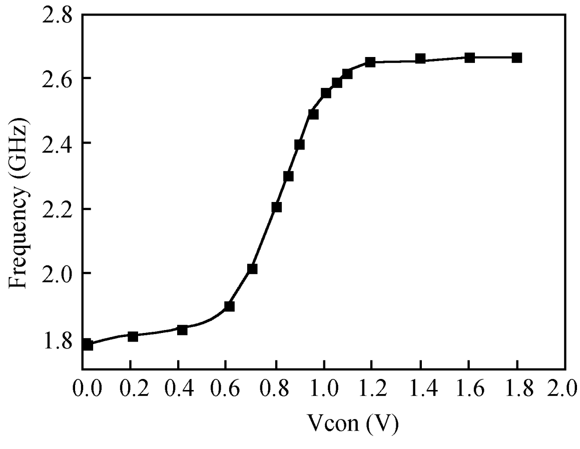
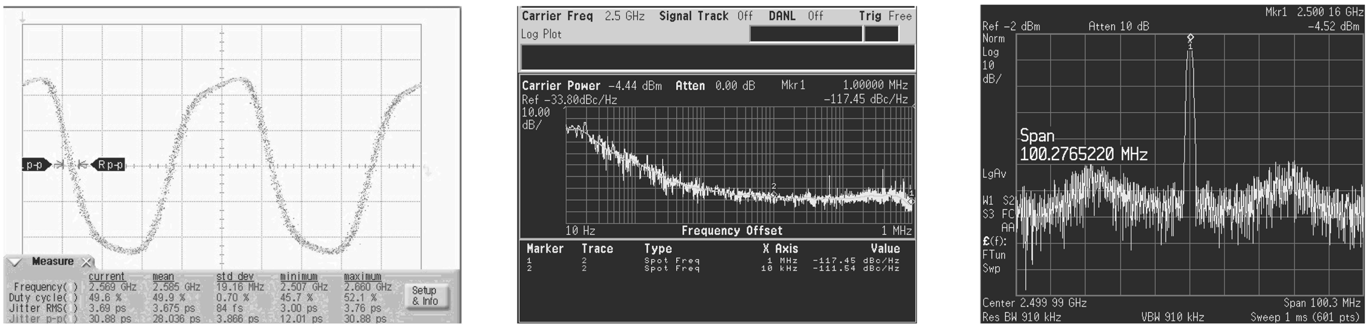


Fig. 8. Measured VCO tuning characteristic curve.

Figure 8 depicts the measured VCO tuning characteristic curve. The VCO achieves a tuning range of more than 800 MHz (> 32%). Although, due to parasitics and imprecise device models, the measured mid-frequency is about 400 MHz lower than predicted by simulation, the desired 2.5 GHz is included in the range all the same.

Figure 9 shows the measured waveform, phase noise, and



(a) (b) (c)

Fig. 9. Measured (a) waveform, (b) phase noise, and (c) spectrum of the 2.5 GHz recovered clock.

Table 1. Performance comparison of previously published 2.5 Gb/s CDRs.

Parameter	This work	Ref. [8]	Ref. [9]	Ref. [5]	Ref. [10]	Ref. [7]
Process	0.18-μm CMOS	0.18-μm CMOS	0.25-μm CMOS	0.25-μm CMOS	0.18-μm CMOS	Si bipolar
Off-chip capacitor	N	Y	Y	Y	N	Y
Off-chip tuning	N	N	Y	Y	—	N
Reference clock	N	N	N	N	N	Y
P_{diss}(mW)	60	26.1	550	680	120	800
Area (μm^2)	670 × 760	2400 × 2400	970 × 970	1490 × 1000	675 × 875	2500 × 2500
Pull-in range (MHz)	800	220	80	40	250	400
Phase noise (dBc/Hz)	–111.5 @ 10 kHz –117.45 @ 1 MHz	–100 @ 1 MHz	–106 @ 100 kHz	–110 @ 100 kHz	–111 @ 10 kHz	—

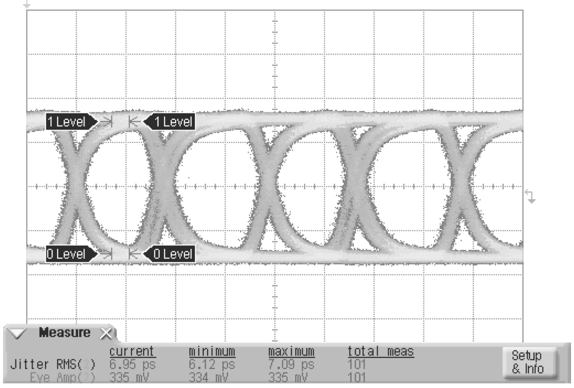


Fig. 10. Measured 5 Gb/s multiplexed eye diagram when two 2.5 Gb/s data streams were applied.

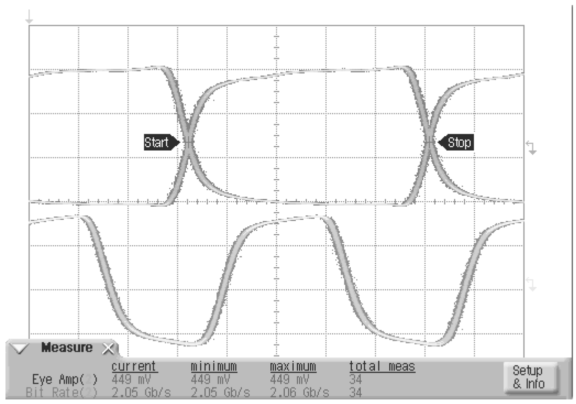


Fig. 11. Measured eye diagrams of recovered clock and data when one 2.0 Gb/s data stream was applied to two input ports at the same time.

spectrum of the 2.5 GHz recovered clock in response to a 2.5 GHz pseudorandom bit sequence (PRBS) of length $2^{31} - 1$, from a 1.8 V supply. From Fig. 9, it can be found that the recovered clock has an RMS jitter of 3.69 ps, a duty cycle of 49.6%, a phase noise of –111.54 dBc/Hz at 10 kHz offset (–117.45 dBc/Hz at 1 MHz offset), and so on.

Figure 10 shows the measured 5 Gb/s multiplexed single-ended eye diagram with an RMS jitter of 6.95 ps when two different 2.5 Gb/s data streams were applied to two input ports of the IC, and the data recovery function was embedded in the MUX. Actually, if a single data stream was applied to both ports at the same time, the MUX could serve as a DR unit, for example, as shown in Fig. 11, in which only one 2.0 Gb/s data stream was applied.

The measurement results show that under a 1.8 V supply, the pull-in range of the CDR is actually limited by the available operating range of the VCO, that is, approximately between 1.8 and 2.6 GHz. In other words, the CDR can work properly with any input data rate between 1.8 and 2.6 Gb/s. Two examples are shown in Figs. 9 and 11.

Under a 1.8 V supply, the whole IC consumes a power of about 112 mW, of which about 53% is taken up by the CDR with relevant buffers. The CDR has an input sensitivity of less than 25 mV, and an output single-ended swing of more than 300 mV. Even when the voltage was reduced to 1.45 V, the CDR could work properly. From the 1.45 V supply, the CDR only consumed 23 mW.

A comparison with results from similar, previously published studies is tabulated in Table 1. According to Table 1, it can be seen that this CDR has a better performance.

6. Conclusions

A system-level design methodology for bang-bang CDRs has been devised from relevant developing design theories and practices. Based on the design methodology, a 2.5 Gb/s monolithic PLL-based bang-bang CDR has been designed and fabricated in SMIC's 0.18-μm CMOS technology.

The circuit choice and principle of the CDR and its building blocks are discussed and analyzed in detail. A Pottbäcker PFD was selected for a wider acquisition range. A differential 4-stage inductorless ring VCO was used, because of its better duty, smaller tuning delay, smaller area cost, and so on. Also, an additional current source was added to the VCO cell to improve the linearity of the VCO characteristic.

The CDR has an active area of 340×440 μm^2, and consumes a power of about 60 mW from a 1.8 V supply voltage, with an input sensitivity of less than 25 mV, and an output single-ended swing of above 300 mV. Actually, the CDR can work properly under a 1.45 V supply, with a power consumption of only about 23 mW.

The CDR works reliably at any input data rate between 1.8 Gb/s and 2.6 Gb/s without any need for a reference clock, off-chip tuning, or external components. It has a phase noise of –111.54 dBc/Hz at 10 kHz offset at 2.5 Gb/s data input.

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