A 2.1–6 GHz SiGe BiCMOS low-noise amplifier design for a multi-mode wideband receiver*

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Abstract: A wideband low-noise amplifier (LNA) with ESD protection for a multi-mode receiver is presented. The LNA is fabricated in a 0.18-μm SiGe BiCMOS process, covering the 2.1 to 6 GHz frequency band. After optimized noise modeling and circuit design, the measured results show that the LNA has a 12 dB gain over the entire bandwidth, the input third intercept point (IIP3) is –8 dBm at 6 GHz, and the noise figure is from 2.3 to 3.8 dB in the operating band. The overall power consumption is 8 mW at 2.5 V voltage supply.

Key words: SiGe; BiCMOS; low- noise-amplifier; wideband; electrostatic discharge
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1. Introduction

Recently, the increasing demand for multi-mode wireless service has made wideband RF systems more popular in modern lives and the consumer electronics market. Wideband receivers will allow a higher data rate and support multiple wireless communication standards. The market interests continuously focus on short-range, multi-standard transceivers which are ultimately developed to cover standards such as wireless local area network (WLAN) 802.11a/b/g, global service mobile (GSM) and wide-band code division multiple access (WCDMA). According to the different operation frequency and crucial requirements on such a wide band, a fully integrated, multi-mode wideband low noise amplifier (LNA) is critical to overall RF frontend performance. The main design metrics in this wideband LNA are noise figure (NF), gain and linearity, of which NF is the most important consideration in our study.

There have been many studies and papers proposed on wideband LNA and ultra wideband (UWB) LNA design, mainly divided into two categories based on process: RFCMOS[1, 2] and SiGe BiCMOS[3–5]. Bipolar transistors have obvious advantages of low noise and high speed, making them particularly suitable for low noise applications. The SiGe process increases the characteristic frequency f_T due to the built-in electric field induced by Ge, resulting in a higher beta value and lower base resistor r_b, which is dominant in overall noise performance.

In this paper we present an LNA to cover from 2.1 up to 6 GHz for multi-mode wideband applications; for the high-end frequency up to 6 GHz, we use a simple equation to estimate a process characteristic frequency by

$$\text{Gain} = f_T/f = 60\ \text{GHz}/6\ \text{GHz} = 10 = 20\ \text{dBV}. \quad (1)$$

So we choose the 60 GHz SiGe heterojunction bipolar transistor (HBT) with a BVCEO of 2 V for LNA design, whose characteristics are quite suitable for low noise application and ensure efficient gain.

2. Noise analysis

To minimize the noise figure in the SiGe BiCMOS LNA, we must study the complex noise mechanism in the SiGe HBT. Firstly, we must set a general noise model for the HBT and analyze its main noise sources contributing to the noise figure. Secondly, the minimum noise figure is dominated by base current density J_b (μA/μm^2), illustrating that an optimum device size, especially emitter width, can decide the noise performance to some extent. So optimal device selection of the HBT and other passive components is discussed afterwards; the purpose is to get a better understanding of the trade-off between best noise performance and other terms such as gain and linearity.

(1) The three main noise sources in the SiGe HBT are shot noise, thermal noise and flicker noise. When the LNA is biased in the active region, collect current mainly generates a shot noise source $\overline{i_c^2}$, base current noise can also be represented by $\overline{i_b^2}$, which has a shot noise part, but base noise is mainly dominated by thermal noise generated by r_b, and flicker noise across the BE junction. The HBT noise can be modeled as Figure 1 shows.

Then we have,

$$\overline{i_c^2} = 2qI_{DC}\Delta f, \quad (2)$$

$$\overline{v_b^2} = 4kTr_b\Delta f, \quad (3)$$

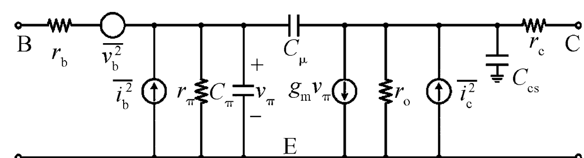

Fig. 1. Noise modeling of the SiGe HBT.

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$$\overline{i_{\rm b}^2} = 2qI_{\rm B}\Delta f + K_1 \frac{I_{\rm B}^{\rm a}}{1+\left[\dfrac{f}{f_{\rm c}}\right]^2}\Delta f. \tag{4}$$

(2) According to the simulation results, we find that the minimum NF is decided by the emitter width (emitter length has a weak relationship with noise performance, but it is a strong function of total gain) and bias current density, or base current density, so the minimum width HBT is selected, and the available maximum gain is obtained by setting an appropriate HBT length. Back to the two-port noise model, the circuit noise figure can be expressed only by the impedance and admittance term, as below[7]:

$$\begin{aligned} \mathrm{NF} &= 1 + \frac{G_{\rm u} + |Y_{\rm c} + Y_{\rm s}|^2 R_{\rm n}}{G_{\rm s}} \\ &= 1 + \frac{G_{\rm u} + \left|(G_{\rm c} + G_{\rm s})^2 + (B_{\rm c} + B_{\rm s})^2\right| R_{\rm n}}{G_{\rm s}}, \end{aligned} \tag{5}$$

where $Y_{\rm c} = G_{\rm c} + {\rm j}B_{\rm c}, Y_{\rm u} = G_{\rm u} + {\rm j}B_{\rm u}$, are part of the noise source admittance, and $Y_{\rm s} = G_{\rm s} + {\rm j}B_{\rm s}$ is the source admittance. We finally have a minimum noise figure as,

$$\mathrm{NF_{min}} = 1 + \frac{n}{\beta_{\rm dc}} + \sqrt{\frac{2I_{\rm c}}{V_{\rm T}}(r_{\rm e} + r_{\rm b})\left(\frac{f^2}{f_{\rm T}^2} + \frac{1}{\beta_{\rm dc}}\right) + \frac{n^2}{\beta_{\rm dc}}}, \tag{6}$$

$$\mathrm{NF_{min}} \propto r_{\rm b}, \quad \mathrm{NF_{min}} \propto I_{\rm c}, \tag{7}$$

$$\mathrm{NF_{min}} \propto \sqrt{(f/f_{\rm T})^2}, \tag{8}$$

So it is clear that NF is a function of the base resistor $r_{\rm b}$, bias current $I_{\rm c}$ which is decided by the base bias current density and characteristic frequency $f_{\rm T}$. NF is proportional to the base resistor and bias current density, and inversely proportional to the characteristic frequency $f_{\rm T}$.

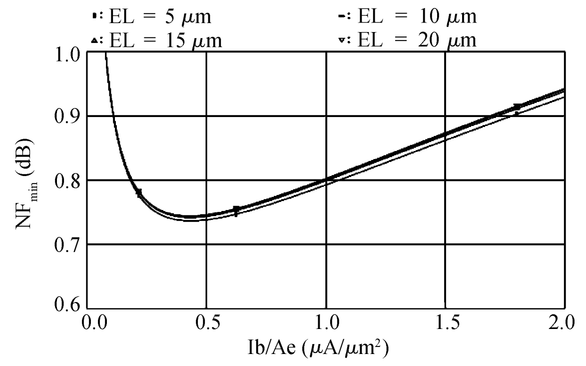

Fig. 2. Minimum NF versus bias current density in the HBT.

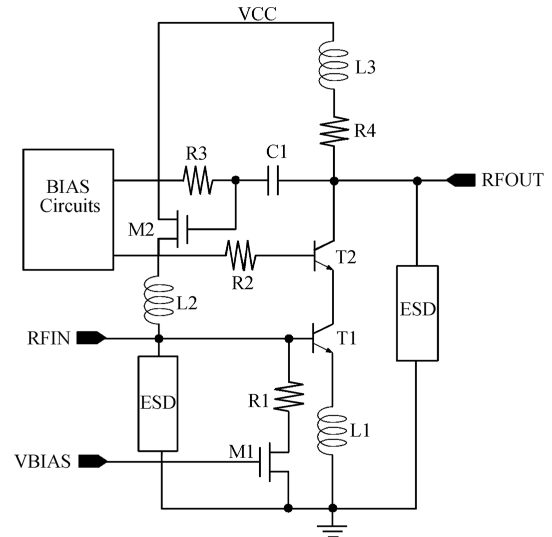

Fig. 3. Simplified schematic of the proposed LNA.

3. Circuit topology

Based on discussions in Section 2, we choose a 60 GHz SiGe HBT of a minimum of 0.24 μm width, which has germanium ejected into the base to help lower the base resistor, lift $f_{\rm T}$ and beta value, finally resulting in a relevant lowest noise figure. The relationship between the minimum noise figure and bias current density is shown in Fig. 2. The HBT gets a minimum NF of about 0.75 dB at 0.5 μA/μm^2 bias current density; the emitter length does not have much impact on the noise figure, so the main amplifying HBT is biased at near this current density.

According to previous work, there are mainly two kinds of SiGe LNA structure selections: common emitter cascade[1, 2, 5] and common base[4].

Common base structure has advantages such as low power dissipation, ease of obtaining input impedance match and saving chip area due to there being no LC matching networks[4], but it is not suitable for lowering NF because the common base amplifier is based on current amplification, collator noise will be totally injected into the signal path, and the NF will rise and cannot adjust satisfactorily.

Traditional common emitter cascade topology using a degeneration inductor can achieve perfect noise matching at narrowband. However, this topology is usually used with resistive feedback to match the input impedance and improve linearity, which will degrade the noise performance to a large extent. Furthermore, based on cancellation of the reactance for a narrow frequency range by using an inductor, traditional topology is not suitable for broadband operation[6].

The proposed broadband LNA in this work without bias circuits is simply shown in Fig. 3. The LNA is a single stage cascade amplifier with ESD protection at both input and output ends.

The feedback is different from normal resistive or capacitive feedback but is a common-drain stage loop, see C1, M2 and L2, which provides another degree of freedom in the design and adjusts the input impedance over a wide band. The real part of the input impedance can be approximated by

$$Z_{\rm in,\,real} = \frac{1}{g_{\rm m2}(1 + \beta_1 Z_{\rm load,\,real})}, \tag{9}$$

where $g_{\rm m2}$ is the transconductance of feedback MOSFET M2, which is a frequency-invariant term, $Z_{\rm load}$ is load impedance, including L3 and R4. The LNA has a traditional common-emitter source amplifying stage with a resistive load, see R4, the L3 is added to bring an inductive term at load, used to broaden the bandwidth and achieve better output matching. The inductor L2 in the feedback path is utilized to achieve a flat

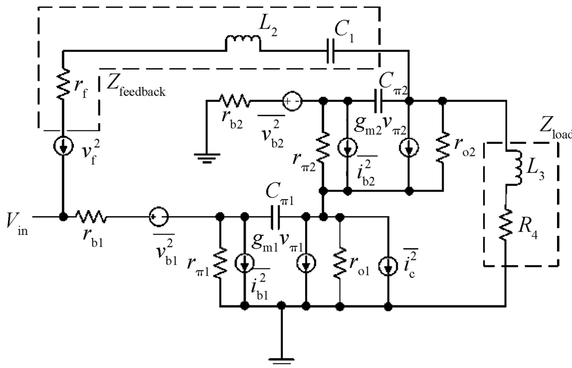

Fig. 4. Small-signal noise model of the proposed LNA.

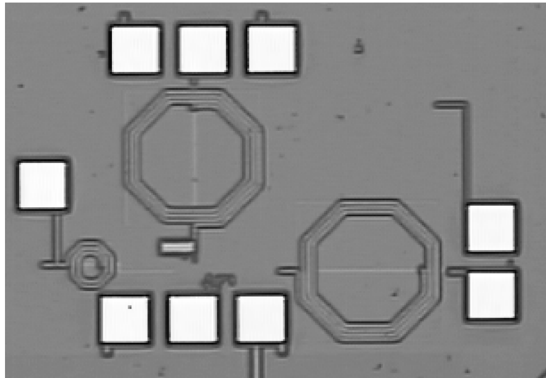

Fig. 5. Chip photograph.

frequency impedance response, and in this way, better noise performance can be obtained at the same time.

Because the most important design target in circuit design is to minimize the noise figure, to fulfill this purpose, a small-signal noise model of the proposed LNA is drawn in Fig. 4; the noise figure is dominated by the noise from the input transistor T1 and will be lowered if β_1 is increased. According to Eqs. (2)–(4), the primary noise sources determining the overall LNA NF are input base-current shot noise $\overline{i_{b1}^2}$, collector- current shot noise $\overline{i_c^2}$ (same collector current), input base resistance thermal noise $\overline{v_{b1}^2}$ and feedback resistance thermal noise $\overline{v_f^2}$.

According to these analyses, we rewrite Eq. (8) below:

$$\mathrm{NF}_{\min} = 1 + \frac{n}{\beta_1} + \sqrt{\frac{2I_c}{V_T}(r_e + r_b)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_1}\right) + \frac{n^2}{\beta_1}}. \quad (10)$$

So after careful HBT device modeling and simulation, the base resistor r_b, bias current I_c and β_1 are obtained by appropriate device selection and current bias. We find that the parasitic term accompanied by increasing device size reduces the bandwidth rapidly; to solve this trade-off, the input stage is biased at 3.2 mA to get the best base current density for noise performance.

4. Experimental results

The presented LNA is implemented in 0.18 μm SiGe BiCMOS technology, which features an up to 60 GHz SiGe HBT. The minimum lithography is 180 nm and substrate resistivity is 16 Ω·cm. The LNA is fabricated and tested on a bare die.

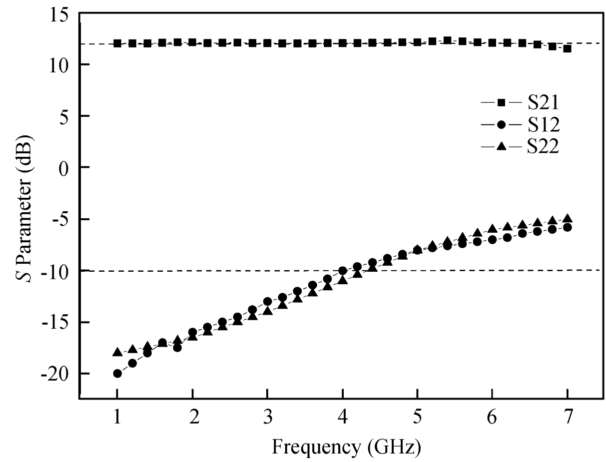

Fig. 6. Measured S parameters.

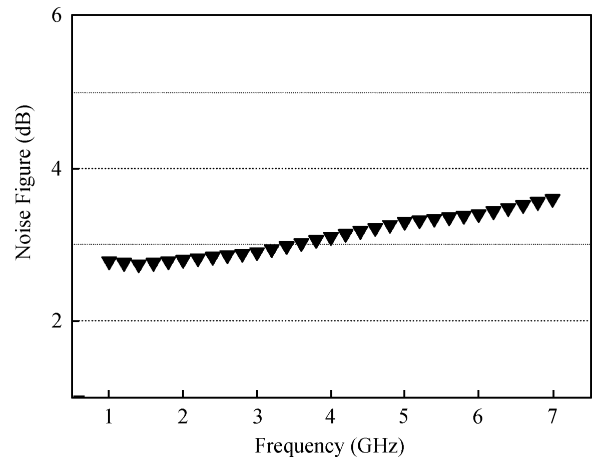

Fig. 7. Noise performance.

Figure 5 shows the die photograph; we add the necessary ESD protection circuits to both RF signal ends and power ends.

The total occupied size is 550 × 850 μm^2, the RF signal is on-chip probed by a GSG structure, and the measurements are performed with an Agilent 40 GHz vector network analyzer 8722D and a spectrum analyzer E4440A. DC power supply is 2.5 V, bias current is 3.2 mA. The measured S parameters from the 2.1 to 6 GHz band are shown in Fig. 6 and the NF measurement results are displayed in Fig. 7. The measured input third intercept point (IIP3) at 6 GHz is about −8 dBm using a two-tone test using 200 MHz spacing, as shown in Fig. 8.

It can be seen that the S_{21} of the LNA all around the 2.1–6 GHz band has almost reached above 12 dB. At 6 GHz the gain drops by as much as 1 dB because of the parasitic increase. As can be seen, the bandwidth is higher than 6 GHz. The S_{11} and S_{22} are all below −10 dB when the frequency is lower than 4 GHz, but obviously degradation shows up on input return loss and reverse isolation to −6 dB worst at 6 GHz; this is probably caused by shunt capacitance introduced by ESD. So there needs to be a careful adjustment of the parasitic resistance and parasitic capacitance in future layout work, trading matching conditions, bandwidth and gain.

The measured noise figure is in the range of 2.3–3.8 dB, which is worst at 6 GHz. As we can see clearly, NF increases in

Table 1. Performance comparisons.

Reference	Technology	Freq. (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm) @ 5 GHz	Power (mW)	ESD (kV)
Ref. [3]	0.18 μm SiGe BiCMOS	2–10	< 3.5	11.5	> -7.5	7.2	–
Ref. [4]	0.18 μm SiGe BiCMOS	3.1–10.6	< 5.65	16.1	–	3.65	1.5
Ref. [5]	0.35 μm SiGe BiCMOS	3.1–10.6	< 6.4	10	–	5.4	–
Ref. [1]	0.18 μm RFCMOS	2.3–9.2	< 3.9	9.3	> -15	13.2	–
This work	0.18 μm SiGe BiCMOS	2.1–6	2.3–3.8	12	> -8	8	2

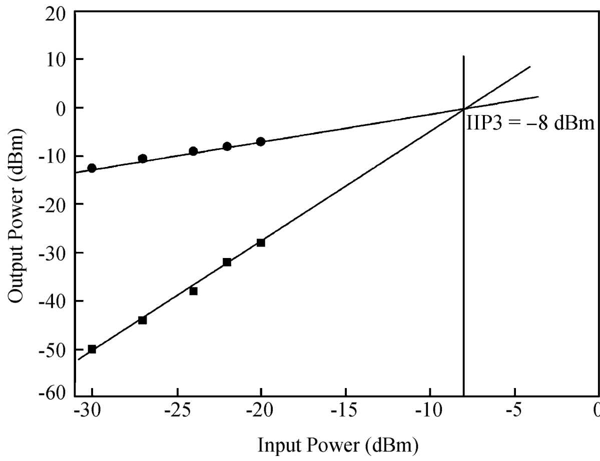

Fig. 8. Measured IIP3 at 6 GHz.

high frequency to the roll-off in S_{21}. Table 1 provides a comparison of the main RF performance metrics of some representative RFCMOS and BiCMOS wideband LNAs, including UWB LNAs covering 3.1–10.6 GHz; the noise performance of this work is the lowest of all surveyed wideband LNAs.

5. Conclusions

This paper presents a multi-mode, wideband SiGe BiCMOS low-noise amplifier (LNA) for multi-mode wireless applications. When the LNA is operating at the 2.1–6 GHz band with ESD protection, the experimental results show an average 12 dB gain over the whole band. The LNA has a noise figure of 2.3–3.8 dB and the IIP3 is −8 dBm at 6 GHz.

References

[1] Bevilacqua A, Niknejad A. An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers. ISSCC Dig Tech Papers, 2004: 384

[2] Dao V K, Choi B G, Park C S. A dual-band CMOS RF front-end for 2.4/5.2 GHz applications. Proceedings of International Conference on Applied Sciences & Technology, 2007: 145

[3] Park Y, Lee C H, Laskar J. The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation. IEEE Trans Microw Theory Techs 2006, 54: 1687

[4] Bhatia K, Hyvonen S, Rosenbaum E. A compact, ESD-protected, SiGe BiCMOS LNA for ultra-wideband applications. IEEE J Solid-State Circuits, 2007, 42: 1121

[5] Tsai M D, Lin K Y, Wang H. A 5.4-mW LNA using 0.35 μm SiGe BiCMOS technology for 3.1–10.6-GHz UWB wireless receivers. RFIC Symp Dig, 2005: 335

[6] Goo J, Ahn H T, Ladwig D J, et al. A noise optimization technique for integrated low-noise amplifiers. IEEE J Solid-State Circuits, 2002, 37: 994

[7] Lee T H. The design of CMOS radio-frequency integrated circuits. Cambridge University Press, 1998