120-nm gate-length $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ InP-based HEMT*

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Abstract: 120 nm gate-length $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ InP-based high electron mobility transitions (HEMTs) are fabricated by a new T-shaped gate electron beam lithograph (EBL) technology, which is achieved by the use of a PMMA/PMGI/ZEP520/PMGI four-layer photoresistor stack. These devices also demonstrate excellent DC and RF characteristics: the transconductance, maximum saturation drain-to-source current, threshold voltage, maximum current gain frequency, and maximum power-gain cutoff frequency of InGaAs/InAlAs HEMTs is 520 mS/mm, 446 mA/mm, –1.0 V, 141 GHz and 120 GHz, respectively. The material structure and all the device fabrication technology in this work were developed by our group.

Key words: HEMT; InP; InGaAs/InAlAs; cutoff frequency; T-shaped gate
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1. Introduction

With the recent development of broadband and satellite communications, one of the main objectives of modern microelectronics is the fabrication of devices with increasing cutoff frequency and low noise figure[1,2]. The state-of-the-art of high-frequency and low noise performances is achieved mainly by HEMTs using the InAlAs/InGaAs material system due to high electron mobility, high saturation velocity, and high sheet carrier density obtained in this material system[3].

This paper reports a 120-nm gate-length InP-based HEMT which exhibits excellent DC and RF performances by our group's optimizing a series of key processes. The current-gain cutoff frequency (f_T) of 141 GHz is achieved successively. The other corresponding characteristic parameters including transconductance (G_m), maximum saturation drain-to-source current (I_{DSS}), threshold voltage (V_T), and maximum power-gain cutoff frequency (f_{max}), of the InAlAs/InGaAs HEMTs are 520 mS/mm, 446 mA/mm, –1.0 V and 120 GHz respectively. These good performances are advantageous in many millimeter-wave applications.

2. Material structure

An epitaxial structure of the InGaAs/InAlAs channel HEMT employed in our study is shown in Fig. 1. All layers were grown by MBE on a semi-insulating InP-substrate. From bottom to top, the basic structure consists of a 300-nm $In_{0.52}Al_{0.48}As$ buffer layer, a 10-nm $In_{0.7}Ga_{0.3}As$ channel followed by a 3-nm spacer layer and Si-δ-doped (5×10^{12} cm^3) $In_{0.52}Al_{0.48}As$ donor layer. Then a 10-nm undoped $In_{0.52}Al_{0.48}As$ Schottky layer was grown followed by a 6-nm InP Etch-stopper layer and a 30-nm doped (1×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ cap layer.

3. Fabrication process

The shape of source and drain was defined first, and then a six-layer Ni/Ge/Au/Ge/Ni/Au alloy was deposited and lifted off on the layer, and a low temperature alloy method was performed in order to achieve low contact resistance[4]. Secondly, the measurement of contact resistivity was carried out by the transmission line model (TLM) method with a typical result of 0.20 Ω· mm. Then the mesa isolation was formed by wet chemical etching using an aqueous solution of phosphate (H_3PO_4) and hydrogen peroxide (H_2O_2) and Ti/Au connection wire metal was evaporated by an electronic beam evaporation system.

The gate formation process is followed: first, four layers of electron beam (EB) resist (PMMA/PMGI/ZEP520/PMGI) were coated upon the surface, which is different from our group previous trilayer resist process[4–6]. This is mainly due to these considerations as follows. First of all, to produce around 100-nm T-shaped gate, the width-length ratio of the T-shaped gate foot should meet certain requirements, and the measurement such as replacing a part of the ZEP520A with PMGI can thin the thickness of ZEP520A and are conducive to producing a shorter gate length device. Then ZEP520 is difficult to remove

$In_{0.53}Ga_{0.47}As$	Cap	30 nm	Si	1×10^{19} cm^{-3}
InP	Etch-stopper	6 nm		
$In_{0.52}Al_{0.48}As$	Barrier	10 nm		
Planar Si-δ-doped			Si	5×10^{12} cm^{-3}
$In_{0.52}Al_{0.48}As$	Spacer	3 nm		
$In_{0.7}Ga_{0.3}As$	Channel	10 nm		
$In_{0.52}Al_{0.48}As$	Buffer	300 nm		
SI InP substrate				

Fig. 1. InGaAs/InAlAs HEMT epitaxial layer structure.

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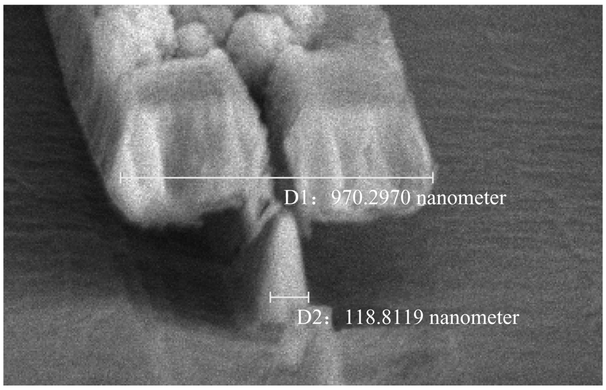

Fig. 2. SEM photo of T-shaped pattern of the InGaAs/InAlAs HEMT.

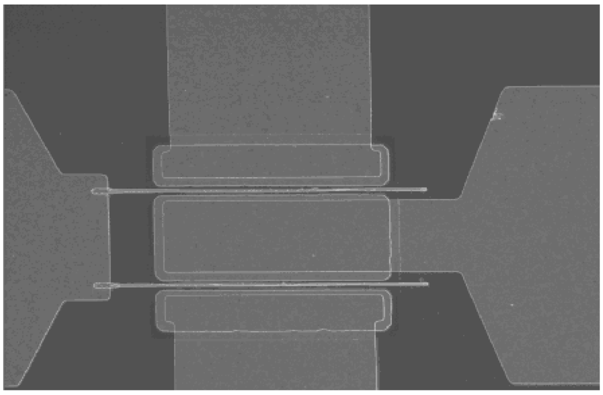

Fig. 3. Partial photograph of the InGaAs/InAlAs HEMT.

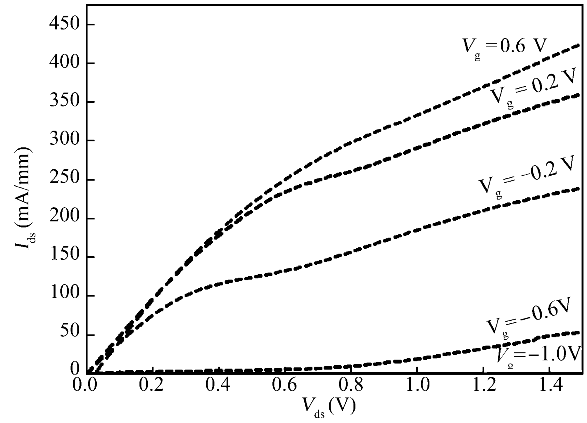

Fig. 4. DC characteristics of the InGaAs/InAlAs HEMT.

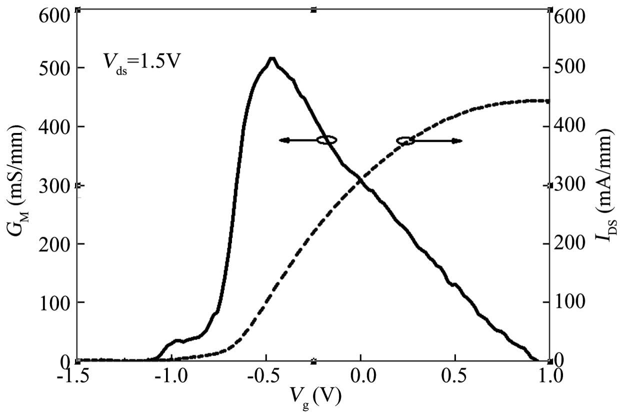

Fig. 5. Transfer characteristics of the HMET.

clearly. So we choose PMGI as the bottom of the four-layer photoresistor stack. It is easily removed to ensure imaging is complete without EB resist on chip surface. Secondly, EB exposure, development of each photoresistor layer and gate recess etching were carried out in turn. The gate-recess etching was performed by wet chemical etching using an aqueous mixture of citric acid ($C_6H_8O_7$) and H_2O_2, whose etching selectivity ratio of InGaAs over InP is about 160[7]. Finally, a Ti/Pt/Au gate metal was evaporated and lifted off. Figure 2 shows an SEM photo of the T-shaped gate pattern. Figure 3 shows a photograph of the device we obtained with a gate length of 120 nm, a gate width of 2×50 μm and source–drain space L_{ds} of 2 μm. During the whole process, no surface passivation is performed. This is because passivation will cause a parasitic capacitance effect of the gate, and then weaken the high-frequency performances such as the current cut-off frequency and maximum oscillation frequency.

4. Device performances

Figure 4 shows the current–voltage characteristics of a 120-nm-gate HEMT, which was measured at room temperature. The gate-source voltage V_{gs} is increased from (bottom) –1.0 to (top) 0.6 V with steps of 0.4 V. Good pinch-off characteristics and saturation drain current are observed. The saturation drain-to-source current is about 446 mA/mm. Figure 5 shows the gate-bias dependence of transconductance and drain current of the HEMT with a 120-nm gate length. A maximum extrinsic transconductance of 520 mS/mm is obtained at $V_{gs} = -0.5$ V and $V_{ds} = 1.5$ V. The drain current in the subthreshold is predominated by the gate leakage current from the drain to the gate. The gate leakage current is nearly 0.1 μA, which shows the excellent pinch-off performance. The pinch-off voltage V_T is –1.0 V.

RF performances of the device were characterized by on-wafer S-parameter measurements using a HP8510C vector analyzer. The measurements were carried out over the frequency from 0.1 to 26.1 GHz with steps of 0.1 GHz at room temperature. S-parameter measurements for open and short pads were also performed on the same wafer in order to calibrate the parasitic capacitance and inductance components related to the pad metals. Figures 6 and 7 show the frequency dependence of current gain (H_{21}) and maximum power-gain cutoff frequency of the 120-nm-gate HEMT with drain–source voltage of 1.5 V and a gate-source voltage of -0.5 V after these parasitic effects are de-embedded. Finally, the current cut-off frequency (f_T) of 141 GHz is extrapolated with –20 dB/decade in the curve of H_{21} versus frequency. In accordance with the same extrapolation method, the fabricated 2×50 μm HEMT demonstrated a maximum power-gain cutoff frequency of about 120 GHz.

5. Conclusion

120-nm gate-length InP-based HEMTs have been fabricated by electron beam lithography technology. A T-shaped gate has been used to decrease the parasitic capacitance and

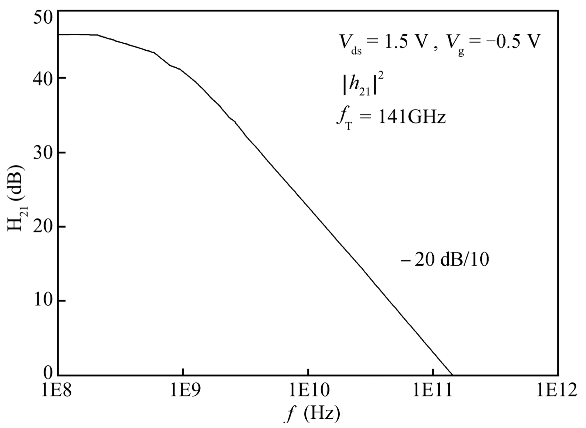

Fig. 6. Frequency dependence of current gain (H_{21}) of the HEMT.

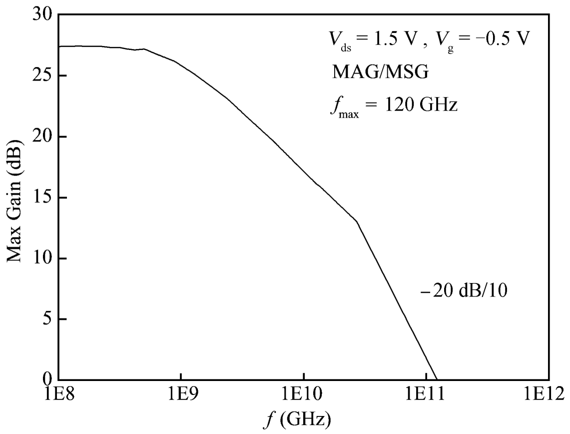

Fig. 7. Frequency dependence of maximum power gain of the HEMT.

resistance of the gate. The device exhibits excellent DC and RF performances. The transconductance, maximum saturation drain current, the threshold voltage, current cut-off frequency , and maximum power-gain cutoff frequency of the $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ HEMTs were 520 mS/mm, 446 mA/mm, –1.0 V, 141 GHz and 120 GHz respectively. Consequently, the InGaAs/InAlAs HEMTs are promising in millimeter wave devices and integrated circuits.

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