Fast statistical delay evaluation of RC interconnect in the presence of process variations

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Abstract: Fast statistical methods of interconnect delay and slew in the presence of process fluctuations are proposed. Using an optimized quadratic model to describe the effects of process variations, the proposed method enables closed-form expressions of interconnect delay and slew for the given variations in relevant process parameters. Simulation results show that the method, which has a statistical characteristic similar to traditional methodology, is more efficient compared to HSPICE-based Monte Carlo simulations and traditional methodology.

Key words: process variations; RC delay; static delay
DOI: 10.1088/1674-4926/30/4/045010 **EEACC:** 7410D; 5120

1. Introduction

As process technology moves into the DSM regime, process fluctuation, which causes interconnect geometry to deviate from the ideal case, is now playing a more important role in determining the timing behavior of high performance IC[1]. Delay and slew evaluation of RC interconnect is changed from a deterministic problem to a probabilistic problem. Most researchers still consider interconnect timing analysis to be a deterministic problem, and statistical behaviors of the delay and slew cannot be captured in the early design stage[2]. Furthermore, conventional static timing analysis (STA) using best/worst case analysis is overly pessimistic[3]. Thus, it is crucial to develop an efficient and accurate strategy for delay analysis during early design.

Recently, Agawal *et al.*[4] developed a new statistical approach to capture the effect of interconnect variability on delay. Actually, the method is not very accurate or efficient owing to the adoption of linear fitting and traditional statistical delay evaluation methodology.

In order to solve the above-mentioned problem, fast statistical delay and slew evaluation of RC interconnect in the presence of process variations is given in this paper. Based on optimized quadratic fitting, delay and slew are expressed directly as functions of interconnect geometric parameters. The proposed strategy is more accurate than that obtained by using linear fitting, and has higher computational efficiency than that using normal quadratic fitting. Compared to HSPICE-based Monte Carlo simulation, the proposed method is several times faster than, and also maintains practically the same accuracy as, the traditional method. Typically, distribution characteristics of delay and slew are dramatically improved.

2. Impact of process variations on interconnect parameters

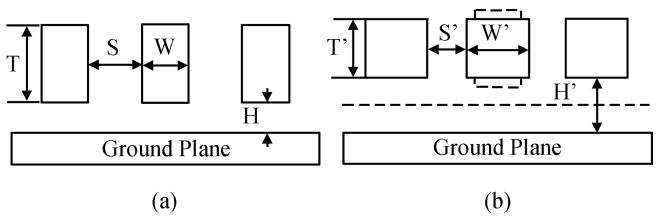
Process variations of interconnect originate from two aspects, non-uniform thickness caused by chemical mechanical polishing (CMP), and line edge roughness (LER) or line width roughness (LWR) caused by photolithography. With any change in the physical dimensions of interconnect, its resistance and capacitance also change, causing interconnect delay and slew to fluctuate. In order to model the impact of variability on delay and slew, we need to capture the effect of geometric variations on the electrical parameters.

For the simple interconnect structure shown in Fig. 1, the geometric parameters of interest are metal thickness (T), interlayer dielectric (ILD) thickness (H), linewidth (W) and linespace (S). For the middle line surrounded by two lines on the sides, the line resistance R, self-capacitance $C_{\rm af}$, and coupling capacitance $C_{\rm Coup}$ per unit length can be expressed using the following equations[5]:

$$R = \rho_{\rm eff}\frac{1}{WT}, \tag{1}$$

$$\frac{C_{\rm af}}{\varepsilon_{\rm ox}} = \frac{2W}{H} + 4.08\left(\frac{T}{T+4.53411H}\right)^{0.071} \times \left(\frac{S}{S+0.5355H}\right)^{1.773}, \tag{2}$$

$$\frac{C_{\rm couple}}{\varepsilon_{\rm ox}} = 1.4116\frac{T}{S}\exp\left(-\frac{4S}{S+8.014H}\right) + 2.3704\left(\frac{W}{W+0.3078S}\right)^{0.25724}$$



(a) (b)

Fig. 1. Cross-section of parallel interconnect lines.

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Received 16 September 2009, revised manuscript received 21 December 2009
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Table 1. Comparing errors of the linear model and nonlinear models.

Ranges of process variations (%)	Errors of linear model (%)	Errors of complete quadratic model (%)	Errors of simplified quadratic model (%)
±40	–9.65 to 17.72	–7.76 to 5.94	–8.52 to 6.17
±30	–4.77 to 8.66	–3.00 to 2.36	–3.85 to 2.50
±20	–1.86 to 3.55	–0.76 to 0.63	1.34 to 0.71
±10	–0.41 to 0.85	–0.04 to 0.03	–0.23 to 0.05

$$\times\left(\frac{H}{H+8.961S}\right)^{0.7571}\exp\left(-\frac{2S}{S+6H}\right), \tag{3}$$

where ρ_{eff} is the effective resistivity and ε_{ox} is the effective dielectric constant.

Any change in the physical dimensions of the wire can cause changes in the electrical parameters. Changes in electrical parameters can have an impact on circuit performance. Quantification of process variations is required. The parameters influenced by process variations are shown in Fig. 1. To simplify the analysis we assume linewidth (W) and linespace (S) are perfectly negatively correlated. Therefore, the parameters considered are metal thickness (T), ILD thickness (H) and linewidth (W).

Relative variations of different geometric parameters with process fluctuations are, to simplify the analysis, defined as follows

$$\Delta w=\frac{\Delta W}{W},\quad \Delta t=\frac{\Delta T}{T},\quad \Delta h=\frac{\Delta H}{H}, \tag{4}$$

where ΔW, ΔT and ΔH are absolute variations of the corresponding geometric parameters.

Then, interconnect resistance and capacitance in the presence of process variations can be written as

$$R=[1+f_{\text{R}}(\Delta w,\Delta t)]\,R_{\text{nom}}, \tag{5}$$

$$C=[1+f_{\text{C}}(\Delta w,\Delta t,\Delta h)]\,C_{\text{nom}}, \tag{6}$$

where R_{nom} and C_{nom} are the nominal resistance and nominal capacitance, respectively. f_{R} and f_{C} signify relative changes in interconnect electrical parameters with process fluctuations. f_{R} can be derived from Eq. (1).

$$f_{\text{R}}=[(1+\Delta w)(1+\Delta t)]^{-1}-1. \tag{7}$$

The next step is to compute f_{C}. For small process variations, a linear model is adopted to estimate the effects of process variations on capacitance[4, 6]. With the increments in process variations, the accuracy of the linear model quickly decreases, especially for the cases in which ±20% process variations exist. The errors of the linear model are illustrated in Table 1. To improve the accuracy, a quadratic model is used to evaluate the effects of process variations on capacitance. The expression of f_{C} is obtained as

$$\begin{aligned}f_{\text{C}}=&\alpha_1\Delta w+\alpha_2\Delta t+\alpha_3\Delta h+\alpha_4(\Delta w)^2+\alpha_5(\Delta t)^2\\&+\alpha_6(\Delta h)^2+\alpha_7\Delta w\Delta t+\alpha_8\Delta w\Delta h+\alpha_9\Delta t\Delta h.\end{aligned} \tag{8}$$

According to the simulations shown in Table 1, high-order items $(\Delta w)^2$, $(\Delta t)^2$and $\Delta w\Delta t$ in Eq. (6) which have little effect on f_{C} can be ignored. Equation (6) can be rewritten as

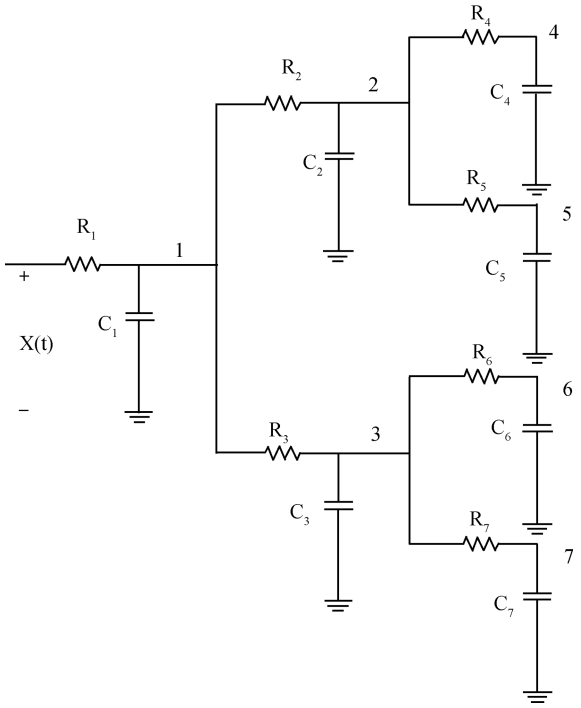

Fig. 2. Circuit of general RLC tree.

$$\begin{aligned}f_{\text{C}}=&\alpha_1\Delta w+\alpha_2\Delta t+\alpha_3\Delta h+\alpha_5(\Delta h)^2\\&+\alpha_6\Delta w\Delta h+\alpha_7\Delta t\Delta h.\end{aligned} \tag{9}$$

3. Fast statistical delay of RC interconnect

In this section, a simple but accurate nominal delay metric named the D2M model[6] is first briefly introduced. Then, a fast statistical delay model is developed by taking the D2M model as an example. Actually, the other delay models can be easily extended to fast statistical delay evaluation in a similar manner.

Much work has been done to develop accurate metrics for calculating delay and slew in RC interconnects. Most of the existing models are moment-based, requiring computation of circuit moments that are then translated to delay and slew. The first two moments of any node i in the general RC interconnect tree shown in Fig. 2 can be described as[7–9]

$$m_1^i=-\sum_k C_k R_{ik}, \tag{10}$$

$$m_2^i=\sum_k\sum_j C_k R_{ik} C_j R_{kj}. \tag{11}$$

After obtaining the first two moments, the D2M model[6] and

S2M model[10] with closed-form expressions are as follows:

$$\text{Delay}_{\text{D2M}} = \ln 2 \frac{(m_1^i)^2}{\sqrt{m_2^i}}, \tag{12}$$

$$\text{Slew}_{\text{S2M}} = \frac{\sqrt{-m_1}}{\sqrt[4]{m_2}} \ln 9 \sqrt{2m_2 - m_1^2}. \tag{13}$$

Substituting Eqs. (5) and (6) into Eqs. (10) and (11) gives

$$m_1^i = (1 + f_{\text{R}})(1 + f_{\text{C}})(m_1^i)_{\text{nom}}, \tag{14}$$

$$m_2^i = (1 + f_{\text{R}})^2(1 + f_{\text{C}})^2(m_2^i)_{\text{nom}}. \tag{15}$$

The above two equations show the first and second moment expressions as functions of normal random variables representing variations in back-end physical dimensions. $(m_1^i)_{\text{nom}}$ and $(m_2^i)_{\text{nom}}$ represent nominal values for the first two circuit moments, computed when the wire dimensions are at their nominal or typical values.

Once the moments are expressed as functions of changes in physical dimensions, the 50% delay and slew of the D2M model considering process variations can easily be written as

$$\text{Delay} = (1 + f_{\text{R}})(1 + f_{\text{C}})\text{Delay}_{\text{nom}}, \tag{16}$$

$$\text{Slew} = (1 + f_{\text{R}})(1 + f_{\text{C}})\text{Slew}_{\text{nom}}, \tag{17}$$

where $\text{Delay}_{\text{nom}}$ and Slew_{nom} are the 50% delay and slew without process variations, determined by Eqs. (12) and (13).

Based on the related information described above, and assuming length, geometric parameters and their variations of each interconnect segment in the RC tree are known, the overall computing flow of the fast statistical delay is summarized below.

Step 1: Obtain the length of each interconnect segment of the RC tree;

Step 2: Calculate values of nominal resistance and capacitance for each segment of the given interconnect tree [see Eqs. (1) to (3)];

Step 3: Obtain the $\text{Delay}_{\text{nom}}$ and Slew_{nom} based D2M model and the S2M model [see Eqs. (12) and (13)];

Step 4: Take geometric variations into account to calculate values of f_{R} and f_{C} [see Eqs. (7) and (9)];

Step 5: Capture RC interconnect delay and slew in the presence of process variations [see Eqs. (16) and (17)].

4. Simulation and verification

In this section, we will compare the proposed method with HSPICE-based Monte Carlo simulations and traditional methodology. Method 1 is the traditional statistical delay evaluation methodology. The algorithm of traditional method 1 is as follows:

Step 1: Get the length of each interconnect segment of RC tree;

Step 2: Take geometric variations into account to calculate the resistance and capacitance for each segment of the given interconnect tree [see Eqs. (1) to (3)];

Step 3: Obtain RC interconnect delay and slew in the in the presence of process variations [see Eqs. (12) and (13)];

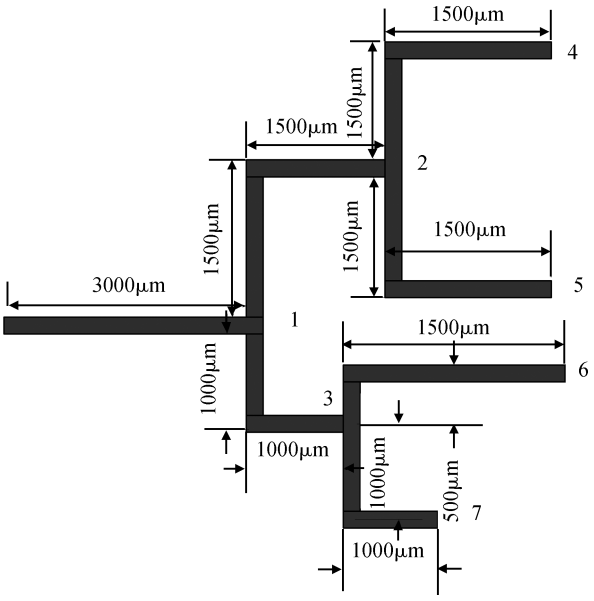

Fig. 3. General interconnect tree.

Table 2. Interconnect technology parameters[11].

Parameter	Value
Technology node	45
Global wiring 1/2 pitch	67.5 nm
Global wiring thickness	162 nm
ILD thickness	81 nm
Conductor effective resistivity	3.10 $\mu\Omega$·cm
Effective dielectric constant	2.75

Method 2 is the proposed model in this paper. For this test case, the values for W, T, and H were chosen from the 45 nm process, and their 3-σ variabilities were all selected to be 30%. The key parameters of the 45 nm process technology are listed in Table 2, and the general interconnect tree is just like that shown in Fig. 3.

Figure 4 shows probability density functions of delay and slew of node 4, obtained using Monte Carlo simulations with 10000 sampling points, and compares them to Gaussian distributions which are obtained using the analytical model proposed in the previous section, and to the traditional methodology. Two important observations can be made. First, the delay and slew in the RC interconnect tree obey Gaussian distributions. Second, the mean values of delay and slew obtained using the proposed model are very close to those obtained using the traditional methodology, and both obtained values of delay mean are close to those obtained using HSPICE-based Monte Carlo simulations.

Table 3 compares the mean and average deviation found using Monte Carlo simulations with the proposed model and the traditional methodology. It is found that the means obtained from different methods have similar accuracy. The errors of means of 50% delay and slew are less than 1% and 3%, respectively. The results show that the accuracy of the proposed model is the same as in the traditional methodology. We also find that the errors of average deviations are all less than 4%. The results show that the statistical characteristic of 50% delay and slew, considering the effects of process variations, are

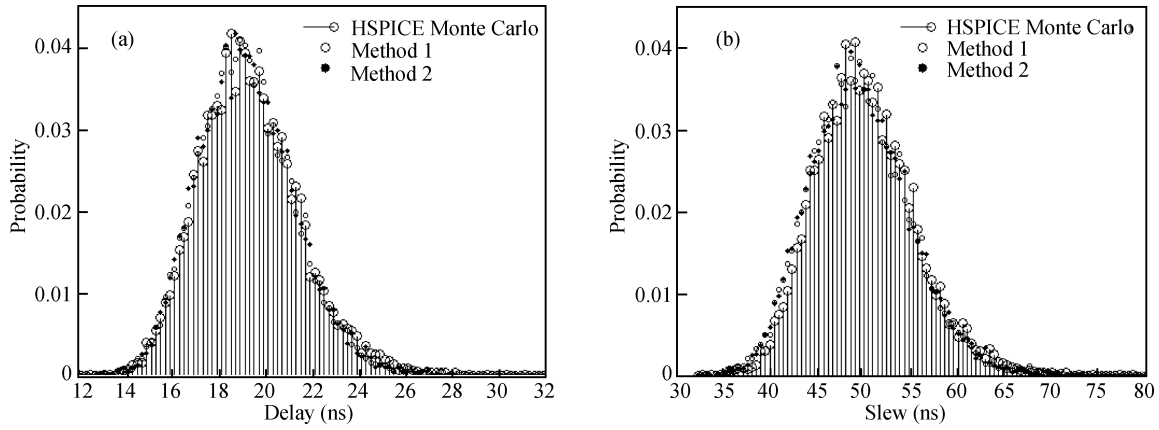

Fig. 4. Probability density as functions of (a) delay and (b) slew (Node 4).

Table 3. Means and average deviations of delay and slew.

Node	Delay/Slew	Mean/Avgdev	HSPICE (ns)	Method 1		Method 2	
				Values (ns)	Error (%)	Values (ns)	Error (%)
4	Delay	Mean	19.3044	19.1874	−0.61	19.2197	−0.44
		Avgdev	1.6915	1.6309	−3.58	1.6795	−0.71
	Slew	Mean	50.0723	49.5821	−0.98	49.6656	−0.81
		Avgdev	4.1862	4.2144	0.67	4.1457	−0.97
5	Delay	Mean	19.3044	19.2203	−0.44	19.3032	−0.01
		Avgdev	1.6915	1.6539	−2.23	1.6998	0.49
	Slew	Mean	50.0723	49.6674	−0.81	49.8815	−0.38
		Avgdev	4.1862	4.2739	2.09	4.2254	0.94
6	Delay	Mean	13.5743	13.6672	0.68	13.7017	0.94
		Avgdev	1.1896	1.1699	−1.66	1.1824	−0.61
	Slew	Mean	45.3271	44.1436	−2.61	44.3251	−2.21
		Avgdev	3.7578	3.7785	0.55	3.8190	1.63
7	Delay	Mean	13.5743	13.6604	0.63	13.6587	0.62
		Avgdev	1.1896	1.1772	−1.04	1.1824	−0.61
	Slew	Mean	45.3271	44.1216	−2.66	44.1160	−2.67
		Avgdev	3.7578	3.8019	1.17	3.8190	1.63

Table 4. Operation time.

	Method	Operation time (s)
HSPICE	HSPICE	5.98×10^{3}
D2M	Method 1	7.00×10^{-2}
	Method 2	3.60×10^{-3}
S2M	Method 1	7.10×10^{-2}
	Method 2	3.60×10^{-3}

good.

The running time for all three methods on the same PC is also listed in Table 4. It can be found that the proposed method has less running time compared with the Monte Carlo simulations and traditional methodology. This is due to the fact that the proposed model enables closed-form computation of interconnect delay and slew for the given variations in relevant process parameters, such as linewidth, metal thickness, metal spacing, and ILD thickness.

Finally, an actual net taken from an industrial design was tested and the results were compared with a linear model that also used statistical static timing analysis[4]. An actual clock tree is shown in Fig. 5(a), and the topology of the clock tree is shown in Fig. 5(b). 3-σ variabilities in the physical dimensions were taken from relevant process technology. We examined delay and slew distributions at representative nodes 3, 10 and 16 and compared them to the proposed model in this paper and the linear model in Ref. [4]. The results shown in Table 5 indicate that the model works very well and is more accurate than the linear model.

5. Conclusion

In this work, we proposed fast delay and slew models of interconnect for statistical static timing analysis taking into account process variations. In this method, a quadratic model is used to estimate the effects of process variations for higher computational efficiency. The proposed models enable optimized closed-form computation of interconnect delay and slew for the given variations in relevant process parameters. Results show that the proposed method has less running time compared with the HSPICE-based Monte Carlo simulations and traditional methodology.

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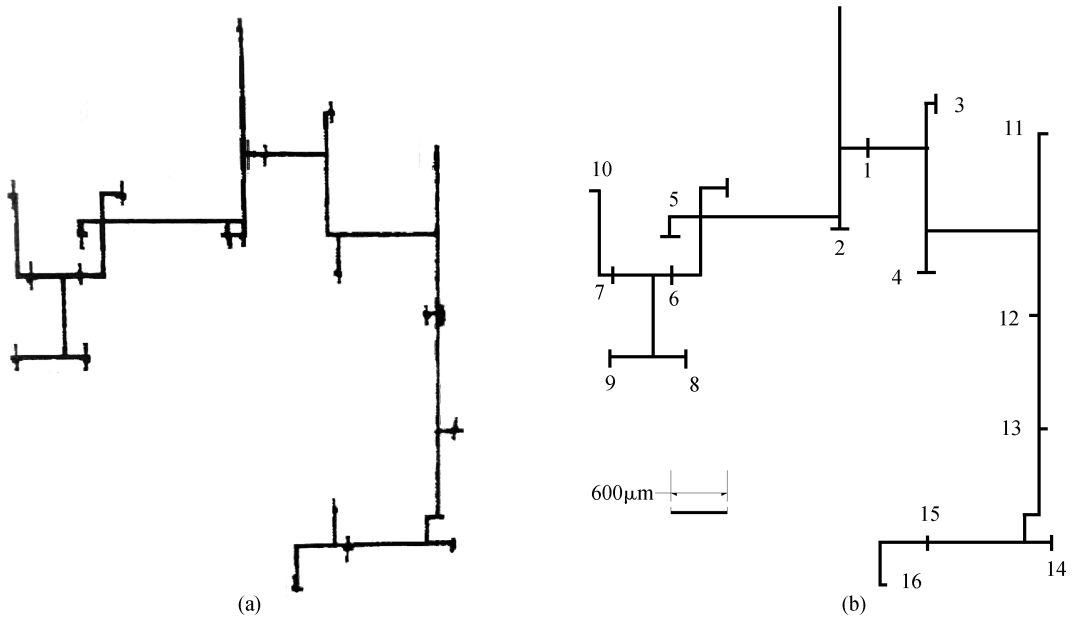

Fig. 5. (a) A clock tree taken from an industrial design. (b) Topology of the clock tree.

Table 5. Delay and slew distributions of a clock tree shown in Fig. 5.

Node	Delay/Slew	Mean/Avgdev	HSPICE (ns)	Proposed model		Linear model	
				Values (ns)	Error (%)	Values (ns)	Error (%)
3(2)	Delay	Mean	5.5075	5.5927	1.55	5.5752	1.23
		Avgdev	0.5976	0.6084	1.81	0.6075	1.66
	Slew	Mean	28.5470	27.9687	−2.03	27.9370	−2.14
		Avgdev	2.9865	3.0425	1.88	3.3835	13.29
10(7)	Delay	Mean	8.9263	9.0198	1.05	9.6689	8.32
		Avgdev	0.9917	0.9769	−1.49	1.0725	8.15
	Slew	Mean	29.1189	28.9470	−0.50	28.4673	−2.24
		Avgdev	2.8635	2.9005	1.29	3.3116	15.65
16(9)	Delay	Mean	17.8888	18.0951	1.15	18.0840	1.09
		Avgdev	1.9735	1.9874	0.704	2.0091	1.80
	Slew	Mean	39.6624	40.5949	2.35	42.6927	7.64
		Avgdev	3.9344	4.0482	2.89	4.3852	11.46

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