Grain boundary layer behavior in ZnO/Si heterostructure*

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Abstract: The grain boundary layer behavior in ZnO/Si heterostucture is investigated. The current–voltage (I–V) curves, deep level transient spectra (DLTS) and capacitance–voltage (C–V) curves are measured. The transport currents of ZnO/Si heterojunction are dominated by grain boundary layer as high densities of interfacial states existed. The interesting phenomenon that the crossing of ln I–V curves of ZnO/Si heterojunction at various measurement temperatures and the decrease of its effective barrier height with the decrement of temperature are in contradiction with the ideal heterojunction thermal emission model is observed. The details will be discussed in the following.

Key words: ZnO/Si heterostructure; grain boundary layer; intrinsic defects; deep level
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1. Introduction

Zinc oxide (ZnO) is a wide-band-gap semiconductor having properties suitable for various applications such as ultraviolet (UV) optoelectronic devices, transparent high power and high frequency electronic devices, surface acoustic wave devices, piezoelectronic transducers, and chemical gas sensors. The native ZnO is an insulator if it is satisfied stoichiometry. However, the undoped ZnO shows typically n-type conductivity, which is attributed to the structural defects[1]. In view of the advantages of electronic and optical confinements offered by heterojunction structures, n-type ZnO has, thus, been frequently deposited on various p-type semiconductors[2]. ZnO films depositing on a silicon substrate usually form polycrystalline structure as a large lattice mismatch, and the behavior of the grain boundary layer of ZnO/Si heterostructure is noteworthy in the carrier transport process. However, so far as we know, there is still no systematic investigation regarding these aspects.

In this paper, DLTS, I–V and C–V measurements are used to investigate the behavior of grain boundary layer of ZnO/Si heterostructure in the carrier transport process.

2. Sample prepared and measurements

P-Si (100) wafers with a resistance of 2–4 Ω·cm were used as substrates. ZnO:LiCl thin films were prepared by the sol–gel approach. The sol solution was prepared by zinc acetate dehydrate (ZnO $(AC)_2$) and polyvinyl alcohol (PVA) with a concentration of 0.33 mol/L and 0.05 g/cm^3, respectively. LiCl solution with a concentration of 3.3×10^{-4} mol/L was used as dopant, which was heated up to 80 °C and stirred for 60 min. The sol was spin-coated on the polished side of Si substrate at 3000 rpm for 30 s followed by a drying process at 300 °C in a tube furnace in air for 5 min. This procedure was repeated six times for each sample. At last, sample 1 (S1) and sample 2 (S2) were annealed at O_2-600 °C and O_2-900 °C for 1 h, respectively.

A 0.01 Hz ultralow frequency sawtooth wave generator (model 439 function generator) was used as the voltage source for I–V measurement. Indium was employed as the Ohmic contacts. During all the electrical properties measurement, the samples were kept in a dark chamber. DLTS signals were obtained from the NJ.M.DLTS deep level transient spectrometer in a temperature range of 77–350 K. C–V measurement was performed with a multi-frequency LCR meter (HP model 4275A). More details about samples structure and electrical measurement apparatus can be examined in Ref. [3].

3. Experimental results and discussion

The I–V characteristics of S1 and S2 are investigated at different temperatures from 211.2 to 280.6 K and 128.6 to 276.6 K, respectively. The currents as a function of applied voltages are shown in Fig. 1.

By the theory of the heterojunction thermal emission, the characteristics of I–V can be expressed as[4]:

$$I = SA^{**}T^2 \exp(-q\phi_0/kT)\,[\exp(qV - IR_S/nkT)] = I_0\,[\exp(qV - IR_S/nkT)], \quad (1)$$

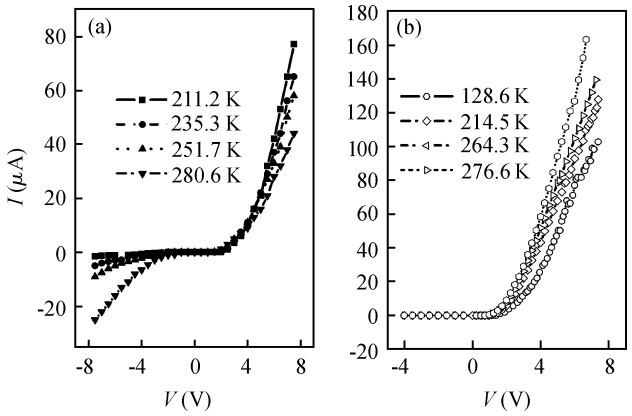

Fig. 1. I–V curves of samples after (a) O_2-600 °C and (b) O_2-900 °C annealing.

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Table 1. Characteristics of I–V, C–V, and DLTS of samples.

Sample	I–V		DLTS			C–V	
	n	R_S (kΩ)	E_T (eV)	N_t/N_B	N_t (cm^{-3})	ϕ_B(eV)	N_i(cm^{-3})
S1	19 (T = 276.6 K)	26	$E_C - 0.239$	8.99%	4.5×10^{14}	1.24	6.4×10^{14}
S2	14 (T = 280.6 K)	16	$E_C - 0.238$	8.47%	4.2×10^{14}	0.72	5.8×10^{14}

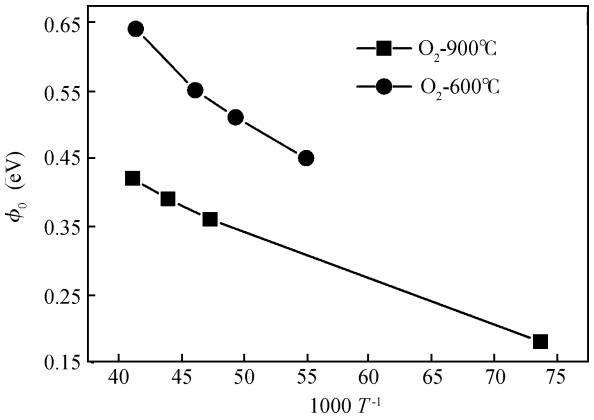

Fig. 2. Barrier height ϕ_0 as a function of the various measurement temperatures for O_2-600 °C and O_2-900 °C annealing.

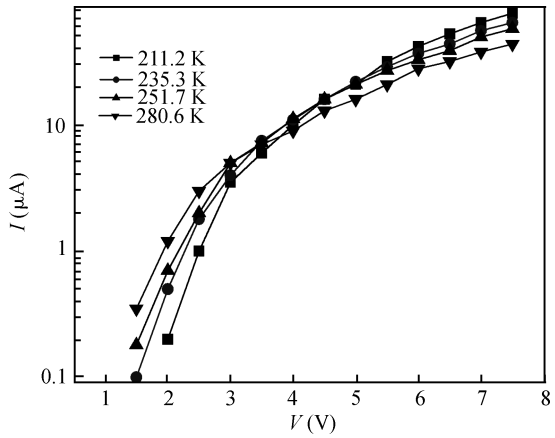

Fig. 3. ln$I$–V curve of O_2-600 °C annealing.

$$I_0 = SA^{**}T^2 \exp(-q\phi_0/kT). \quad (2)$$

Here S is the cross-sectional area, A^{**} is the Richardson's constant, ϕ_0 is the Schottky barrier height, n is the ideality factor, V is the bias voltage, k is the Boltzmann constant, T is the Kelvin temperature, R_S is the bulk series resistance, and I_0 is the saturated drain current. The ideality factor n of S1 and S2 (S1, T = 276.6 K and S2, T = 280.6 K) can be obtained by fitting Arrhenius-Plot of one of curves in Fig. 1. Also, the series resistance R_S can be obtained by fitting I–V data in Fig. 1 using the first derivative of Eq. (1)[5]. The obtained results are listed in Table 1.

Due to Eq. (2), there are obviously relationships between ϕ_0 and I_0:

$$\phi_0 = \frac{kT}{q} \ln\left(SA^{**}T^2/I_0\right), \quad (3)$$

$$\ln\left(I_0/T^2\right) = \ln SA^{**} - q\phi_0/kT. \quad (4)$$

To avoid errors of ϕ_0 caused by unreasonable selected SA^{**}, we deduce SA^{**} from following steps. Make Arrhenius-Plot using curves in Fig. 1, I_0 at various temperatures can be obtained from intercepts, where the slopes of the extrapolated ln$I$–V lines intersect with ln$I$ axis. Fit curve using Eq. (4) with obtained I_0, and then SA^{**} can be got from intercept of fitting curve. So ϕ_0 at various temperatures can be got from Eq. (3) using obtained SA^{**}. Figure 2 shows ϕ_0 of S1 and S2 as a function of the various measurement temperatures.

Figure 3 is Arrhenius-Plot of Fig. 1(a). Look into Fig. 3, it is interesting that the crossing of ln$I$–V curves is observed and the forward transport currents have a negative temperature characteristic. This phenomenon can hardly be explained by using the inhomogeneous Schottky barrier model[6].

As mentioned before, ZnO films depositing on a silicon substrate will form polycrystalline structures due to a large lattice mismatch, and grain boundary is an important feature to be considered. During the sample preparation process, the adsorption oxygen in the grain boundary forms high densities of electrons traps. Those electrons traps capture the carriers that originate from ionized bulk deep level defects, which induce the formation of electrons depleted regions adjacent to the grain boundary and corresponding space charge barriers[7].

The currents transport mechanisms of ZnO/Si heterostructure can be regarded as an emission–recombination model as high densities of interface states existed[8]. In this model, the p–n heterojunction can be regarded as p-type and n-type Schottky barrier in serials, and the I–V characteristics of heterojunction are dominated by broad gap semiconductor side completely[4]. Look into Fig. 1(a), the I–V characteristics of S1 reveals that the currents transport mechanisms are dominated by ZnO grain boundary completely. The electrons in p region inject interface region by tunneling and cross grain boundary barrier with thermal emission as S1 is applied reverse voltages. The probability of tunneling increases with reverse voltages rising and the temperature has a direct influence on the number of carriers that can cross the ZnO grain boundary. The effective concentration of carriers in ZnO grains equals to the product of the concentration of carriers that inject into interface region by tunneling and the probability of those carriers that can cross grain boundary barrier. This probability can be described as $P = \exp[-(e\phi)/kT]$ using Boltzmann distribution. Here $e\phi$ is the height of the grain barrier. Observe one of the curves shown in Fig. 1(a) whose measured temperature is 211.2 K. The probability of carriers at this measurement temperature that can cross grain boundary is low, which causes the reverse currents saturation. This probability increases with the measurement temperature rising. So the reverse currents of S1 are unsaturated gradually with the measurement temperature rising. Furthermore, the grain boundary causes the negative temperature characteristics of forward transport currents in S1, which results in the interesting phenomenon of the crossing of ln$I$–V curves. This can be illuminated as follows. In the

forward transport process, the electrons are filled into the shallower empty electron traps which are located in the intergranular regions (grain boundary layers) firstly, and then formed space charges. Those carriers can easily overcome the grain barrier from some energy state and flow into the conduct band to form electrons currents. The electrons currents increase due to the increment of electron kinetic energy as the measurement temperature rises. Thus, the numbers of space charges in the intergranular regions decrease, the electron inject interface region has to be filled with the deeper electron trap levels. This dictates the nature of the grain boundary layer as the carriers need to surmount for conduction over this barrier height. So the barrier height that these carriers have to overcome as they cross the grain boundary layer increases. Therefore, transport currents decrease with the measurement temperature rising.

The curves of ϕ_0–$1000/T$ shown in Fig. 2 reveal another aspect of the influence of interfacial states that is caused by grain boundary. On the one hand some interfacial electrons traps are not thermal activation at the low measurement temperature which causes ϕ_0 of both samples decreased with the measurement temperature decreased, but on the other hand note that ϕ_0 of S2 is lower than that of S1 in all measurement ranges as shown in Fig. 3, and R_S of S2 are smaller than that of S1 as well as n. This suggests that the microstructures of ZnO are decorated as the annealing temperature rising at O_2 ambience. Generally, the average sizes of ZnO grains enlarge with the annealing temperature rising. It can be suspected that the smaller average grain size, the more grain boundary has and the larger voltages will be dropped. This explains ϕ_0 of S2 less than that of S1 as well as R_S and n.

As high temperature annealing at O_2 ambience, oxygen diffusion into the interface of ZnO/Si heterostructure is stronger, and then Si–O bonds are formed there, which reduces the dangling bonds caused by lattice mismatch[9]. Besides, the diffusion of oxygen in the grain boundary causes the grain barrier to move into bulk grain, which results in an increase in the depletion region width[7]. So the tunneling probability of electrons is suppressed and the reverse currents of S2 at various measurement temperatures are almost saturated.

Generally, the origination of n type carriers in ZnO films is regarded as related with Zn_i [7]. In polycrystalline ZnO films, the densities of donors near the surface is lower than that in the bulk, while near the ZnO/Si interface, the donor density is even much lower. So the changes of depleted regions mainly in ZnO grains adjacent to the grain boundary as measured with C–V and DLTS[10].

Figure 4 shows the e_n–T^{-1} relationship curves of S1 and S2 measured with DLTS at different rate windows, where e_n is the electron emission rate of deep level. Due to the principle of DLTS, the slopes of curves are related with the location of deep level. Thus, it is clearly that the S1 and S2 have a same deep level E_T located at $E_c - 0.24$ eV. The obtained relative gap densities of S1 and S2 are $N_t/N_B = 8.99\%$ and $N_t/N_B = 8.47\%$, respectively. Taking the resistivity and impurity concentration of p-Si are $\rho = 2$–$4\ \Omega\cdot$cm and $N_B = 4 \times 10^{15}\text{cm}^{-3}$, the concentration of deep level impurities of S1 and S2 are $N_{t1} \approx 3.6 \times 10^{14}\ \text{cm}^{-3}$ and $N_{t2} \approx 3.4 \times 10^{14}\ \text{cm}^{-3}$, respectively.

As is known to us all, the deep levels of ZnO films have a great influence on its electrical barrier formation. There are a lot of researches about the investigation into the origination of deep level in ZnO films. Reference [11] reports the two bulks deep levels in ZnO ceramic are 0.14 eV and 0.24 eV, and also Reference [12] reports a deep level ($E_c - 0.25 \pm 0.01$eV) as research ZnO films doping with Al and Ag. All of those levels are proved not to be related with doping impurities. It is interesting that our early research work also reports the same results and has proved $E_c - 0.24$eV related with Zn_i^{**} [13].

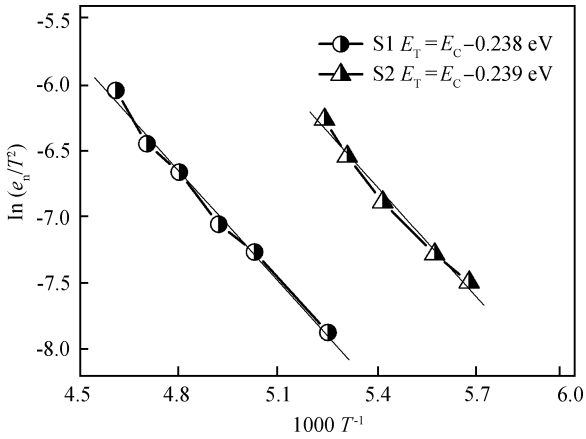

Fig. 4. Arrhenius plots of deep levels for the samples S1 and S2.

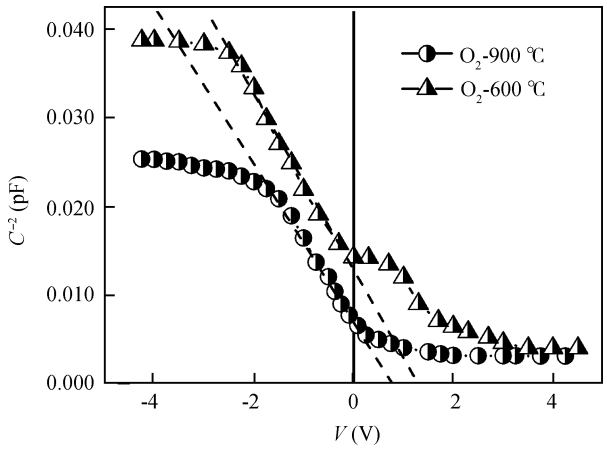

Fig. 5. Inverse of the square of capacitance versus applied voltage curves of samples.

The C^{-2}–V relationship curves of S1 and S2 measured with 1 MHz frequency are shown in Fig. 5. There is a clear shoulder on the C^{-2}–V relationship of S1 which indicates high densities of trap states in the interface. Thus, it supports that the current transport mechanisms of S1 accords with the emission-recombine model. However, note the C^{-2}–V curves of S2 returned to normal and its capacitance values decreased after annealing at O_2-900 °C, which indicts the densities of interface states decreased. This suggests that microstructures of ZnO are decorated after the high temperature annealing at O_2 ambience in another aspects.

Due to the relationship of depletion layer capacitance[14]:

$$N_i = \frac{2}{q\varepsilon_s\varepsilon_0 A^2}\frac{1}{\mathrm{d}\,(C^{-2})/\mathrm{d}V}, \tag{5}$$

$$C^{-2} = \frac{2\,(\phi_{\rm B} + V_{\rm R} - kT/q)}{q\varepsilon_{\rm s}\varepsilon_0 A^2 N_{\rm i}}. \quad (6)$$

Here, $\varepsilon_{\rm s}$ is the dielectric constant of ZnO, $\varepsilon_{\rm o}$ is the dielectric constant of vacuum, A is the junction area, $N_{\rm i}$ is the concentration of ionized donors in depleted regions and $\phi_{\rm B}$ is the apparent barrier. $N_{\rm i}$ of S1 and S2 can be obtained from the slopes of linear regions of C^{-2}–V curves (dash lines in Fig. 5) using Eq. (5), and $\phi_{\rm B}$ can be obtained from intercepts that the slopes of the extrapolated linear regions of C^{-2}–V curves intersect with voltages axis. We calculate $N_{\rm i}$ and $\phi_{\rm B}$ of S1 and S2 and list them in Table 1. Seen from Table 1, $N_{\rm t}$ and $N_{\rm i}$ of S1 and S2 are almost same, it can be confirmed that the electrons in the grain boundary layer are origination from ionized intrinsic defects $Zn_{\rm i}$.

Due to the relationship $\phi_{\rm B} = \frac{e^2 N_{\rm S}^2}{8\varepsilon_0\varepsilon_{\rm s} N_{\rm d}}$ using data in Table 1, the densities of effective trap states on grain surface of S1 and S2 are $N_{\rm S1} = 1.9 \times 10^{11}$ cm^{-2} and $N_{\rm S2} = 1.3 \times 10^{11}$ cm^{-2}, respectively. These decrease obviously compared with the report value that is 10^{13} cm^{-2} in the undoped ZnO grain boundary which are not heat treatment at O_2 ambience[1]. Note that $N_{\rm t}$ and $N_{\rm i}$ of S2 has a little decrement compared with that of S1, but $\phi_{\rm B}$ of S2 decreases obviously. It is clearly that the densities of electrons have a relationship with O_2 ambience due to the relationship $\mathrm{ZnO} \Longleftrightarrow \mathrm{Zn_i^{**}} + 2\mathrm{e}' + \frac{1}{2}\mathrm{O_2(g)}$. The covered oxygen on grain surface begin to desorption and the diffusion of $Zn_{\rm i}$ to grain surface is stronger at the high annealing temperature. The oxygen ions recombine with $Zn_{\rm i}^{**}$ which reduce $[Zn_{\rm i}]$ and $[V'_{\rm Zn}]$. The reasons mentioned above working together result the height of grain boundary reduced. As to $N_{\rm i2}$ reduces little compared with $N_{\rm i1}$, we suspect the decomposable process of ZnO at O_2-900 °C has suppressed the reduction of intrinsic defects. The diffusion of oxygen from grain boundary into grain not only decreases $Zn_{\rm i}$ but also changes its distributing. So the effective concentration of $Zn_{\rm i}$ near grain surface is lower than $[Zn_{\rm i}]$ measured with C–V, but $\phi_{\rm B}$ of S2 decreases obviously.

4. Conclusion

In this paper, the behaviors of the grain boundary layer of ZnO/Si heterostructure are investigated. The crossing of $\ln I$–V curves and negative temperature characteristics of forward transport currents in S1 can be explained using the behaviors of the grain boundary layer. The experiment shows that the n type carriers in ZnO film originate from $Zn_{\rm i}^{**}$. After high temperature annealing at O_2 ambience, the microstructures of ZnO/Si heterostructure are decorated and stoichiometric deviation is improved, the influence of interfacial states on the carriers transport process of ZnO/Si heterostructure is weakened.

References

[1] Van de Walle C G. Hydrogen as a cause of doping in zinc oxide. Phys Rev Lett, 2000, 85: 1012

[2] Chuang R W, Wu R, Li W, et al. ZnO-on-GaN heterojunction light-emitting diode grown by vapor cooling condensation technique. Appl Phys Lett, 2007, 91: 231113

[3] Liu Cihui, Chen Yulin, Lin Bixia. Electrical properties of ZnO/Si heterostructure. Chin Phys Lett, 2001, 18(8): 1108

[4] Yu Lisheng. Semiconductor heterostructure physics. 2nd ed. Beijing: Science Press, 2006: 73 (in Chinese)

[5] Liu Cihui, Liu Bingce, Ma Zeyu, et al. The contact and temperature characteristic of ZnO/Si. J Func Mater, 2006, 37: 6857 (in Chinese)

[6] Chand S. On the intersecting behaviour of current–voltage characteristics of inhomogeneous Schottky diodes at low temperatures. Semicond Sci Technol, 2004, 19: 82

[7] Mantas P Q, Baptista J L. The barrier height formation in ZnO varistors. Journal of the European Ceramic Society, 1995, 15: 605

[8] Liu Enke, Zhu Bingsheng, Luo Jinsheng. Semiconductor physics. 3rd ed. Beijing: National Defense Industry Press, 1994: 241 (in Chinese)

[9] Kang Xiaohu, He Shanhu, Sang Baosheng. Electrical properties and annealing effects of MZOS structure. Chinese Journal of Semiconductors, 1997, 18(12): 926 (in Chinese)

[10] Liu Cihui, Liu Bingce, Fu Zhuxi. Electrical and deep levels characteristics of ZnO/Si heterostructure by MOCVD deposition. Chinese Physics B, 2008, 17(5): 2292

[11] Tuller H L. ZnO grain boundary: electrical activity and diffusion. Journal of Electroceramics, 1999, 4(Suppl 1): 33

[12] Fan J, Freer R. Deep level transient spectroscopy of zinc oxide varistors doped with aluminum oxide and/or silver oxide. Journal of the American Ceramic Society, 1994, 77(10): 2663

[13] Liu Cihui, Xu Xiaoqu, Zhong Ze. Donor-acceptor luminescence in ZnO:LiCl/p-Si films. Chinese Journal of Semiconductors, 2007, 28(suppl): 171 (in Chinese)

[14] Aankaya G C, Abay B. Current–and capacitance–voltage characteristics of Cd/p-GaTe Schottky barrier diodes under hydrostatic pressure. Semicond Sci Technol, 2006, 21: 124