A low power 12-b 40-MS/s pipeline ADC*

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Abstract: This paper describes a 12-bit, 40-MS/s pipelined A/D converter (ADC) which is implemented in 0.18-μm CMOS process drawing 76-mW power from 3.3-V supply. Multi-bit architectures as well as telescopic operational transconductance amplifiers (OTAs) are adopted in all pipeline stages for good power efficiency. In the first two stages, particularly, 3-bit/stage architectures are used to improve the ADC's linearity performance. The ADC is calibration-free and achieves a DNL of less than 0.51 LSB and an INL of less than 1 LSB. The SNDR performance is above 67 dB below Nyquist. The 80-dB SFDR performance is maintained within 1 dB for input frequencies up to 49 MHz at full sampling rate.

Key words: analog-to-digital converter; A/D converter; pipeline; telescope OTA; low power; high linearity
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1. Introduction

12-bit 40-MS/s analog-to-digital converters (ADCs) are used in many applications ranging from medical imaging and optical networking to wireless receivers. These applications pose challenges on the design of ADCs. Taking a software-defined radio (SDR) receiver as an example[1], in order to support multiple communication standards for various frequencies, the ADC should have a wide input bandwidth, an excellent sub-sampling performance, a high linearity performance, as well as low power and a small area. Compared with 10-bit ADCs, 12-bit ADCs can evidently relax the requirement of analog channel filters for receiver systems. Furthermore, the system would gain more tolerance on interference from the high linearity performance of the ADC[2].

This paper presents a 12-bit 40-MS/s pipelined A/D converter demonstrating 80-dB SFDR maintained within 1 dB for input frequencies up to 49 MHz without trimming or calibration. The fundamental objective is to develop an efficient (compact and low power) ADC architecture optimized for SFDR. The requirement of improving the linearity performance is achieved by adopting a 3-bit/stage architecture in the first two stages and careful design of circuit elements. We discuss the architecture considerations for the ADC, and describe circuit implementation details.

2. Architectural considerations

In the proposed design, a pipeline ADC is selected for sufficient trade-off between speed, resolution and power. A sample-and-hold amplifier (SHA) is set at the front-end of the ADC for sub-sampling performance consideration, while multi-bit/stage architectures are chosen for good power efficiency. Figure 1 shows the main part of the ADC, which consists of an SHA, two 3-bit stages, and three 2.5-bit stages followed by a 3-bit flash converter. This gives a total of 13 internal bits out of the digital error correction block, of which only 12 bits are used.

2.1. S/H stage

The architecture of SHA is shown in Fig. 2, in which a flip-around topology is used for low noise and low power consideration[3]. The amplifier in SHA is a folded-cascode OTA which enables large input common-mode compliance to track differential inputs with various common modes as well as single-ended inputs. As shown in Fig. 2, the input voltage is sampled on capacitor C_S at the end of the sample phase Φ_{2e}. During the hold phase Φ_1, the voltage on the top plate of C_S is transferred to the SHA output, which is sampled by the next stage at the falling edge of Φ_{1e}. Bootstrapped switches are used on the sampling paths to reduce input-dependent signal distortion caused by on-resistance non-linearity of MOS switches.

2.2. Multi-bit pipeline stages

For pipelined ADC resolution above 10-bit, multi-bit topology is becoming popular from power and area perspective[4−7].

One of the most important design considerations of switched capacitor (SC) circuits is the size of capacitors, which constraints the noise performance, power consumption and chip area. For SC pipelined ADC resolution below 12 bits, compared with the thermal noise parameter caused by KT/C and the OTAs, the cap mismatch parameter is more crucial when determining the size of the sampling capacitors. For an N-bit pipeline ADC, the requirement of capacitor matching accuracy for the n-bit first stage is $(N-n)$-bit. Since capacitor mismatch is inversely proportional to the square root of the total capacitance value, the whole size of the capacitors in the first stage MDAC of a 2.5-bit topology is only half of the 1.5-bit one for a 12-bit pipelined ADC.

The reduction of capacitor size evidently decreases the area of a 2.5-bit stage. With decreasing capacitive load, the amplifier in a 2.5-bit stage is more feasible and power economical. Finally, the 2.5-bit/stage structure benefits more power and area advantage from stage number reduction.

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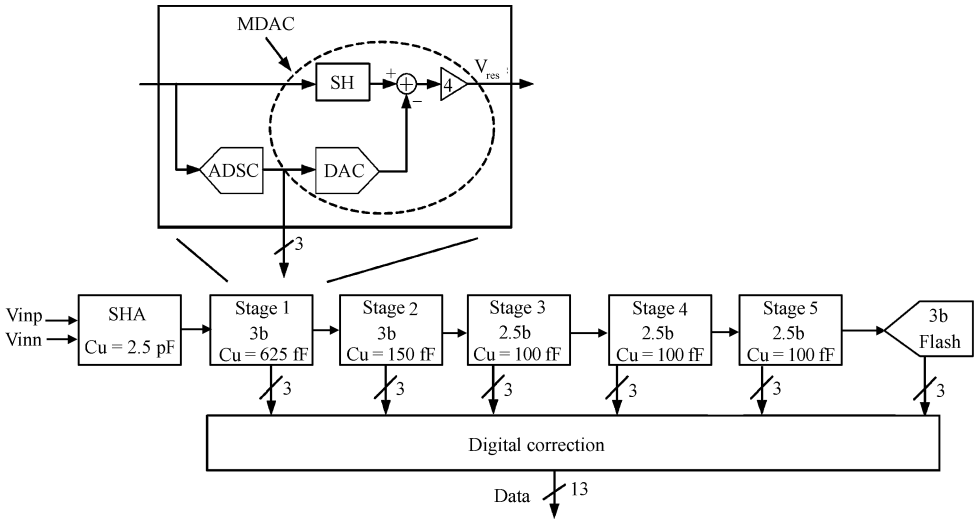

Fig. 1. Proposed ADC architecture.

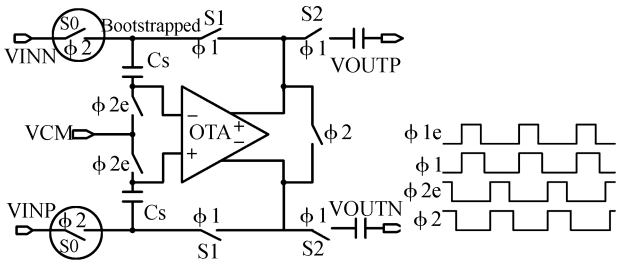

Fig. 2. SHA architecture.

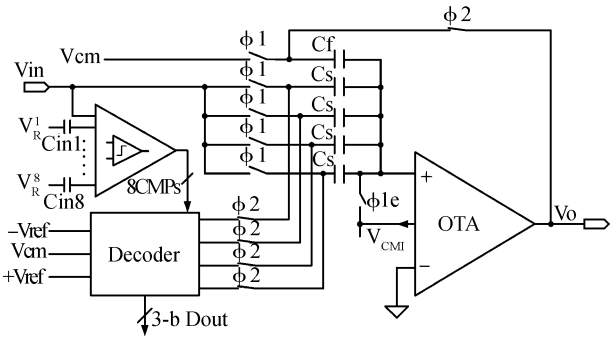

Fig. 3. Architecture of a 3-bit MDAC.

2.3. The first two 3-bit stages

In this design, 3-bit MDACs are used in the first two stages to enhance the linearity performance[4, 6, 7].

Figure 3 shows the architecture of a 3-bit MDAC in the first stage of ADC. Only a single-ended version is represented for simplicity, although the implementation is fully differential. During the track phase Φ_1, both capacitors C_s and $C_{in1...8}$ are charged and tracking the input voltage. Then in the non-overlapping phase between Φ_1 and Φ_2, digital outputs of the eight comparators are transferred to the decoder block. According to the decoder outputs, one of the voltage references ($-V_{ref}$, V_{cm} and V_{ref}) is chosen and fed to the bottom plate of each sampling capacitor (C_s) during the amplification phase Φ_2. At the same time, the OTA outputs are connected to the bottom plate of the feedback capacitors C_f, producing the residue output voltage, which is sampled by the next stage at the falling edge of Φ_{2e}. Both C_s and C_f have the same value, which gives a residue gain of four.

The transfer characteristics of a 3-bit stage and a 2.5-bit stage are shown in Fig. 4. The main difference occurs at the end of the curves. The 3-bit transfer line folds at input voltages of $-7/8\ V_{ref}$ and $7/8\ V_{ref}$, while the 2.5-bit one does not. This gives two advantages for the 3-bit stage. First, the residue voltage output of the 3-bit stage is only half of the 2.5-bit one, which enables relaxation of the OTA output swing requirement. Second, the low output range of the 3-bit stage significantly suppresses the third-order gain compression error, improving the

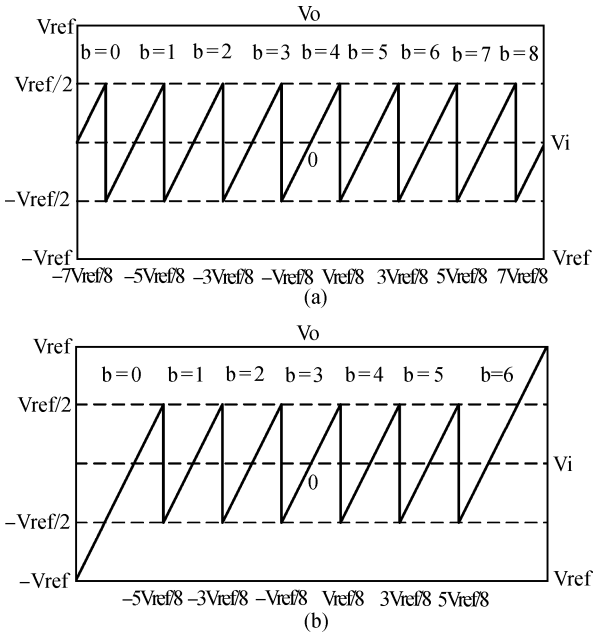

Fig. 4. Transfer characteristic of (a) 3-bit stage and (b) 2.5-bit stage.

ADC linearity performance. The main reason is that the third-order harmonic distortion (HD3) of stage gain nonlinearity due

to the OTA input pair's transconductance is proportional to the OTA output signal swing (V_{sig}) squared, and the third-order nonlinearity at the OTA's output node also tends to increase with V_{sig}[8].

The only disadvantage of a 3-bit stage is that the MDAC feedback factor is lower than a 2.5-bit one and two more comparators are required, which would increase a small quantity of power dissipation.

3. Circuit design of the ADC

The most power hungry elements of a pipelined ADC are the amplifiers. Therefore it is important to decrease the power consumption of them. The main design technique to maximize the power efficiency is the selection of gain-boosted single-stage telescope architecture as the main OTA structure. In addition, the OTA bias circuits generate the MDAC input common-mode voltage (V_{cmi}), which enables the omission of the external V_{cmi} buffer for further power reduction.

In a 12-bit pipelined ADC, the 2.5-bit topology has more of a power advantage than the 1.5-bit one. However, less comparator-offset tolerance is one of the disadvantages. In the proposed design, the sampling sequence of sub-ADCs is improved to alleviate this problem.

3.1. Operational transconductance amplifiers (OTAs)

High-resolution MDACs sampling at high clock speeds need high DC-gain OTAs. In general, a single stage telescopic OTA offers excellent bandwidth with less power consumption at the cost of reduced signal swing range compared with other types of OTAs[9]. Figure 5 shows the main structure of the gain-boosted single-stage telescoped OTA. With a 3.3-V supply, the peak-to-peak differential output signal swing can be as high as 2.0 V. The current consumption of the main OTA in the first stage is 1.5-mA, while for the subsequent stages this is scaled down.

Figure 6 shows the OTA bias circuit that generates the MDAC input common-mode voltage (V_{cmi}), which is first shown in Fig. 3. During the sampling and amplifying phases, the common-mode voltage of both the bottom and top plates of the sampling capacitors maintain unchanged, thus the top plates of the sampling capacitors (C_s) seldom take any current from the V_{cmi} buffer. Therefore, the V_{cmi} voltage can be generated by the OTA bias circuit, which enables the omission of the external common-mode voltage buffer and further enhances the power efficiency. As shown in Fig. 6, the V_{cmi} voltage is generated at the drain/gate of transistor MBIN5, and can be calculated as

$$V_{cmi} = V_{DS(BN3)} + V_{GS(BN5)} = V_t + 2V_{ov}. \quad (1)$$

This provides another advantage that V_{cmi} voltage tracks the corner, temperature as well as supply variation, keeping the OTA input transistors working in saturation region.

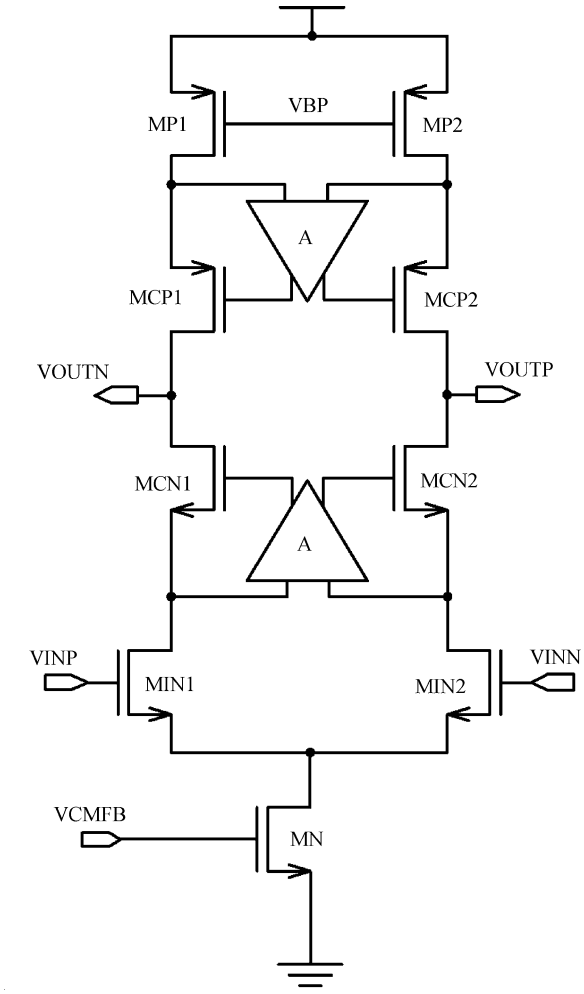

Fig. 5. Telescope OTA with gain-boosters.

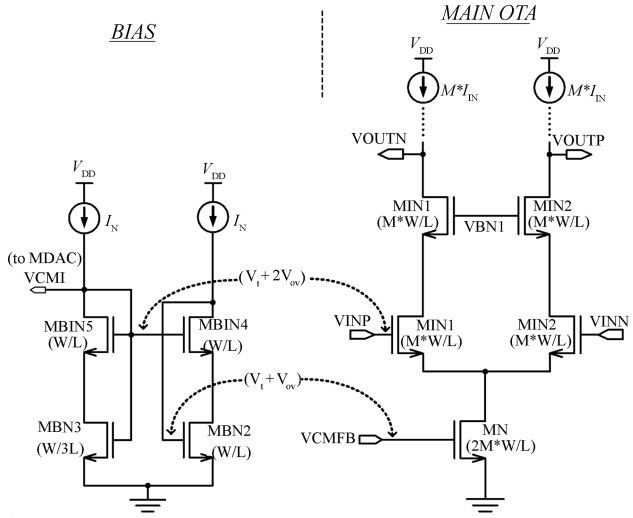

Fig. 6. OTA bias circuit which generates V_{cmi}.

3.2. Sub-ADC design

The comparators in the sub-ADC have three stages, a pre-amplifier, a latch and an output stage, as shown in Fig. 7. The pre-amplifier amplifies the differential voltages during the tracking phase, and applies it to the latch. Then at the falling edge of clk_L, the latch generates the output and feeds it to the output stage, which ultimately generates CMOS levels and drives the digital logic gates in the decoder block of Fig. 3.

As shown in Fig. 8, the reference voltages (V_R^1 to V_R^8) of each sub-ADC unit are generated by a series of resistors. During the hold phase Φ_2, the comparator pre-amplifier is con-

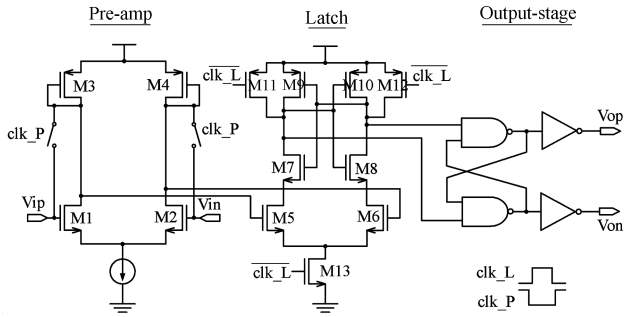

Fig. 7. Comparator circuit design.

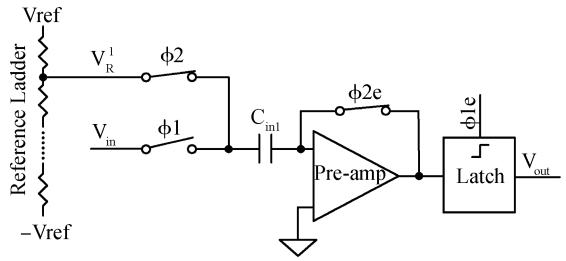

Fig. 8. One unit of the sub-ADC in the first stage.

nected as a unit-gain buffer, and its output equals the offset voltage of the input transistors (M1 and M2). When the reference voltage V_{R1} is sampled on the bottom plate of capacitor C_{in1}, the offset of M1 and M2 is stored on the top plate of it. During the next clock phase Φ_1, the bottom plate of C_{in1} tracks the input signal (V_{in}), while the top plate of it makes a subtraction between V_{in} and V_R^1. At the same time, the input offset of comparator pre-amplifier is cancelled.

4. Implementation and measured results

The ADC is fabricated in a 1P6M 0.18-μm CMOS process with a core area of 1.4×2.1 mm^2. Figure 9 presents the die photograph, while Figure 10 shows the measured static performance. The ADC differential nonlinearity (DNL) and integral nonlinearity (INL) are less than 0.51 LSB and 1 LSB respectively. Figure 11 shows measured spectrum for the input frequencies of 19.1 and 49.1 MHz. The ADC achieves more than 67-dB SNDR and above 80-dB SFDR performance with Nyquist input at full sampling rate. In Fig. 11, SFDR performance is 0.3 dB higher for 49.1-MHz input than for 19.1-MHz one. This is because the LC bandpass filters used for input signal filtering in ADC test have better linearity performance at higher frequency. As indicated in Fig. 12, the ADC dynamic performance remains relatively constant at 40-MS/s sampling rate for input frequencies up to 49.1 MHz, which is over twice the Nyquist. Table 1 summarizes the ADC performance. The total power consumption of ADC core is 76 mW at 3.3-V supply. To evaluate the efficiency of the ADC, the figures of merit (FOMs) are calculated by

$$\text{FOM1} = \frac{\text{Power}}{10^{\text{SNDR}/20} \times 2 \times \text{BW}}, \tag{2}$$

$$\text{FOM2} = \frac{\text{Power}}{10^{\text{SFDR}/20} \times 2 \times \text{BW}}, \tag{3}$$

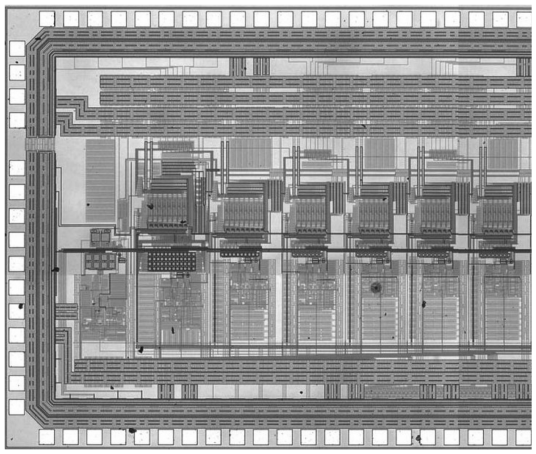

Fig. 9. Die photograph of the ADC.

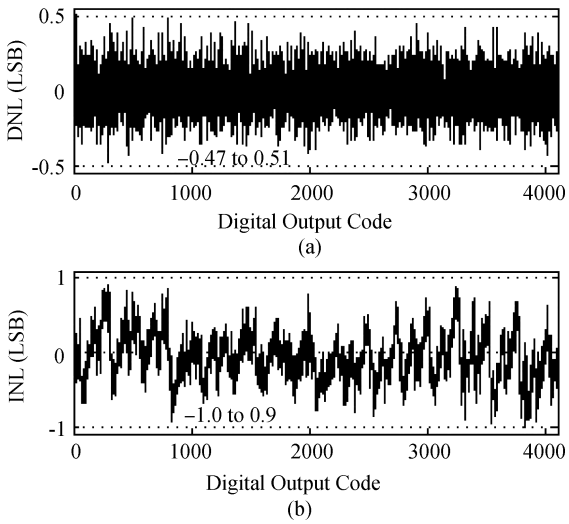

Fig. 10. Measured static performance of ADC. (a) DNL. (b) INL.

Table 1. Summary of measured performances.

Parameter	Value
Technology	0.18-μm CMOS
Conversion rate	40 MHz
Resolution	12 bit
Total power	76 mW @ 3.3V supply
Core area	1.4×2.1 mm^2
DNL, INL	–0.47 to 0.51, –1.0 to 0.9
SFDR	80.21 dB (f_{in} = 19.1 MHz)
	80.54 dB (f_{in} = 49.1 MHz)
SNDR	67.28 dB (f_{in} = 19.1 MHz)
	63.21 dB (f_{in} = 49.1 MHz)
SNR	68.28 dB (f_{in} = 19.1 MHz)
	63.56 dB (f_{in} = 49.1 MHz)
ENOB	10.88 (f_{in} = 19.1 MHz)
	10.21 (f_{in} = 49.1 MHz)

where SNDR is the signal-to-noise-plus-distortion ratio, SFDR is the spurious-free- dynamic-range, and BW is the bandwidth of the input signal over which the used SNDR and SFDR value holds. The power used in this calculation is the total power. Obviously, the smaller the FOM, the more efficient the ADC is[7]. Although the FOM1 formula tends to be more commonly

Table 2. Comparison of performance on several ADCs with similar resolution.

	This work	JSSC01[10]	JSSC05[11]	JSSC07[12]	JSSC09[13]	AD9229[14]
Bits	12	12	12	12	12	12
MS/s	40	54	110	75	200	50
Power (mW)	76	295	97	273	348	246
VDD (V)	3.3	2.5	1.8	3	1.2	3
DNL/INL	0.51/1	1.1/1.7	1.2/1.5	0.64/0.95	0.78/1.7	0.3/0.4
SFDR (dB)	80.21	75	64	71.2	—	85
SNDR (dB)	67.28	64	59	63.5	62	69.5
V_{in} (MHz)	19.1	1	50	37.5	91	25
Technology	0.18 μm	0.25 μm	0.18 μm	0.35 μm	90 nm	—
FOM1 (pJ/step)	0.82	3.4	0.99	2.4	1.4	1.65
FOM2 (pJ/step)	0.19	0.97	0.56	1.0	—	0.28

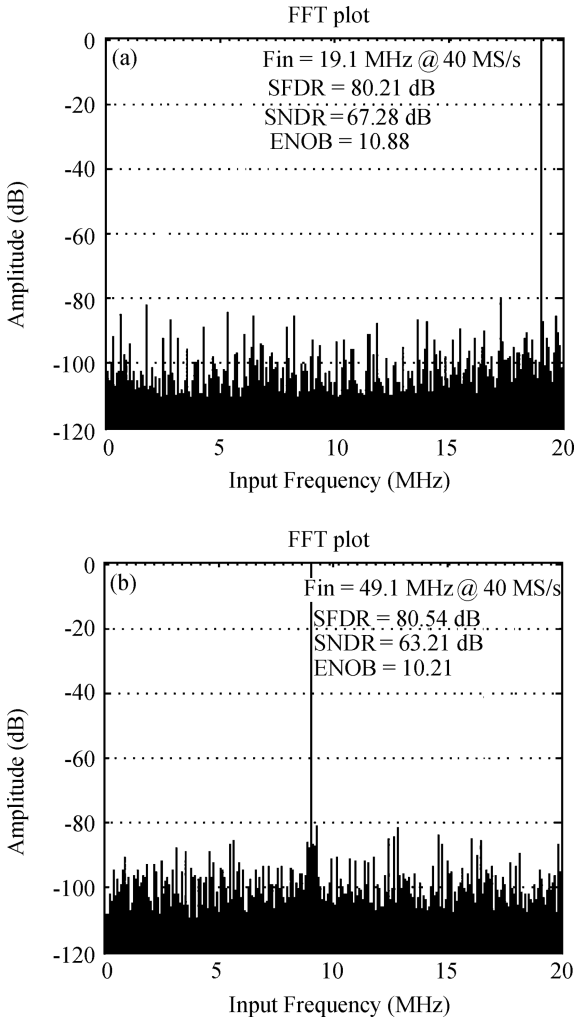

Fig. 11. Measured dynamic performance of ADC with (a) 19.1-MHz input and (b) 49.1-MHz input.

used[7, 8], FOM2 is more technically for the high resolution high speed ADCs, because the linearity is far more important than SNDR due to the application that they are used within. Table 2 shows the comparison of performance on several ADCs with similar resolution. In order to have a fair comparison, only 12-bit ADCs are compared, among which the presented ADC is the only dual-gate high-supply design. As shown in Table 2, the presented ADC achieves the best trade-off between power and performance, for both SNDR and SFDR perspective.

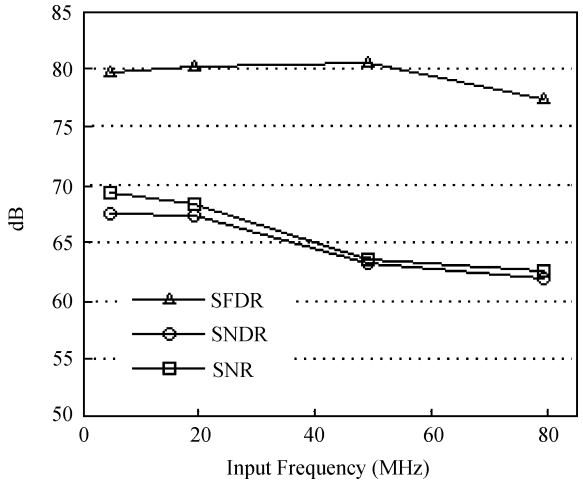

Fig. 12. Measured dynamic performance versus input frequency at 40-MHz sampling rate.

5. Conclusion

This paper describes a 12-bit 40-MS/s pipelined ADC. It achieves a low frequency SFDR of over 80 dB, and preserves a 12-bit level of performance for input frequencies up to 79.1 MHz without calibration. This is enabled by using a wide-band SHA and applying a 3-bit topology in the first two stages. The power consumption is 76 mW with a 3.3-V power supply, which is comparably low among pipelined ADCs with moderate resolution and speed.

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