Low-power switched-capacitor delta–sigma modulator for EEG recording applications*

Chen Jin(陈进)†, Zhang Xu(张旭), and Chen Hongda(陈弘达)

(State Key Laboratory of Integrated Optoelectronics, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)

Abstract: This paper presents a third-order single-loop delta–sigma modulator of a biomedical micro-system for portable electroencephalogram (EEG) monitoring applications. To reduce the power consumption, the loop filter of the proposed modulator is implemented by applying a switched-capacitor structure. The modulator is designed in a 0.35-μm 2P4M standard CMOS process, with an active area of 365 $\times$ 290 μm^2. Experimental results show that this modulator achieves a 68 dB dynamic range with an input sinusoidal signal of 100 Hz signal bandwidth under a 64 over-sampling ratio. The whole circuit consumes 515 μW under a 2.5 V power supply, which is suitable for portable EEG monitoring.

Key words: analog-to-digital converter; delta–sigma modulator; EEG; switched-capacitor circuit
DOI: 10.1088/1674-4926/31/7/075009 **EEACC:** 2570

1. Introduction

There is an increasing trend of using portable or even wearable low-power equipments to sense the biophysiological signals, such as EEG, ECG and EMG[1, 2]. Some prototype integrated circuits with the capability of capturing biopotentials have been used in clinical monitor and physiological research[3]. As the interface between analog front-end and digital back-end in these integrated systems, analog-to-digital converter (ADC) plays a critical role for bio-signals' further analysis and transmission. A robust ADC with the properties of low power consumption and high resolution is quite required.

A wide variety of ADCs with low power consumption and high resolution have been previously reported[4, 5]. However, most of them are not EEG oriented. Therefore, it is not power efficient when using them in EEG monitoring systems. The EEG signals have a small dynamic range (0.1–20 μV) and low signal frequency (0.5–100 Hz)[6]. If we use traditional ADC to handle EEG signals, a sampling & holding (S & H) circuit with high performances is needed. This will increase the power consumption of the EEG monitoring system. In addition, we need an anti-aliasing filter with high performances to avoid aliasing noise or out-of-band signals into the signal bandwidth during the sampling operation. This will further increase the power consumption of the EEG monitoring system. In this paper, we use a delta–sigma ADC to replace the traditional ADC. The delta–sigma ADC consists of a front-end modulator and a back-end digital filter. The front-end modulator is integrated into the EEG monitoring system. While the back-end digital filter is implemented by software. In addition, as the delta–sigma modulator adopts over-sampling technology and quantization noise repressing technology, the requirements of the anti-aliasing filter and S & H circuit are greatly released. The power consumption of the whole system is reduced.

This paper is organized as follows. Section 2 introduces the system design of the EEG front-end system. Section 3 describes the implementation of the modulator including the design of each sub-module. In section 4, the experimental results are given. The conclusions are drawn in section 5.

2. System design

The EEG signals usually suffer from some unwanted signals, which include the power line interference and the DC drift from the electrode-electrolyte interface. These issues complicate the task of designing an EEG monitoring system. One solution is to digitize the EEG signals and the unwanted signals together, and then remove the unwanted signals digitally. This solution requires ADCs with resolutions of over 20 bits, which would complicate the design of ADCs and lead to high power consumption. Another strategy is to filter out the unwanted sig-

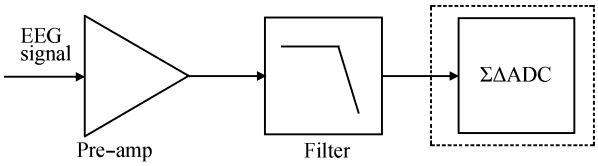

Fig. 1. Front-end for EEG monitoring system.

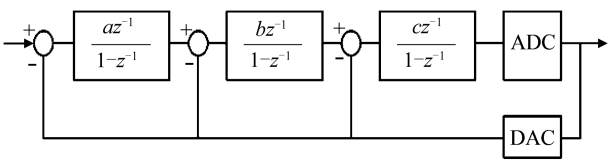

Fig. 2. Third-order single-loop discrete time DSM.

* Project supported by the National Natural Science Foundation of China (Nos. 60776024, 60877035, 90820002, 60976026) and the National High Technology Research and Development Program of China (Nos. 2007AA04Z329, 2007AA04Z254).
† Corresponding author. Email: chenjin@semi.ac.cn
Received 18 September 2009, revised manuscript received 7 February 2010

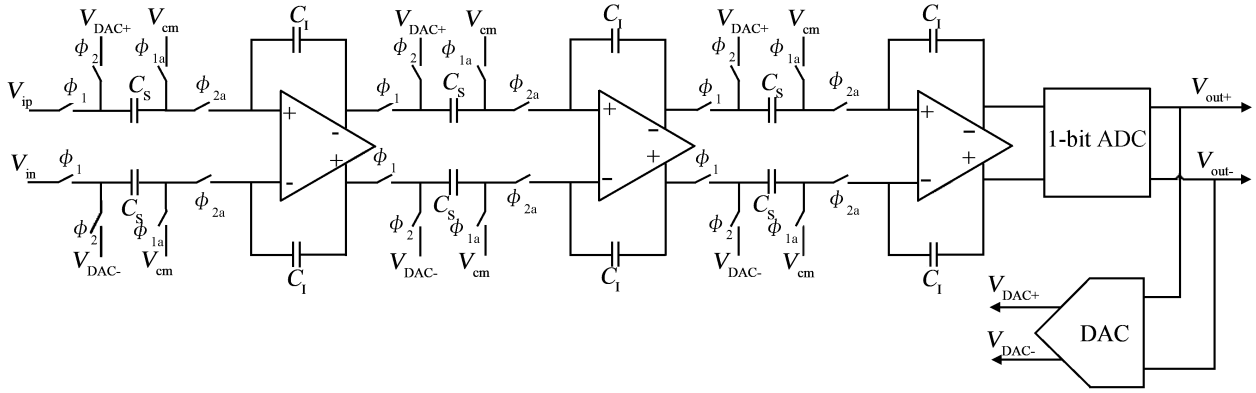

Fig. 3. Switched-capacitor implementation of third-order single-loop DSM.

nals with a bandpass pre-amplifier before digitizing[2]. This method will relax the requirements of the ADCs, although a robust preamplifier with low-frequency poles is difficult to realize on-chip. Preamplifier has been reported in previous paper[7].

Figure 1 shows the basic block diagram of the front-end for an EEG monitoring system. The pre-amplifier provides a gain of 40 dB to amplify the weak EEG signal and filters out the unwanted signals. The anti-aliasing filter is used to avoid aliasing noise or out-of-band signals into the signal bandwidth during the sampling operation. If the sampling frequency of the following ADC is set high, the anti-aliasing filter is not necessary. In order to improve the power efficiency, switched-capacitor (SC) technology is adopted.

The block diagram of the third-order single-loop modulator is shown in Fig. 2. The advantages of this topology are simplicity and low sensitivity to device mismatch.

The noise transfer function of L-th order delta–sigma modulator is expressed by

$$H_{\mathrm{e}}(z) = \frac{1}{1 + \sum_{i=1}^{L} \prod_{j=1}^{L} a_j k \left(\dfrac{z^{-1}}{1 - z^{-1}} \right)^{L-i+1}}$$

$$\Rightarrow |H_{\mathrm{e}}(z)| \approx \frac{\left|1 - z^{-1}\right|^{L}}{\prod_{i=1}^{L} a_j k} . \qquad (1)$$

From Eq. (1), the larger product of the integrator parameters can decrease in-band noise power, which leads to a high signal-to-noise ratio (SNR). However, increasing the integrator parameters deteriorates the stability of the modulator. Therefore, the combination of the parameters should be optimized to obtain a maximal dynamic range (DR).

In order to improve DR, fully-differential circuits and double polarity reference voltages are chosen[8]. Optimization of the integrator parameters has been made in previous work[9]. However, the actual integrator parameters may be larger or smaller than the designed value due to capacitor mismatch. A larger actual value could improve the in-band noise power but degrade the stability, or vice versa. Assuming 1% capacitor mismatch which is modest in modern technology, system simulations have been performed using MATLAB/SIMULINK based on models in Refs. [9, 10]. Integrator parameters have been chosen as $a = 0.25$, $b = c = 0.5$.

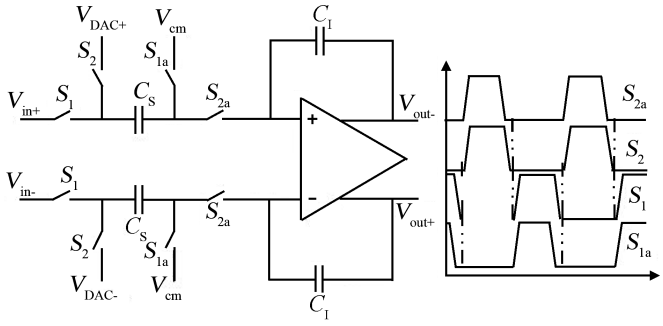

Fig. 4. SC integrator.

3. Modulator implementation

Figure 3 shows the implementation of the modulator in Fig. 2. The architecture is composed of three SC integrators, a 1-bit ADC and a 1-bit DAC. Fully differential topology with double polarity reference voltages are chosen to increase the signal to white noise ratio ($\mathrm{SNR}_{KT/C}$) by 6 dB[8].

3.1. Integrators

As shown in Fig. 4, integrator is implemented by SC structure in order to lower power consumption. S_1 and S_2 are two non-overlapped clocks. $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ are advanced than S_1 and S_2 respectively. As the desired signal bandwidth is only 100 Hz, flicker noise is the dominant noise source. Correlated double sampling (CDS) integrators can be used to shape the flicker noise out of the signal band[11]. Increasing the transistors' dimension of the amplifier is another method to reduce the effect of flicker noise. In this paper, the later one is adopted.

In order to reduce the effects caused by the non-ideal behaviors of switches such as charge injection and clock feedthrough, several technologies have been adopted[11]. Advanced falling of $S_{1\mathrm{a}}$ and $S_{2\mathrm{a}}$ can reduce the effect of charge injection. Switches of S_1, S_2 and $S_{2\mathrm{a}}$ are implemented by complementary PMOS and NMOS which can reduce the effect of charge injection and the loss of signal passing through switches. Switch $S_{1\mathrm{a}}$ is compensated by a dummy switch with the same gate length and half gate width to reduce the charge in-

Table 1. Capacitor value for each integrator.

Integrator	C_S/C_I
Integrator 1	500 fF / 2 pF
Integrator 2	500 fF / 1 pF
Integrator 3	500 fF / 1 pF

jection and clock feedthrough. In addition, "bottom-plate sampling"[11] technology is adopted to minimize parasitic capacitance which deteriorates the performance of integrator.

Using small sampling and integrating capacitor can reduce power consumption and improve the frequency characteristic of amplifier. However, the minimum capacitor size in SC circuit is limited by either KT/C noise or the capacitor mismatch.

The input-referred noise of the circuit in Fig. 4 is expressed by[12]

$$N_{\text{in}} = \frac{N_{\text{in},1}}{M} + \frac{\pi^2 N_{\text{in},2}}{a^2 \cdot 3M^3} + \frac{\pi^4 N_{\text{in},3}}{a^2 b^2 \cdot 5M^5}, \tag{2}$$

$$N_{\text{in},i} = \frac{4KT}{C_{Si}}, \quad i = 1, 2, 3, \tag{3}$$

where $N_{\text{in},1}$, $N_{\text{in},2}$ and $N_{\text{in},3}$ are the input-referred noise power of the first, second and third integrator, respectively. M is the over-sampling ratio. When $M = 64$, $a = 0.25$ and $b = 0.5$, the background noise over the bandwidth of the second and third integrators is attenuated by 2×10^{-4} and 1.16×10^{-6}, respectively. Therefore, the noise floor is mainly determined by the first integrator sampling capacitance.

For the first integrator of this modulator, the SNR due to KT/C noise can be written as[8]

$$\text{SNR}_{KT/C} = \frac{(2 \cdot \text{OL} \cdot V_{\text{ref}})^2}{2} \frac{C_S R}{4kT}, \tag{4}$$

where OL represents the overload level of the modulator, and V_{ref} is limited by the output swing of the integrator. Since the circuit operates from a 2.5 V supply, V_{ref} is 0.5 V with an output swing of 2 V (differentially) for the integrator. From Eq. (4), using a 125 fF sampling capacitor, $\text{SNR}_{KT/C}$ can reach to 83.8 dB theoretically enough for the required resolution of 10-bit. In order to provide an enough margin, the first sampling capacitor is set to be 500 fF. The second and third sampling capacitances are determined by matching considerations. In this paper, they are the same as the first sampling capacitance to simplify the layout design. The integrating capacitances of the first, second and third integrators are calculated by their integrating parameters. The chosen value of each capacitance is listed in Table 1.

3.2. Amplifier

Amplifier is the most important component in SC integrator. Considering the influences of finite gain of the amplifier, transfer function of the integrator is approximated as[8, 13]

$$H(z) = \frac{C_S}{C_I} \frac{r_2 z^{-1}}{1 - r_1 z^{-1}}, \tag{5}$$

$$r_1 = \frac{1 + A + C_P/C_I}{1 + A + C_S/C_I + C_P/C_I}, \tag{6}$$

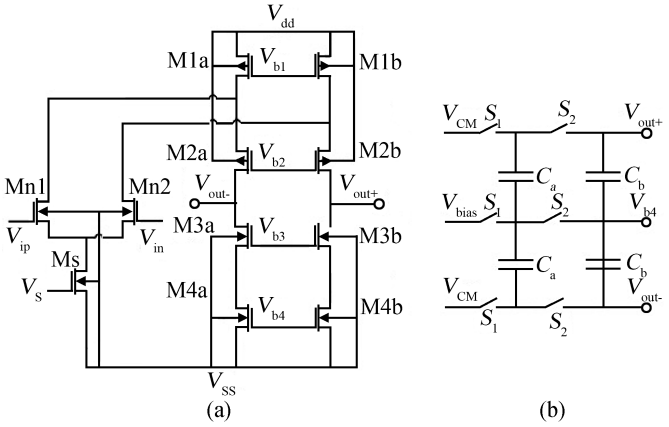

Fig. 5. Amplifier used in SC integrator. (a) Amplifier. (b) CMFB.

$$r_2 = \frac{A}{1 + A + C_S/C_I + C_P/C_I}, \tag{7}$$

where C_P is the parasitic capacitance at the input, A is the open-loop gain of the amplifier. Using Eqs. (5)–(7), simulations are performed using SIMULINK/MATLAB based on models in Ref. [14]. A gain of 60 dB is sufficient. In order to provide a safety margin, 70 dB is selected.

Considering the influences of the finite gain-bandwidth product (GBW) of the amplifier, transfer function is written as[8, 13]

$$H(z) = \frac{C_S}{C_I} \frac{r_2(1-k)z^{-1}}{1 - r_1(1 - k(1 - r_1))z^{-1}}, \tag{8}$$

$$k = \exp \frac{-g_m \tau_2}{(C_S + C_P + (C_S + C_P + C_I)\, C_L/C_I) r_2}, \tag{9}$$

where τ_2 represents the time available for settling during the integrating phase. For clock frequency of 16 kHz used in this modulator, GBW of 100 kHz is enough. We selected 200 kHz in order to provide an enough margin.

In order to associate high gain and low power consumption, a fully differential folded-cascode topology is selected. The schematic is shown in Fig. 5(a). The circuit of common feed-back (CMFB) is implemented by SC circuit in order to reduce power consumption[15]. However, it affects the frequency characteristic of the amplifier. Considering the effect of CMFB, the load capacitance of the amplifier is $C_I + C_S + C_b$ at the sampling stage. While at the integrating stage, the load capacitance is $C_I + C_S + C_b + C_a$. Details about the design of the amplifier have been presented in Refs. [11, 13]. Consider an amplifier in the feedback configuration shown in Fig. 6 which corresponds the charge transfer phase of the SC integrator. C_P is the parasitic input capacitor. The response of an OPA includes a slew rate limited region T_{SL} followed a linear response region T_{Lin}. Using the method in Ref. [12], we can get the expression of I_1.

$$I_1 = \frac{2Mf_N C_I (C_S + C_P)}{C_I + C_S + C_P} \left[\frac{C_S}{C_I} (V_{SW} - V_{ref}) - (V_{GS1} - V_{T1}) \right] + Mf_N (\ln 2 + \ln DR)(C_S + C_P)(V_{GS1} - V_{T1}), \tag{10}$$

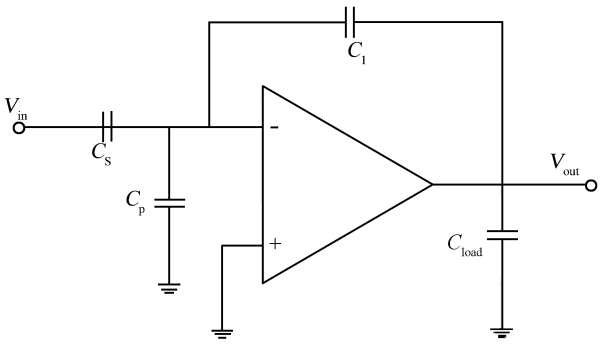

Fig. 6. OPA with capacitive feedback.

where V_{SW} is the final value of the output. In order to minimize τ, C_P should be approximately equal to C_S[12]. Therefore,

$$V_{GS1} - V_{T1} = \frac{2L_1^2}{3u_N}\frac{I_1}{C_S - C_{W1}}, \tag{11}$$

$$(V_{GS1} - V_{T1})_{min} \leqslant V_{GS1} - V_{T1} \leqslant (V_{GS1} - V_{T1})_{max}, \tag{12}$$

where C_{W1} represents wiring parasitic. In order to find the minimum current I_1 we can first choose an arbitrary value for I_1. Then compute $V_{GS1} - V_{T1}$ through Eq. (11) which should be satisfied with Eq. (12). Through Eq. (10), we can compute the value of I_1 which should be consistent with the chosen value of I_1. Otherwise, we increase the value of I_1 and repeat the steps above.

From Ref. [12], we know that

$$\tau_2 \leqslant \frac{(C_s + C_p)(V_{GS1} - V_{T1})}{I_1}, \tag{13}$$

$$\tau_2 = \frac{C_2}{g_{m2}} = \frac{C_2(V_{GS2} - V_{T2})}{2I_2}, \tag{14}$$

$$C_2 = \frac{2L_{2a}^2}{3u_p}\frac{I_2}{V_{GS2} - V_{T2}} + \frac{2I_2L_{1a}}{u_pC_{OX}(V_{GS1a} - V_{T1a})^2}C_{DBT} + \frac{2I_1L_1}{u_pC_{OX}(V_{GS1} - V_{T1})^2}C_{DBT} + C_{w2}, \tag{15}$$

where C_{W2} represents the wiring parasitic at the source of the transistor $M_{2a,b}$. In order to find the minimum value of I_2, we can first set $I_2 = I_1/2$. Then compute the value of τ_2. If the constraint of Eq. (13) is satisfied, the iteration is completed. Otherwise, the value of I_2 is increased and steps above are repeated.

When all the iterations are completed, the power consumption of the amplifier $P = (2I_1 + 2I_2)V_{DD}$ is optimized. In this design, the achieved output swing is 2 V (differentially) with a gain of 72 dB. The GBW of this amplifier is approximately 1 MHz. The power consumption is 44.2 μW.

3.3. 1-bit ADC and 1-bit DAC

The 1-bit ADC has been implemented using the architecture illustrated in Fig. 7(a). This is a latched comparator with power consumption of 1 μW. Each output of the comparator is followed by an inverter to enhance the driving ability. The schematic of DAC is shown in Fig. 7(b).

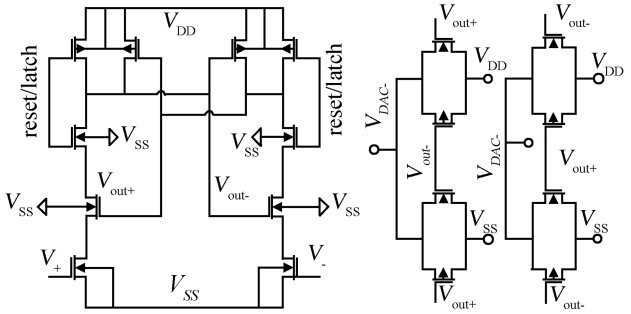

Fig. 7. ADC and DAC. (a) Latched comparator. (b) DAC.

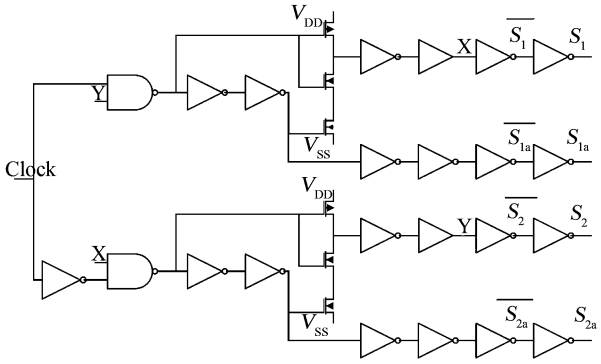

Fig. 8. Schematic of clock driver.

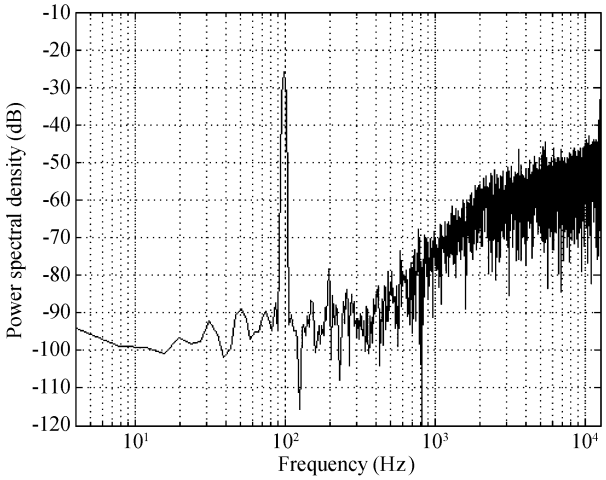

Fig. 9. Output spectral with a sinusoidal input.

3.4. Clock driver

The schematic of the clock driver is depicted in Fig. 8[8]. S_1 and S_2 have a non-overlapping interval of 8 ns. The clock for the latched comparator is obtained by delaying the S_2. During the delay, integrators can get stable

4. Experimental results and discussions

The modulator was driven by a 16 kHz clock. The output bit stream was recorded by FPGA and then processed off-line by MATLAB. The fast Fourier transformation with 8192 points and the Hanning window were applied. Figure 9 shows the output spectrum density of the modulator for a sinusoidal input

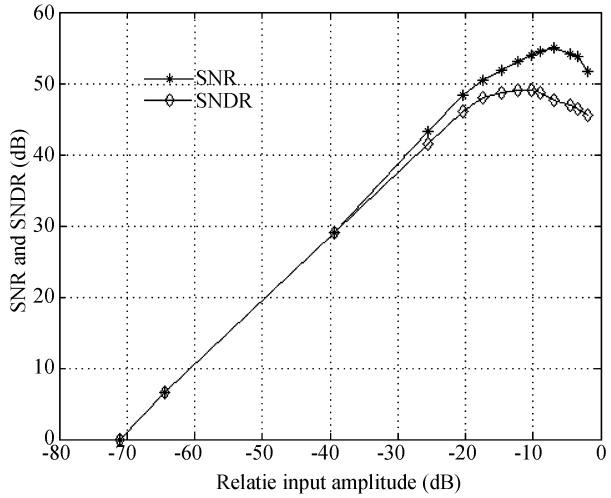

Fig. 10. SNR & SNDR versus the normalized input.

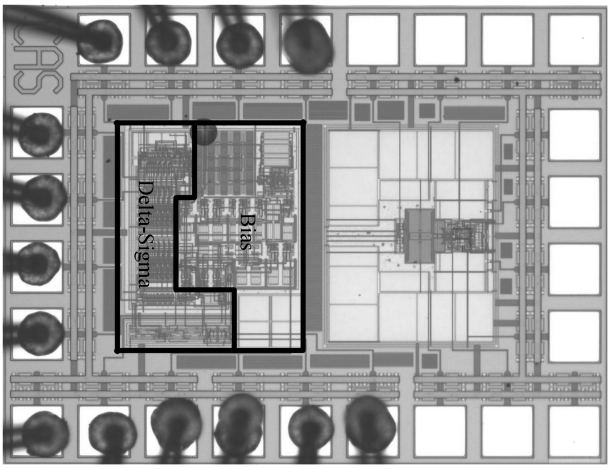

Fig. 11. Chip microphotograph.

signal of 100 Hz and 210 mV amplitude. The sampling frequency is 16 kHz. Figure 10 shows the SNDR and signal-to-noise ratio (SNR) versus the input amplitude normalized by 2.5 V. It can be seen that the modulator achieves a dynamic range (DR) of 67.5 dB, a peak SNR of 55.03 dB and a peak SNDR of 49.01 dB. The effective number of bits (ENOB) is 8.

Figure 11 shows the microphotograph of the chip of the front-end system for EEG monitoring applications. The annotated part contains the active area of the delta–sigma modulator and the area of circuits used to generate biasing voltages and reference voltages shared by each system module. The whole area of the modulator and the biasing circuits is 365 × 290 μm^2. The whole power consumption is 515 μW in which 250 μW is consumed by delta–sigma modulator and 265 μW is consumed by biasing circuits. Table 2 summarizes the overall experimental results.

The figure of merit (FOM) is used to evaluate the power efficiency of this modulator.

$$\mathrm{FOM} = \frac{P}{2^n f_{\mathrm{sample}}}, \tag{16}$$

where n is the number of bits, P is the power consumption in watts and f_{sample} is the sampling frequency in hertz. The FOM is 6.0 × 10^{-11} J/state.

Table 2. Modulator performance.

Parameter	Value
Technology	0.35-μm CMOS
DR	67.5 dB
ENOB	8 bit
SNR (peak)	55.03 dB
SNDR (peak)	49.01 dB
Over-sampling ratio	64
Sampling rate	16 kHz
Signal bandwidth	100 Hz
Supply voltage	2.5 V
Power consumption	250 μW (By modulator)
	265 μW (By biasing)
Active die area	365 × 290 μm^2

Table 3. Comparative study.

	P (μW)	N (bit)	Tech.	V_{DD} (V)	FOM (10^{-11}J/state)
Ref. [16]	400	11	0.18 μm CMOS	1.8	2.4
Ref. [17]	180	8	0.18 μm CMOS	0.8	3.7
This work		8	0.35 μm CMOS	2.5	6.0

5. Conclusions and discussions

A low power 8-bit delta–sigma modulator which is to be integrated in the front-end system for EEG monitoring applications is presented in this paper. This ADC reaches a FOM of 6.0 × 10^{-11} J/state. The active area of this ADC is less than 0.1 mm^2. These advantages make this ADC suitable to be integrated in the EEG monitoring system.

Table 3 shows the comparative study of some recently published ADCs for biomedical applications. The modulator in this paper is fabricated by less advanced technology. But the power efficiency of our modulator reaches the same level of the listed references.

References

[1] Yang H Y, Sarpeshkar R. A bio-inspired ultra-energy-efficient analog-to-digital converter for biomedical application. IEEE Trans Circuits Syst, 2006, 53(11): 2349

[2] Lopez-Morillo E, Carvajal R G, Muno F Z, et al. A 1.2-V 140-nW 10-bit sigma–delta modulator for electroencephalogram applications. IEEE Trans Biomedical Circuits Syst, 2008, 2(3): 223

[3] Goes J, Paulino N, Pinto H, et al. Low-power low-voltage CMOS A/D sigma–delta modulator for bio-potential signals driven by a single-phase scheme. IEEE Trans Circuits Syst, 2005, 52(12): 2595

[4] Gerosa A, Maniero A, Meviani A. A fully integrated two-channel A/D interface for the acquisition of cardiac signals in implantable pacemakers. IEEE J Solid-State Circuits, 2004, 39(7): 1083

[5] Liew W S, Yao L, Lian Y. A moving binary search SAR-ADC for low power biomedical data acquisition system. IEEE APCCAS, 2008: 646

[6] Aksenov E V, Ljashenko Y M, Plotnikov A V, et al. Biomedical data acquisition systems based on sigma–delta analogue-to-digital converters. IEEE EMBS 23rd Annu Int Conf, 2001: 3336.

[7] Harrison R R, Charles C. A low-power low-noise CMOS amplifier for neural recording applications. IEEE J Solid-State Circuits,

2003, 38(6): 958

[8] Geerts Y, Marques A M, Steyaert M S J, et al. A 3.3-V, 15-bit, delta–sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications. IEEE J Solid-State Circuits, 1999, 34(7): 927

[9] Peluso V, Steyaert M, Sansen W. Design of low-voltage low-power CMOS delta–sigma A/D convertors. Kluwer Academic Publishers, ISBN 0-7923-8417-2, 1999

[10] Ruiz-Amaya J, de la Rosa J M, Fernandez F V, et al. High-level synthesis of switched-capacitor, switched-current and continuous time $\Sigma\Delta$ modulators using SIMULINK based time domain behavioral models. IEEE Trans Circuits Syst I, Reg Papers, 2005, 52(9): 1795

[11] Razavi B. Design of analog CMOS integrated circuits. Published McGraw-Hill, ISBN 0-07-236032-2, 2001

[12] Rabii S, Wooley B A. The design of low voltage, low power sigma delta modulators. Norwell, MA: Kluwer, 1999

[13] Allen P E, Holberg D R. CMOS analog circuit design. Oxford University Press, Inc, ISBN 978-7-121-04746-6, 2002

[14] Brigati S, Francesconi F, Malcovat P, et al. Modeling sigma delta modulator non-idealities in simulink. ISCAS, Orlando, USA, 1999: 384

[15] Choksi O, Carley L R. Analysis of switched-capacitor common-mode feedback circuit. IEEE Trans Circuits Syst II, Analog and Digital Signal Processing, 2003, 50(12): 906

[16] Lee H Y, Hsu C M, Huang S C, et al. Designing low power of sigma delta modulator for biomedical application. Biomed Eng Applicat, Basis, Commun, 2005, 18: 181

[17] Lee S Y, Cheng C J. A low-voltage and low-power adaptive switched-current sigma–delta ADC for bio-acquisition microsystems. IEEE Trans Circuits Syst I, Reg Papers, 2006, 53(12): 2628