RF CMOS modeling: a novel empirical large-signal model for an RF-MOSFET*

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Abstract: A novel empirical model for large-signal modeling of an RF-MOSFET is proposed. The proposed model is validated in the DC, AC, small-signal and large-signal characteristics of a 32-finger nMOSFET fabricated in SMIC's 0.18 μm RF CMOS technology. The power dissipation caused by self-heating is described. Excellent agreement is achieved between simulation and measurement for DC, S-parameters (50 MHz–40 GHz), and power characteristics, which shows that our model is accurate and reliable.

Key words: RF-MOSFET; large-signal model; self heating
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1. Introduction

In recent years, the rapid growth of wireless communication at radio frequencies (RF) has created a huge demand in high-performance RF components for power amplifiers (PA). Because of the good RF performance and low cost, CMOS transistors have been more and more frequently applied in PA circuit design[1–4]. A reliable model for RF-MOSFET device is a key requirement for a successful design, simulation and evaluation of a PA. Unfortunately, RF-MOSFET models for PA design have rarely been reported so far.

A good large-signal for non-linear circuit design (such as PA) is capable of extracting and approximating third- or fifth-order derivatives of I/V and Q/V functions[5]. However, the standard MOSFET models, such as BSIM[6, 7] and PSP[8, 9], are not developed for PA design, which emphasizes a model equation of continual high-order derivation. For example, the BSIM[6, 7] model's equation is the discontinuity of first-order derivatives. The PSP[8, 9] model is developed for describing device characteristics of nanometer dimension; the derivatives of its equation are not verified, so it is not suitable for large-signal simulation.

Some work on the CMOS large-signal model can be found in the literature, such as the Angelov–Zirth model[10, 11]. The model developed by Angelov *et al*.[10, 11] is capable of describing I–V characteristics at low gate voltages or in the saturation region. However, the model uses a tanh function to characterize the $I_{\rm ds}$, so the curve of its first-order trans-conductance is symmetrical at the point of maximum trans-conductance, which means that the model cannot describe the trans-conductance accurately.

In this paper, we propose an accurate, well convergent large-signal model for RF CMOS transistors, whose equation is continuous and high-order differentiable. The power dissipation caused by self-heating is described. Wonderful results were achieved in the comparison between measurements and simulation of DC, AC, small-signal, large-signal and power characteristics for 0.18 μm CMOS FETs.

2. Model topological structure

Figure 1 gives the topology of the equivalent circuit employed in this work. $R_{\rm g}$, $R_{\rm d}$ and $R_{\rm s}$ are the gate, drain and source resistances respectively. $C_{\rm gs}$ and $C_{\rm gd}$ are gate–source and gate–drain capacitances, respectively. $R_{\rm gs}$ and $R_{\rm gd}$ are in series with $C_{\rm gs}$, $C_{\rm gd}$, respectively, used to improve the prediction of S_{11} and S_{22} at high frequencies. $I_{\rm ds}$ is the channel current, while $I_{\rm db}$ is used to capture the frequency distribution effect of trans-conductance. The value of $I_{\rm db}$ is $\alpha I_{\rm ds}$, where α is a constant. $R_{\rm db}$ and $C_{\rm db}$ generate a critical frequency for the frequency distribution effect of trans-conductance. A sub-circuit constructed with $R_{\rm th}$, $C_{\rm th}$ and $P_{\rm dev}$ is used to predict the power dissipation caused by the self-heating effect and $P_{\rm dev}$, is calculated as $I_{\rm ds}V_{\rm ds}$, represents the average power level. In this work, $C_{\rm gs}$, $C_{\rm gd}$, $I_{\rm ds}$ and $I_{\rm db}$ are bias-dependent components, while the others are bias-independent components.

3. Current equation

For non-linear simulation, a continuity and high-order differentiable channel model is of the utmost importance. The channel current model ($I_{\rm ds}$) proposed in this work is as follows:

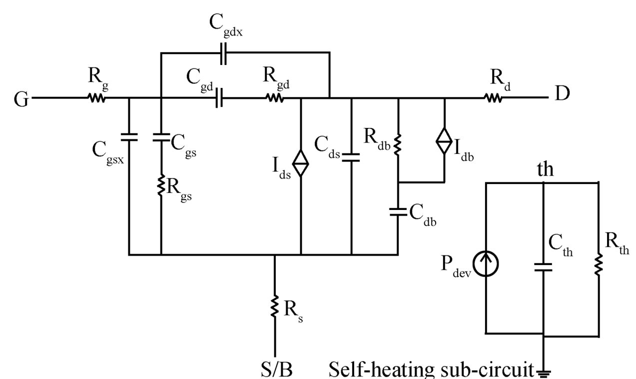

Fig. 1. Equivalent circuit of CMOS.

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$$\text{vgs1p} = P_1\{1 + B_1[\cosh(B_0 V_{ds})]\}^{-2})(V_{gsi} - V_{th} - P_{n0} V_{ds}), \quad (1)$$

$$\text{vgs1n} = P_1\{1 + B_1[\cosh(B_0 V_{ds})]\}^{-2})(V_{gdi} - V_{th} - P_{n0} V_{ds}), \quad (2)$$

$$\text{vgs2p} = 0.5\text{vgs1p} + 0.5\left[\sqrt{(\text{vgs1p} - V_k)^2 + D_{elta}^2} - 0.5\sqrt{V_k^2 + D_{elta}^2}\right], \quad (3)$$

$$\text{vgs2n} = 0.5\text{vgs1n} + 0.5\left[\sqrt{(\text{vgs1n} - V_k)^2 + D_{elta}^2} - 0.5\sqrt{V_k^2 + D_{elta}^2}\right], \quad (4)$$

$$\text{vgs3p} = V_{st}\left[\ln(1 + e^{\text{vgs2p}/V_{st}})\right], \quad (5)$$

$$\text{vgs3n} = V_{st}\left[\ln(1 + e^{\text{vgs2n}/V_{st}})\right], \quad (6)$$

$$\text{idspp} = B_{eta}\,(\text{vgs3p})^2 / \left[1 + V_l\,(\text{vgs3p})^{P_{lin}}\right], \quad (7)$$

$$\text{idspn} = B_{etar}\,(\text{vgs3n})^2 / \left[1 + V_l\,(\text{vgs3n})^{P_{linr}}\right], \quad (8)$$

$$a_0 = (H_1 V_{ds}) \ln\left[H_2 + H_3(\text{vgs3p})^{H_4}\right], \quad (9)$$

$$a = \tanh\left\{A_{lphas} a_0 \left[1 + \tanh(\text{vgs1p})\right]\right\}, \quad (10)$$

$$b_0 = (H_{11} V_{ds}) \ln\left[H_{21} + H_{31}(\text{vgs3n})^{H_{41}}\right], \quad (11)$$

$$b = \tanh\left\{A_{lphar} b_0 \left[1 + \tanh(\text{vgs1n})\right]\right\}, \quad (12)$$

$$\lambda\text{p} = L_{ambda} V_{ds}(1 + V_{klambda} \tanh(K_{lambda}(V_{gsi} - V_{llambda}))), \quad (13)$$

$$\lambda\text{n} = L_{ambda} V_{ds}\,(1 + V_{klambda} \tanh(K_{lambda}(V_{gdi} - V_{llambda}))), \quad (14)$$

$$I_{dsp} = \text{idspp}\,(1 + a)\,(1 + \lambda p V_{ds}) \quad (15)$$

$$I_{dsn} = \text{idspn}\,(1 + b)\,(1 - \lambda n V_{ds}) \quad (16)$$

$$I_{dsi} = 0.5\left(I_{dsp} - I_{dsn}\right) \quad (17)$$

where P_1, V_{th}, V_k, V_l, D_{elta}, V_{st}, P_{lin}, P_{linr}, B_{eta}, B_{etar}, P_{n0}, H_1, H_2, H_3, H_4, H_{11}, H_{21}, H_{31}, H_{41}, A_{lphas}, A_{lphar}, B_0, B_1, $V_{klambda}$, K_{lambda} and L_{ambda} are model parameters. V_{th} is the threshold voltage.

The components idspp and idspn and those relevant parameters determine the fitting precision of model equations on trans-conductance, whereas the following components and the related parameters play a great part in fitting the drain conductance within the linear region. Thus, the drain conductance in the linear region can be fitted. The continuity and high-order differentiability are both realized; meanwhile, the drain conductance G_{ds}, trans-conductance G_m, G_{m2}, G_{m3} and even higher order trans-conductance characteristics can be accurately fitted, which satisfies the need for high order harmonic simulation for non-linear current model equations[5].

In this model, we only consider the self-heating effect of core parameters such as B_{eta}, which are extracted by curve-fitting. The scaling equation of model parameters is stated as follows:

$$K_{ey}_P_{arameter}_T = P_{arameter}\left[\left(rT^{T_1}\exp(E_t\frac{1 - rT}{V_{tv}})\right)\right]^{T_2}, \quad (18)$$

where $P_{arameter}$ is the initial model parameter to be scaled, while T_1, T_2 and E_t are the fitting parameters. B_{eta} and B_{etar} in the current equations can be temperature scaled by applying Eq. (18).

4. Capacitance equations

In the implementation in CAD tools, a capacitance formulation was used directly. Here, we use the effective gate voltage formulations which we used in the current equations to construct the relationship between C_{gs} (C_{gd}) and gate voltage. This capacitance model can give the high-order differentiability of bias, and satisfy the charge conservation law.

$$\text{vgs1} = P_{c1}(V_{gsi} - V_{th}), \quad (19)$$

$$\text{vgs2} = 0.5\text{vgs1} + 0.5\sqrt{(\text{vgs1} - V_{kc})^2 + D_{eltac}^2} - 0.5\sqrt{V_{kc}^2 + D_{eltac}^2}, \quad (20)$$

$$\text{vgs3} = V_{stc}\ln\left(1 + e^{\text{vgs2}/V_{stc}}\right), \quad (21)$$

$$a_{10} = (\text{vgs3})^{P_{linc0}} - (V_{stc}\ln 2)^{P_{linc0}}, \quad (22)$$

$$a_{12} = (\text{vgs3})^{P_{linc1}}, \quad (23)$$

$$a_{11} = 1/(1 + a_{12} V_{lc}) - 1/\left[1 + V_{lc}\,(V_{stc}\ln 2)^{P_{linc1}}\right], \quad (24)$$

$$C_s = C_{beta} a_{11} a_{10}, \quad (25)$$

$$X_{gs} = 1 + \tanh\left[K_{gs}\left(V_{gsi} - V_{t2gs}\right)\right] - \tanh\left[K_{gs}\left(-V_{t2gs}\right)\right], \quad (26)$$

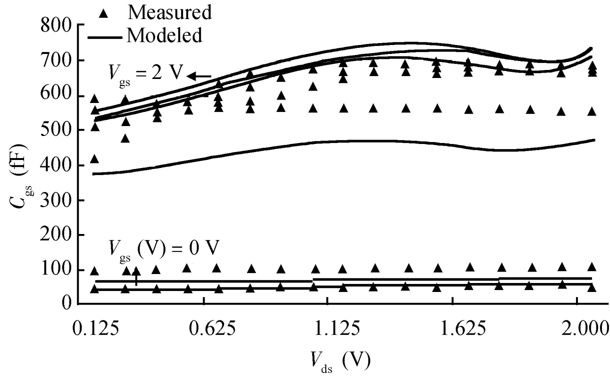

Fig. 2. Comparison of capacitances: C_{gs} of V_{gs} (V_{gs}: 0–2 V, step: 0.4 V).

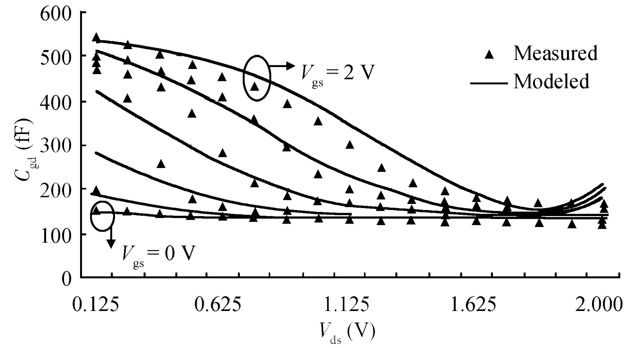

Fig. 3. Comparison of capacitances: C_{gd} of V_{gs} (V_{gs}: 0–2 V, step: 0.4 V).

$$\text{dvgs} = M_{gs}C_{gs0}\left(1+\sinh(B_{C0}V_{ds})\right) + \left(1-M_{gs}\right)C_{gs0}X_{gs}, \tag{27}$$

$$X_{gd} = 1+\tanh[K_{gd}(V_{gdi}-V_{t2gd})]-\tanh[K_{gd}(-V_{t2gd})], \tag{28}$$

$$\text{dvgd} = M_{gd}C_{gd0}\left(1+\sinh(B_{C1}V_{ds}\right) + \left(1-M_{gd}\right)C_{gd0}X_{gd}, \tag{29}$$

$$f_2 = C_s\left[1+\tanh\left(K_{cc}\left(V_{ds}-V_{t4}\right)\right)\right]$$
$$-\frac{\partial C_s}{\partial V_{gs}}\left[V_{gdi}-\ln\left(\cosh\left(K_{cc}\left(V_{ds}-V_{t4}\right)\right)\right)/K_{cc}\right], \tag{30}$$

$$g_2 = -C_s\left[1+\tanh\left(K_{cc}\left(V_{ds}-V_{t4}\right)\right)\right], \tag{31}$$

$$C_{gsi} = \text{dvgs} + f_2, \tag{32}$$

$$C_{gdi} = \text{dvgd} + g_2, \tag{33}$$

where P_{c1}, V_{kc}, V_{lc}, D_{eltac}, V_{stc}, P_{linc0}, P_{linc1}, C_{beta}, V_{t2gs}, K_{gs}, M_{gs}, B_{c0}, C_{gs0}, K_{gd}, M_{gd}, B_{c1}, C_{gd0}, K_{cc} and V_{t4} are model parameters. C_{gs0} and C_{gd0} are the gate–source and gate–drain capacitance when the channel is cut off, respectively.

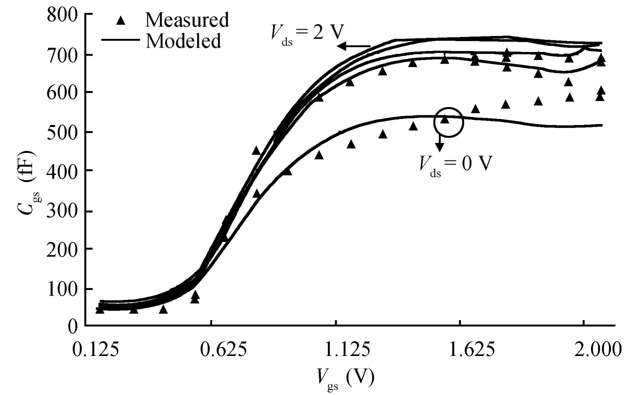

Fig. 4. Comparison of capacitances: C_{gs} of V_{gd} (V_{ds}: 0, 0.8, 1.2, 1.6 and 2 V).

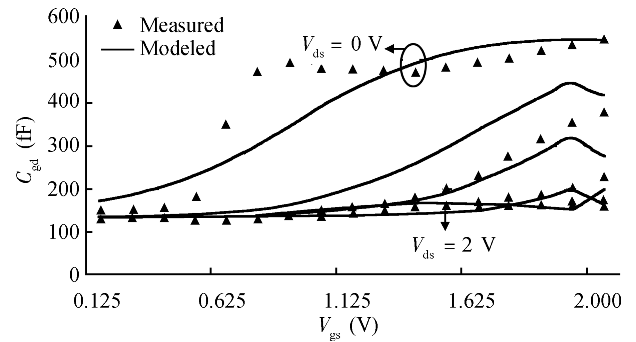

Fig. 5. Comparison of capacitances: C_{gd} of V_{gd} (V_{ds}: 0, 0.8, 1.2, 1.6 and 2 V).

5. Experimental evaluation of the model

To verify and validate the accuracy of the proposed model, a 32-finger RF MOSFET, in which the width and length of each finger is 7.5 μm and 0.18 μm respectively, is fabricated by employing SMIC 0.18 μm RF-CMOS technology. The DC characteristics of this device were measured using an Agilent 4156C LCR-meter. Two-port S-parameters were measured and de-embedded (Open + Short) for parasitics introduced by GSG PAD using an Agilent E8363B network analyzer and a CASCADE Summit probe station, while the parameter value extraction was implemented in Agilent IC-CAP2008. Verilog-AMS technology was used to describe, compile and link this model into the Agilent advanced design system for simulation.

S-parameters are de-embedded, so pad parasitic effects are not considered in this work. The bias-independent components are extracted from the Z-parameter in the linear area ($V_{gs} \gg V_{th}$, $V_{ds} = 0$ V) and the Y-parameter in the zero-bias condition ($V_{gs} = 0$ V, $V_{ds} = 0$ V). They are then optimized with the measured S-parameters at a large range of V_{ds} and V_{gs}. The parameters of the current equations are extracted by fitting the measured I–V curve, while the parameters of the capacitance equations are extracted by fitting the C–V curve which is extracted from the measured S-parameters.

The extracted and modeled C_{gs} versus V_{ds} (V_{gs}: 0–2 V, step: 0.4 V), C_{gd} versus V_{ds} (V_{gs}: 0–2 V, step: 0.4 V), C_{gs} versus V_{gs} (V_{ds}: 0, 0.8, 1.2, 1.6 and 2 V) and C_{gd} versus V_{gs} (V_{ds}: 0, 0.8, 1.2, 1.6 and 2 V) characteristics of the 32-finger RF MOSFET are plotted in Figs. 2–5. Considering measurement errors and capacitance differences at different measured fre-

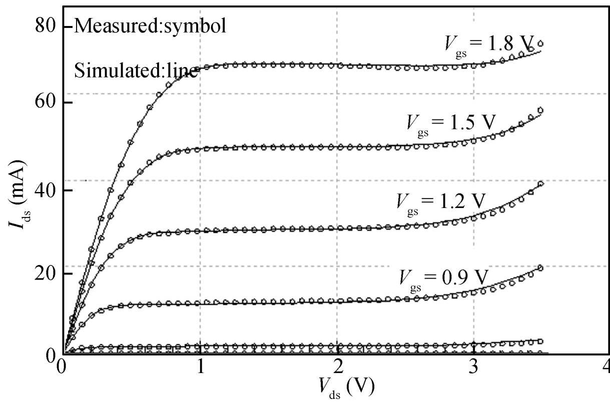

Fig. 6. Comparison of current: I_{ds} of V_{ds}.

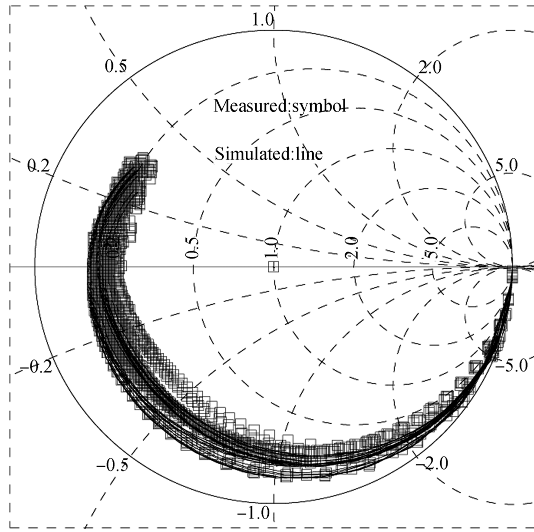

Fig. 7. Comparison of S_{11}.

quency points, the fitting results in the plots indicate that the charge/capacitance model proposed in section 4 can predict the $C-V$ characteristics of the MOSFET accurately.

Figure 6 shows the measured and simulated data under the condition of V_{ds}: 0–3.5 V, step 70 mV, V_{gs}: 0–1.8 V, step 300 mV. It can be seen that this model has a good fitting precision for DC characteristics, as well as the self-heating effect.

Measured and modeled S-parameters, V_{gs}: 0–2 V, step 250 mV, V_{ds}: 0–2 V, step 1 V are compared with frequency up to 40 GHz and shown in Figs. 7–10. It is observed from the comparison results that our model can accurately describe the MOSFET's small-signal characteristic.

For large-signal models, a common validation method is the comparison between measured and modeled load-pull data. Hence, the power characterization measurement has been implemented on a focus microwave multi-harmonic passive load-pull bench based on automated tuners. The optimal source and load impedances are $Z_s = 49.93 + j0.70$ and $Z_l = 50.12 + j0.42$. The fundamental frequency, gate–source, and drain–source voltage have been set to 2 GHz, 1.5 V, 4.5 V, respectively. The input power swept from –8.76 to 13.32 dBm. The comparison results for P_{out}, gain and PAE are plotted in Fig. 11. It can be observed from Fig. 11 that the power characteristics of our model are accurately, continuous and conver-

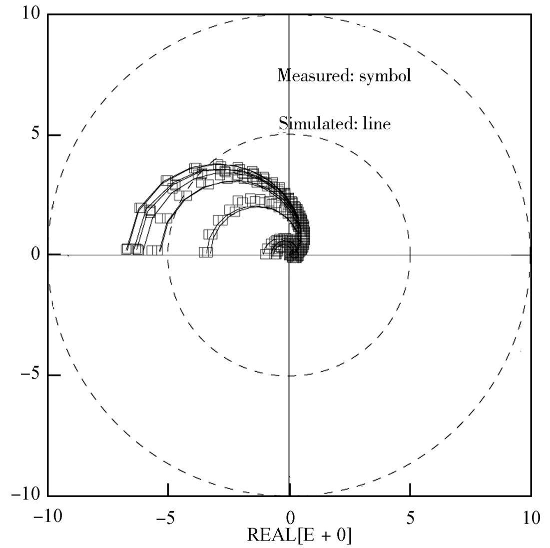

Fig. 8. Comparison of S_{21}.

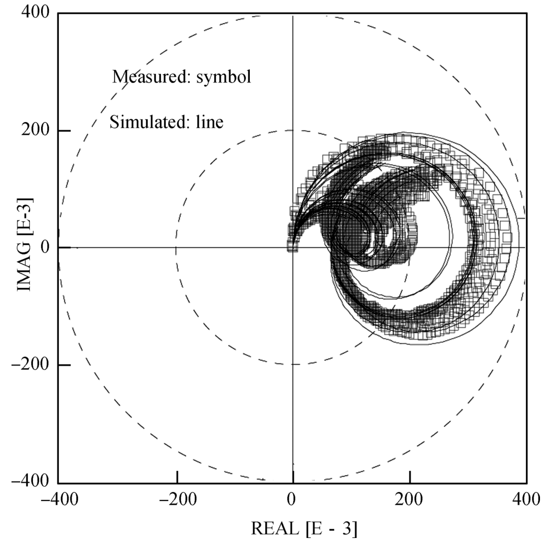

Fig. 9. Comparison of S_{12}.

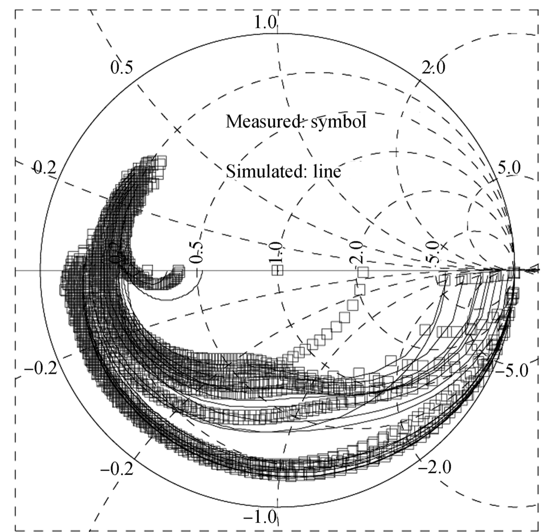

Fig. 10. Comparison of S_{22}.

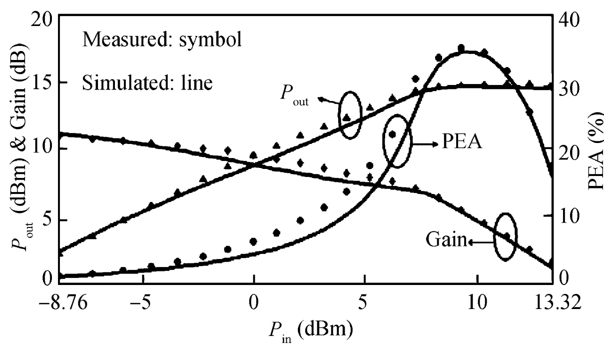

Fig. 11. Comparison of $P_{\rm out}$, Gain and PAE.

gent. The computer setup used in the simulation is CPU: Pentium (R) 4, 3 GHz and EMS memory: 1 GB, the software of simulation: ADS2008, simulation time: 1.65 s.

6. Conclusions

A novel large-signal empirical model for high frequency CMOS transistors has been proposed. The model's current equations and bias-dependent charge equations are continuous and high-order differentiable. This model also takes the heat power dissipation induced by the self-heating effect into account. The model exhibits excellent prediction for the experimental evaluation through DC, AC, small-signal, large-signal and power measurements.

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