A low power wide-band CMOS PLL frequency synthesizer for portable hybrid GNSS receiver*

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Abstract: The design consideration and implementation of a CMOS frequency synthesizer for the portable hybrid global navigation satellite system are presented. The large tuning range is achieved by tuning curve compensation using an improved VCO resonant tank, which reduces the power consumption and obtains better phase noise performance. The circuit is validated by simulations and fabricated in a standard 0.18 μm 1P6M CMOS process. Close-loop phase noise measured is lower than –95 dBc at 200 kHz offset while the measured tuning range is 21.5% from 1.47 to 1.83 GHz. The proposed synthesizer including source coupled logic prescaler consumes 6.2 mA current from 1.8 V supply. The whole silicon required is only 0.53 mm^2.

Key words: CMOS; GNSS; dual-modulus; voltage-controlled oscillator; frequency synthesizer
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1. Introduction

Although global positioning system (GPS) is the only fully operational, available global navigation satellite system (GNSS), other planned GNSS, including GLONASS, Galileo and China's Compass, modernization will undoubtedly further expand and improve applications for users in many fields by allowing the combined use of such systems in hybrid receivers. Many researchers have investigated the dual band GPS receiver and receivers in combination with GPS and other communication standards[1−3]. Future GNSS receivers will have the capability of receiving all GNSS signals with the same RF front-end. The development of handhelds with more and more standards and services requires lower power, higher integration and lower cost for the radio implementation. Therefore, it is desirable to design a wide-band PLL frequency synthesizer with low power, low phase noise and small area.

The main challenge in implementing a PLL frequency synthesizer is the design of a wide band VCO with low power consumption and high phase noise performance. The most popular solutions to increase the tuning range of VCO are switching the LC tank[4], capacitor[5] and inductor[6]. Switching the LC tank is two separate resonators with different tuning ranges. Phase noise, tuning range and power consumption could be optimized separately, but large area cost is required. A switched-capacitor array bank is widely used with a binary-weighted structure. However, it suffers from quality factor (Q) degradation due to MOS switches, especially in low frequency band. Switched-inductor is used but only the Q of the inductor is much larger than that of the capacitor varactor. So, it is difficult to get reasonable phase noise when operation frequency is below 10 GHz. As a result, the conventional wide-band frequency synthesizer suffers from large power consumption and degraded phase noise or large chip area cost.

In this paper, the requirements of PLL for hybrid GNSS receiver are analyzed. A fully integrated CMOS frequency synthesizer for portable GNSS receiver based on dual-modulus frequency divider is proposed. An improved VCO employing tuning curve compensation technique to achieve wide tuning range, while reducing amplitude-to-phase modulation (AM-PM) conversion and improving the phase noise performance[7].

2. Frequency synthesizer design criteria

2.1. Frequency plan

There are currently two operational GNSS: GPS operated by the US government and GLONASS run by the Russian Federation. In addition, the European Union's Galileo positioning system and China's Compass system are two planned GNSS. To meet the stringent power and area requirements in portable devices, only civilian RF bands are supported in hybrid GNSS receiver. So, the tune range of the frequency synthesizer should be wide enough to cover all civilian RF bands of four types of GNSS. With the temperature and process variation considered, the frequency synthesizer is tuned from 1.5 to 1.8 GHz.

2.2. Phase noise on NF degradation

The ultimate goal of a GNSS receiver is to extract the accurate position and time information from the weak satellite signals. Usually, received weak GNSS signals are below the thermal noise floor. The phase noise of the frequency synthesizer reciprocally mixing thermal noise floor (KTB) corrupts output spectrum at the output of mixer. As a result, the equivalent noise from reciprocally mixing phase noise at RF input degrades the cascade noise figure (NF), which is demonstrated in Fig. 1(a). In a receiver, noise figure is defined as[8]

$$\mathrm{NF} = 10\lg F(\mathrm{dB}), \tag{1}$$

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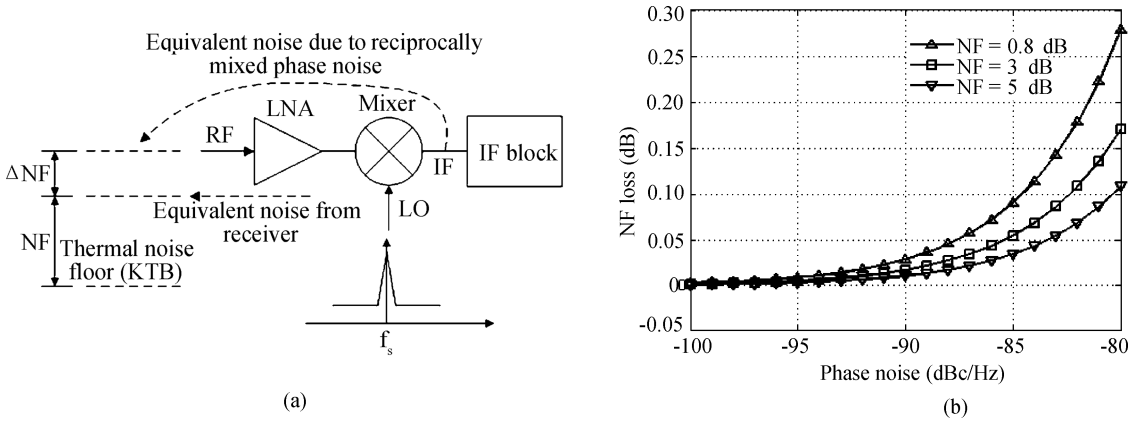

Fig. 1. (a) Reciprocally mixed phase noise and thermal noise floor. (b) Effect of phase noise on NF degradation.

where F is the noise factor. Provided an ideal local oscillator without phase noise, the noise factor of the receiver is expressed as the ratio of total equivalent noise and the thermal noise floor at RF input band.

$$F = \frac{N_{\text{thermal}} + N_{\text{eq}}}{N_{\text{thermal}}} = \frac{\text{KTB} + N_{\text{eq}}}{\text{KTB}}, \tag{2}$$

where N_{thermal} denotes the thermal noise floor in band (KTB) and N_{eq} is the equivalent noise from the receiver. The equivalent added noise due to phase noise at RF input band is calculated by

$$N_{\text{PN}} = N_{\text{thermal}} \int_{-\infty}^{+\infty} L(\omega)\mathrm{d}\omega, \tag{3}$$

where $L(\omega)$ is the phase noise of local oscillator. The NF loss due to phase noise is equal to

$$\begin{aligned}\Delta\text{NF} &= 10\lg\left(1 + \frac{N_{\text{PN}}}{FN_{\text{thermal}}}\right) \\ &= 10\lg\left(1 + \frac{\displaystyle\int_{-\infty}^{+\infty} L(\omega)\mathrm{d}\omega}{F}\right).\end{aligned} \tag{4}$$

From Eq. (4), the NF loss is inversely in proportion to noise factor F. The effect of phase noise is shown in Fig. 1(b). As the emergence of a high sensitivity GNSS receiver, the NF is lower than 1 dB. Considering civilian RF band of GNSS, GLONASS has the largest bandwidth, which is about 8 MHz. To achieve less than 0.1 dB NF loss, the averaged phase noise of local oscillator should be lower than -85 dBc/Hz.

3. Circuit implementation

3.1. PLL architecture

Basically, the frequency synthesizer can be implemented by integer-N and fractional-N PLL. The fractional-N PLL provides a finer frequency resolution with the same reference frequency compared to integer-N and has a faster setting time. The main drawback of fractional-N PLL is suffering from reference spurs. In a hybrid GNSS receiver, startup time and frequency resolution is not a major issue but reference spurs is a concern. As a consequence, the integer-N is adopted in this synthesizer. Figure 2 shows the system architecture of the proposed synthesizer targeting for portable hybrid GNSS receiver. A wide band VCO using a tuning curve compensation technique covers all civil RF bands of GNSS without capacitor or inductor switches, which runs at double output frequency. Consequently, it has lower power consumption and better phase noise performance. A divided-by-two prescaler using source coupled logic (SCL) generates quadrature output, which includes an ECL-CMOS buffer in order to interface between the prescaler and the rest of the divider. To reduce the power consumption, dual-modulus frequency divider based on TSPC circuit is employed.

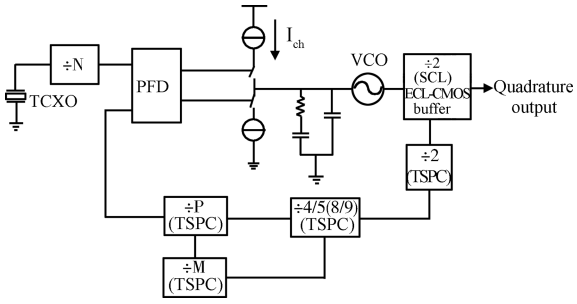

Fig. 2. Block diagram of proposed frequency synthesizer.

3.2. Proposed wide-band LC-VCO with tuning curve compensation

A single wide-band LC VCO covering all RF bands has two profits. It saves chip area cost and reduces power consumption. An improved LC-VCO with tuning curve compensation is introduced to avoid phased noise degrades from MOS switches, which is shown in Fig. 3(a). It consists of cross-coupled transistors MP1, MP2 and MN1, MN2, tail current source MP5 and LC-tank circuit. The cross-coupled transistors generate negative resistance to compensate the equivalent resistance of the LC tank. Tail current source MP5 provides a trade off between phase noise and power dissipation. Large tail current results in a lower phase noise but results in a larger power dissipation. One disadvantage of tail current source is that its $1/f$ noise is up-converted to the LC tank and degrades the phase noise. In this design, $1/f$ noise is reduced by large MP5. An on-chip symmetry spiral inductor L is implemented by top thick metal.

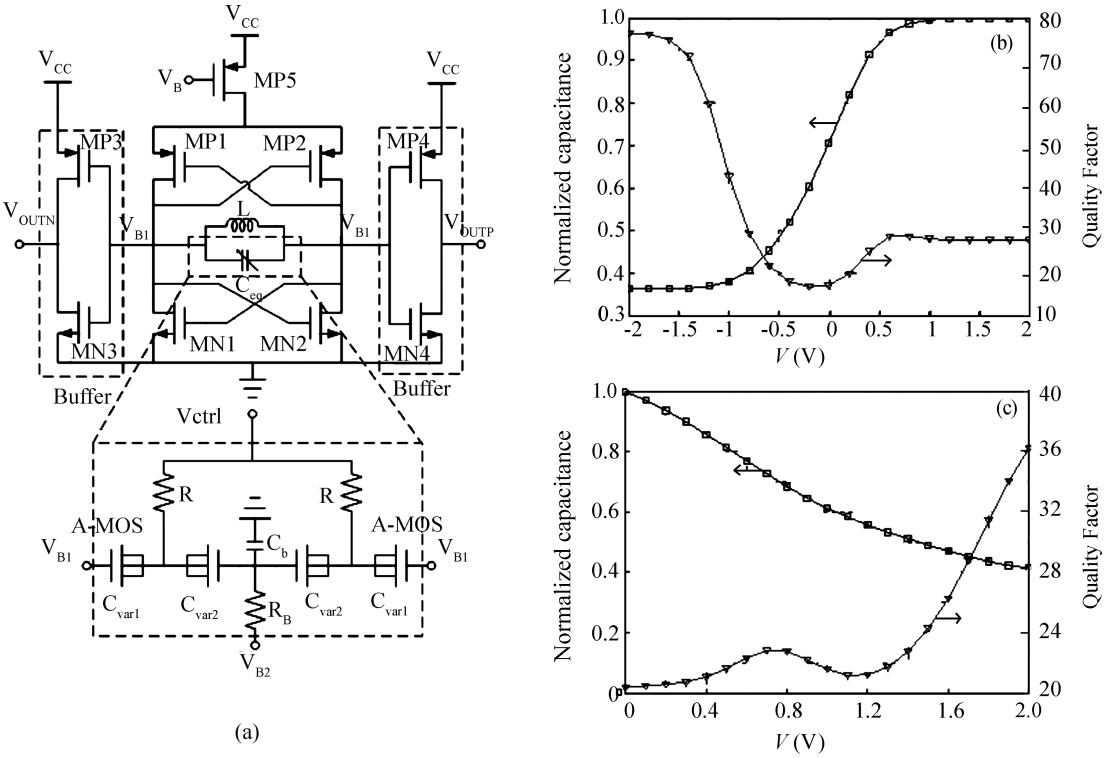

Fig. 3. (a) Schematic of proposed complementary-Gm CMOS LC VCO. (b) Conventional C–V and Q–V curve of varactor. (c) C–V and Q–V curve of proposed varactor.

Larger inductance of L is desired for lower power consumption. However, it limits the tuning range and results in a poor phase noise. Inductor L is optimized according to specified tuning range and phase noise.

Varactor is one of the key components in LC-VCO. Conventionally, varactor using a single A-MOS suffers from a steep capacitance–voltage (C–V) curve and low quality factor (Q) in weak inversion, which is shown in Fig. 3(b). In this design, a novel A-MOS configuration is proposed, which is illustrated in the bottom part of Fig. 3(a). Two serial connected A-MOSs $C_{\rm var1}$ and $C_{\rm var2}$ with offset DC bias voltage $V_{\rm B1}$ and $V_{\rm B2}$ comprise the equivalent tuning curve compensated A-MOS (E-AMOS). $V_{\rm ctrl}$ is the control voltage and connects to the bulk of two A-MOSs by a resistor R. $V_{\rm B1}$ and $V_{\rm B2}$ are DC bias of the gates. When $V_{\rm ctrl}$ varies from 0 to 1.8 V, gate-bulk voltage of $C_{\rm var1}$ is changed from $V_{\rm B1}$ to $V_{\rm B1} - 1.8$ V while that of $C_{\rm var2}$ is biased from $V_{\rm B2}$ to $V_{\rm B2} - 1.8$ V. The offset bias voltage is equal to $V_{\rm B1} - V_{\rm B2}$. The corresponding C–V curves between $C_{\rm var1}$ and $C_{\rm var2}$ is shifted by the same offset bias voltage. The equivalent capacitance is

$$C_{\rm eq}(V_{\rm ctrl}) = \frac{C_{\rm var1}(V_{\rm B1} - V_{\rm ctrl}) \times C_{\rm var2}(V_{\rm B2} - V_{\rm ctrl})}{C_{\rm var1}(V_{\rm B1} - V_{\rm ctrl}) + C_{\rm var2}(V_{\rm B2} - V_{\rm ctrl})}. \quad (5)$$

where $V_{\rm B1}$ is equal to the gate–source voltage of MN1, MN2, normally, $V_{\rm B1}$ is about half of power supply voltage. Because the C–V curve of $C_{\rm var1}$ and $C_{\rm var2}$ are fitted with $\tanh(x)$ function in the spice model, it is difficult to calculate $V_{\rm B2}$ directly from Eq. (5). In fact, if $V_{\rm B1} - V_{\rm B2}$ is about the linear range of $C_{\rm var1}$, $C_{\rm var2}$ in C–V curve, the equivalent C–V tuning curve of E-AMOS is approximately linear. Figure 3(c) shows the normalized C–V curve by the maximum capacitance and quality factor of the equivalent capacitor with 0.9 V offset bias voltage. The C–V curve is smooth the control voltage $V_{\rm ctrl}$ varies from 0 to 2 V. The $C_{\rm max}/C_{\rm min}$ is equal to 2.5, which approaches to the tuning ratio of a single A-MOS. What's more, the equivalent quality factor of A-MOS and the tuning range would be optimized by the offset bias voltage. Two symmetry equivalent tuning curve compensated A-MOS (E-AMOS) are used as the tank varactor. By setting a proper offset voltage between $V_{\rm B1}$ and $V_{\rm B2}$, a smooth tuning curve and reasonable quality factor could be obtained.

Two buffers composed of MN3, MP3 and MN4, MP4 are used to reduce the load effects and frequency variation. They are also biased by the cross-couple pairs and their power consumptions are optimized according to loads.

3.3. Phase frequency detector and improved charge pump

Figure 4(a) shows the commonly used phase frequency detector (PFD). It mainly consists of two D-flip-flops and an AND gate. Dead zone is an important issue in PFD, which is determined by propagation delay from the AND gate. There is a tradeoff between dead zone and spurs. A digital tuned capacitor is employed to eliminate the dead zone problem.

Both integer-N and fractional-N frequency synthesizers suffer from spurs due to mismatch of charge pump. Several structures to reduce the charge current mismatch are compared in Ref. [9]. The charge pump with source switching is superior to others for moderate speed and low power consumption, which is implemented as Fig. 4(b). It basically consists of two low-voltage current mirrors MN7–NM12, MP7–MP10, pump-up switch MP4, MN4 and pump-down switch MP3, MN3. Compared with the charge pump presented in Ref. [9], it employs complementary NMOS and PMOS as source switches, which have similar resistance and parasitics. As a result, the

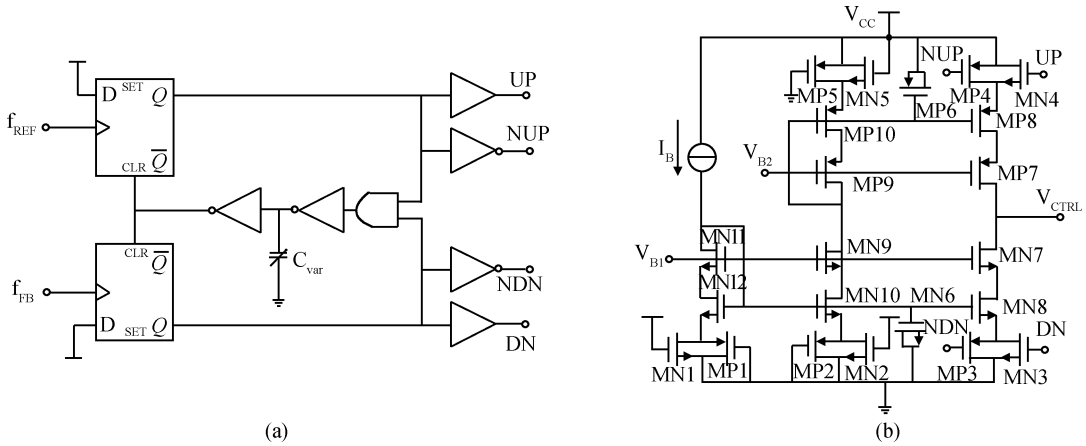

Fig. 4. (a) Simplified schematic of proposed PFD. (b) Schematic of improved charge pump.

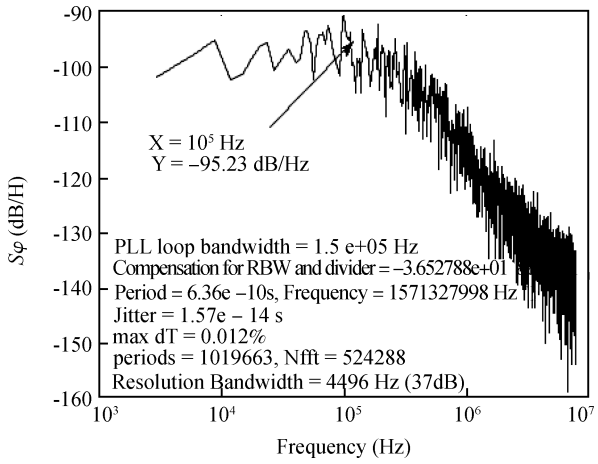

Fig. 5. Simulated phase noise power spectral density of closed-loop PLL.

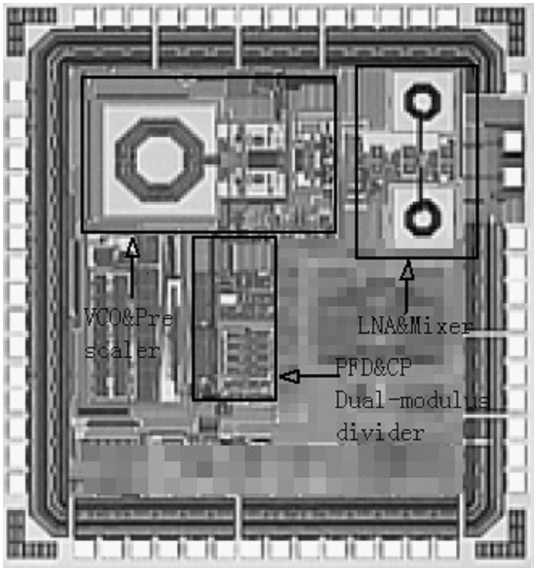

Fig. 6. Die micrograph.

pump-up switch and pump-down switch can be matched well. To obtain accurate current ratio of current mirrors, dummy switches MN1, MP1, MP2, MN2 and MP5, MN5 are used as source load.

4. Simulation results

The proposed frequency synthesizer is verified using voltage-domain models before silicon implementation. The phase noise of the reference oscillator and VCO are represented with accumulating jitter while that of PFD and charge pump is characterized with synchronous jitter. The simulated phase noise spectral density of close-loop PLL is below –95 dB @ 100 kHz, which is shown in Fig. 5.

5. Experimental results

The proposed frequency synthesizer has been manufactured in standard 0.18 μm 1P6M CMOS process integrated with a low noise amplifier (LNA), down-mixer and IF driver, which is shown in Fig. 6. The whole frequency synthesizer occupies 0.53 mm^2. The quadrature output of the frequency synthesizer generated by divided-by-two prescaler is mixed with a very low phase noise RF signal, which is generated by a low phase noise RF signal generator and further amplified by LNA. Down-converted IF signal is about 4MHZ and amplified by IF driver.

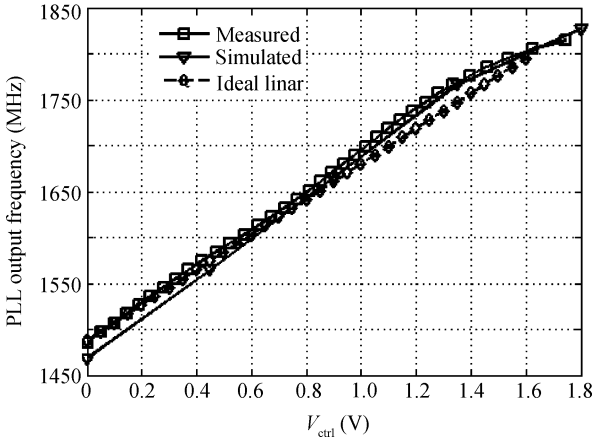

Fig. 7. Simulated and measured PLL tuning curve.

Table 1. Comparison of this work and related frequency synthesizers.

Parameter	This work	Ref. [10]	Ref. [11]	Ref. [12]
Technology	CMOS 180 nm	CMOS 180 nm	CMOS 180 nm	CMOS 130 nm
Center frequency (GHz)	1.65	1.8	2.432	3.5
Tuning range (%)	21.5	22.2	5.26	22.8
Power (mW)	11.2	29	29.6	48
Phase noise (dBc/Hz)	–95 @ 200 kHz (In-band), –118 @ 1 MHz	–98 @ 1 MHz	–113 @ 1 MHz	–84.29 @ 100 kHz
Locking-time (μs)	6.6	N/A	20	N/A
Area (mm^2)	0.53	2	2.08	1.5

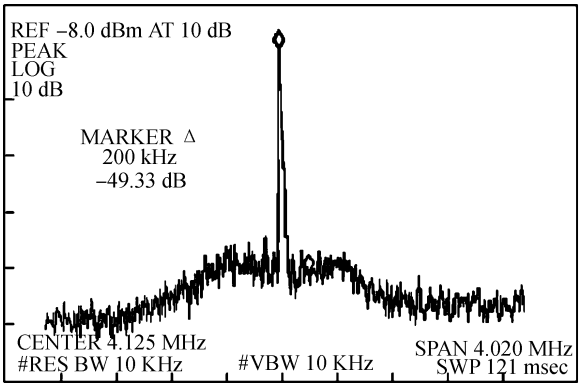

Fig. 8. Measured IF spectrum.

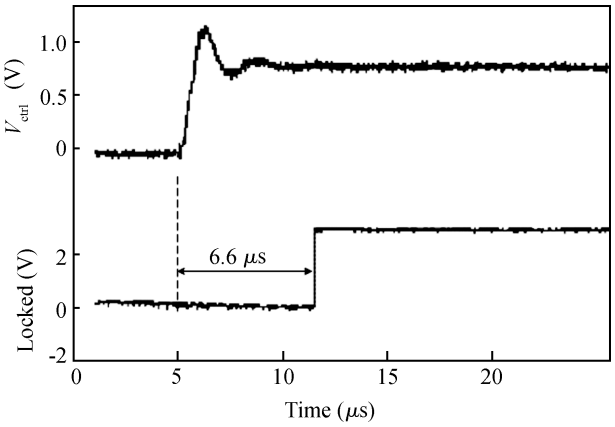

Fig. 9. Measured locking-in time of the proposed PLL.

Figure 7 shows the frequency tuning curve (f–V) of the proposed PLL. The closed-loop tuning curve is measured by fixing the feedback divider's ratio and changing the input reference frequency. The frequency of PLL changes from 1.48 to 1.83 GHz while the control voltage varies from 0 to 1.8 V. The tuning curve of the proposed PLL is much more linear than that of conventional frequency synthesizer during the whole tuning range, especially, when control voltage ($V_{\rm ctrl}$) is below 1 V. The measured result is well in agreement with simulation. During the whole tuning range, the proposed PLL consumes 6.2 mA from 1.8 V power supply including SCL divided-by-two prescaler.

The phase noise of the proposed frequency synthesizer is measured from IF port. Figure 8 shows the measured IF spectrum, and corresponding phase noise of proposed frequency synthesizer is better than −95 dBc at 200 kHz offset. Figure 9 illustrates measured transient response of the proposed PLL. The locking-time is about 6.6 μs with a loop bandwidth of 200 kHz. The performance comparison of proposed PLL with other related frequency synthesizers is listed in Table 1.

6. Conclusion

In this paper, a low power wide band LC-VCO frequency synthesizer for a hybrid GNSS receiver is designed and implemented by the standard 0.18 μm 1P6M CMOS process. An LC-VCO using tuning curve compensation achieves a wide tuning range, while it has low power consumption and low phase noise. The digital tuned dead zone and improved charge pump reduces reference spurs. The measured results show it satisfies the requirements of a portable hybrid civilian GNSS receiver. The proposed frequency synthesizer has been applied to a portable hybrid GNSS receiver.

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