A new static induction thyristor with high forward blocking voltage and excellent switching performances*

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Abstract: A new static induction thyristor (SITH) with a strip anode region and p^- buffer layer structure (SAP^-B) has been successfully designed and fabricated. This structure is composed of a p^- buffer layer and lightly doped n^- regions embedded in the p^+-emitter. Compared with the conventional structure of a buried-gate with a diffused source region (DSR buried-gate), besides the simple fabrication process, the forward blocking voltage of this SITH has been increased to 1600 V from the previous value of 1000 V, the blocking gain increased from 40 to 70, and the turn-off time decreased from 0.8 to 0.4 μs.

Key words: static induction thyristor; strip anode region and p^- buffer layer structure; forward blocking voltage; turn-off time

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1. Introduction

Static induction thyristor (SITH) is a new kind of power semiconductor device based on the static induction effect proposed by Nishizawa *et al.*[1]. Because of high switching speed, high di/dt and dv/dt capabilities, along with a low forward on-state voltage (V_{on}), SITH has been used in systems of energy accelerator, current-source inverter and high-frequency power conversion, etc.[2−6].

A high anode blocking voltage V_{AK} and switching speed are necessary parameters for SITH with good performance. In recent years, many interesting works have been done on fabricating different structures of SITH to improve its forward blocking and switching characteristics, such as anode-shorting pattern[7], shallow-junction pattern[8] and double-gate pattern[9]; the present work is an attempt in this direction.

Basic structural types of SITH had been developed in recent years, such as buried gate, surface gate, recessed gate[10], double dielectrics gate[11] and buried-gate with diffused source region (DSR buried-gate)[12]. Among these structures, the DSR buried-gate structure has the main merit of a simple technological process. A strip anode region and p^- layer structure (SAP^-B) has been firstly proposed in this paper, DSR buried-gate SITHs with SAP^-B structure were designed and fabricated. Compared with the conventional DSR buried-gate SITH, SITH with SAP^-B structure can further simplify fabrication process, efficiently increase anode blocking voltage V_{AK}, and decrease turn-off time t_{off}.

2. Device structure and fabrication

A schematic cross-sectional segment of a DSR buried-gate SITH with SAP^-B structure is shown in Fig. 1.

To comparatively study SITHs with the conventional structure (A-type) and the new structure (B-type), they are fabricated under the same technological conditions. The main processing steps for a SITH with the new structure are briefly described as follows.

(1) N-type floating zone (FZ) (111) oriented silicon wafers (ρ = 80 Ω·cm) are used as substrates.

(2) Low concentration boron impurities of 10^{16} cm^{-3} are diffused into the back side of the original wafers. The diffusion depth is about 50 μm.

(3) The lightly doped n-type epitaxial layers are grown on both sides of the wafers. The thicknesses of the front and back epitaxial layers are about 12 μm and 3 μm, respectively.

(4) A SiO_2 layer is thermally grown and selectively etched on the wafer, then the high concentration 10^{19} cm^{-3} born impurities are diffused into the original wafers at 1150 °C to form the gate stripes and limiting field rings. The diffusion depth is 10 μm and $R_{\square} \approx$ 30–40 Ω/□.

(5) The source region and channel stopper ring are formed by phosphorus diffusion on a large area at 1150 °C for 30 min, the diffusion depth is about 1.5 μm, and $R_{\square}$ = 3 Ω/□.

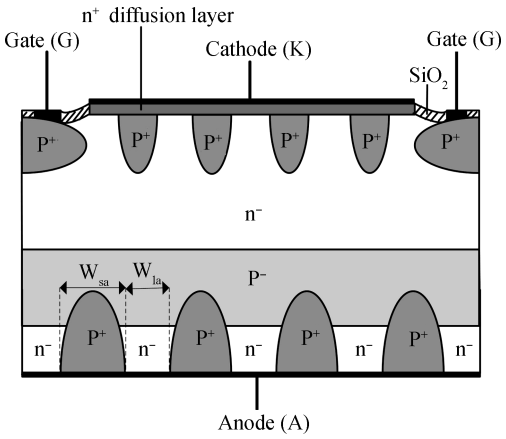

Fig. 1. Schematic cross-sectional view of a DSR buried-gate SITH with SAP^-B structure.

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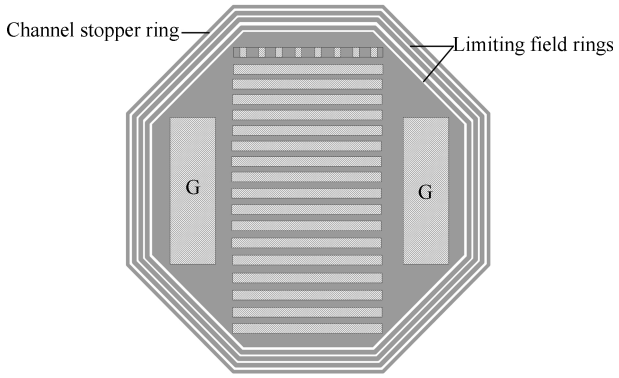

Fig. 2. Schematic top view of fabricated devices.

(6) The back sides of the wafers are oxidized and etched using the masking with strip shapes, then boron with high concentration of 10^{19} cm^{-3} is diffused into the strip shapes to form strip anode region, the back n^- epitaxial layer without doping is just the leakage anode region, the width of strip anode region W_{sa} is about 10 μm and that of leakage anode region W_{la} varies from about 2 to 8 μm.

(7) The Al–Ti–Pt metal electrodes of cathode, gate, anode are prepared by evaporation, sputtering and selective etching.

The back protection is not required during the epitaxial process, so it further simplifies the process compared with the DSR buried-gate structure. The schematic top view of the structure is shown in Fig. 2; three p^+ limiting field rings and one n^+ surface channel stopper ring are fabricated to improve the voltage performance[13]. The geometrical parameters of the device are described as follows: channel width $d = 16\mu$m, channel length $l_c = 10\mu$m, channel number $N_c = 816$, channel width $w = 1.63 \times 10^5 \mu$m, the chip diameter is 30 mm, cathode area $A_{cath} = 0.53$ cm^2, and active anode area of A-type $A_{an} = 7$ cm^2. The strip anode area of the B-type SITH varies from 5.6 to 1.4 cm^2.

3. Experimental results

The forward blocking and conducting as well as switching characteristics of the two types of fabricated SITHs were measured and compared.

3.1. Forward blocking characteristics

Figure 3 shows the forward blocking characteristics of the fabricated A- and B-type ($W_{la} = 7$ μm) SITH when the junction temperature T_j is 25 °C respectively, as a function of gate bias voltage, where the gate bias was changed by –5 V steps from –10 to –30 V.

The maximum forward blocking voltage V_{AK} of A-type SITH is 1000 V when the gate is reversely biased to –30 V, the blocking gain is 40; but for B-type SITH ($W_{la} = 7$ μm), when the gate reverse bias voltage is –30 V, the maximum V_{AK} is 1600 V, and the blocking gain is 70.

3.2. Forward conducting characteristics

Figure 4 shows the relationship between the on-state voltage $V_{on}$and the anode current I_A for the fabricated A- and B-type SITHs, respectively. It was measured at the junction temperature T_j = 25 °C. For A-type SITH, the value of V_{on} is 0.46 V

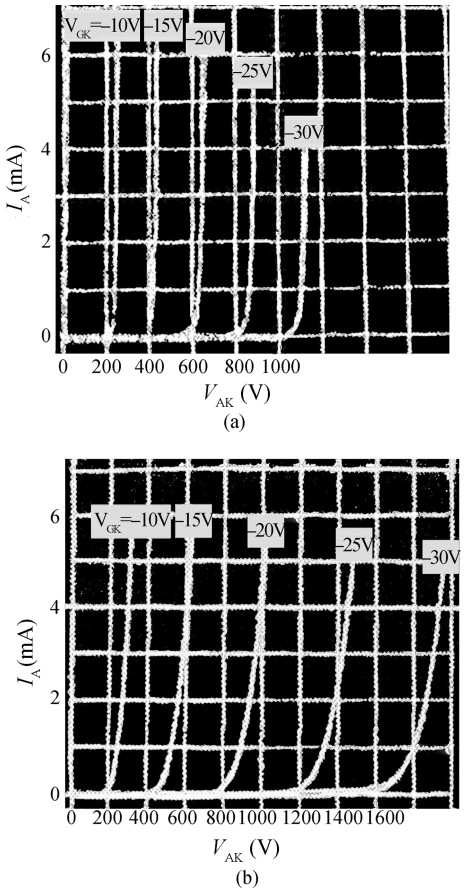

Fig. 3. Forward blocking characteristics of the fabricated A- and B-type SITH. (a) A-type. (b) B-type ($W_{la} = 7$ μm).

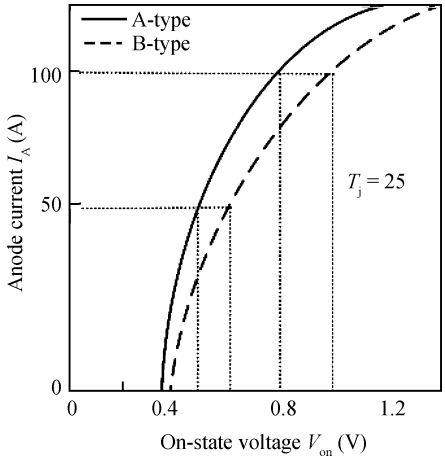

Fig. 4. Relationship between V_{on} and I_A for the A- and B-type (W_{la} = 7 μm) SITH.

at 50 A and 0.8 V at 100 A, while it is 0.6 V at 50 A and 1.0 V at 100 A for B-type SITH ($W_{la} = 7\mu$m), which demonstrates that SAP$^-$B structure may cause increase in V_{on} when $W_{la} = 7$ μm. The blocking voltage V_{AK} and conducting voltage V_{on} are all increased with the increase in W_{la} for constant width of strip anode region W_{sa} as shown in Fig. 5. Therefore, W_{la} should be appropriately chosen to obtain a good trade-off between V_{AK} and V_{on}.

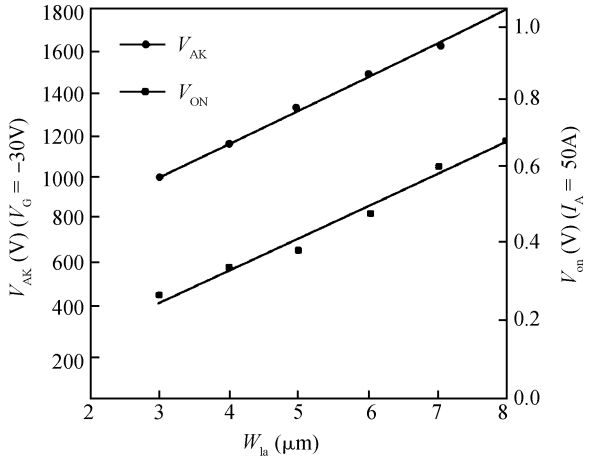

Fig. 5. Influence of W_{la} on V_{AK} and V_{on} for SAP^{-}B structure.

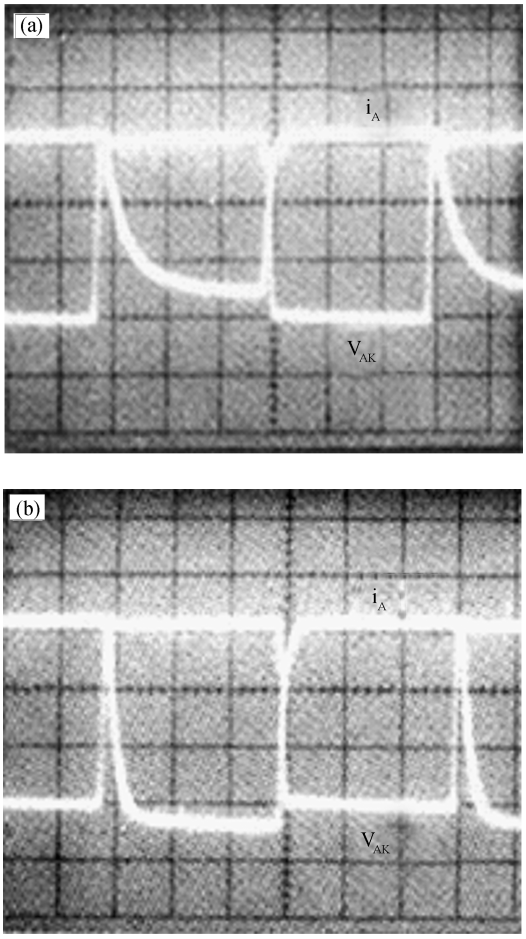

Fig. 6. Turn-on, turn-off waveforms of i_A and V_{AK} for A- and B-type SITHs. i_A: 20 A/div, V_{AK}: 200 V/div, Time: 1 μs/div. (a) A-type. (b) B-type (W_{la} = 7 μm).

3.3. Switching characteristics

Figures 6(a) and 6(b) show typical switching waveforms of the anode current i_A and anode voltage V_{AK} for A- and B-type SITHs, respectively. The turn-off time t_{off} of the A-type thyristor is 0.8 μs and that of the B-type thyristor is t_{off} = 0.4 μs. The experimental results demonstrate that newly designed SITH with SAP^{-}B structure has more excellent switching performance than the conventional one.

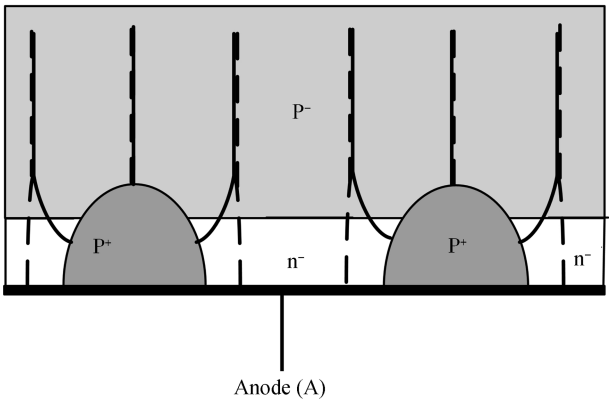

Fig. 7. Schematic diagram for "electron leakage" effect of n^{-} leakage anode region in SAP^{-}B structure. The solid line is for current of holes, and the dash line is for current of electrons.

4. Discussion

SITH with DSR buried-gate structure is composed of a parasitical bipolar transistor (BJT) and a static induction transistor (SIT). In forward blocking state, the anode acts as the emitter of the BJT. The anode blocking voltage V_{AK} is just the breakdown voltage of BTJ when the base terminal is open. Anode injection efficiency γ of holes has an important effect on V_{AK}. For B-type SITH, with existing of p^{-} layer and n^{-} leakage anode region, a part of holes injected from p^{+} region will recombine with electrons in p^{-} layer and depletion regions in p^{+}p^{-} and p^{+}n^{-} junctions. Furthermore, p^{+}p^{-} high-low junctions have some reflection effects on minority carriers, so γ of B-type SITH is lower and V_{AK} is higher than that of A-type SITH. At the same time, a decrease in γ will result in an increase in V_{on} as shown in Fig. 4. Figure 5 shows the influence of W_{la} on V_{AK} and V_{on} for or SAP^{-}B structure. When W_{sa} is a constant, the larger W_{la}, the larger area of the leakage anode region, the more recombination of holes injected from p^{+} region in leakage anode region, the smaller the γ, the larger V_{AK} and V_{on}. In order to obtain optimum electrical performances, the width of leakage anode region W_{la} should be appropriately chosen to acquire a good trade-off between V_{AK} and V_{on}.

In drifting and buffer regions far from the anode, the charge-neutrality condition requires the same density of electrons and holes, current lines of electrons overlap that of holes, each providing half of the anode current. In the buffer region near the anode, because of the different potentials of the strip anode region and leakage anode region, electrons separate from holes, current of holes flows from p^{+} strip anode region into drift region while current of electrons flows from drift region into n^{-} leakage anode region, leakage anode region has an effect of "electron leakage", this effect is schematically shown in Fig. 7. During the turn-off process, the "electron leakage" effect of the leakage anode region accelerates the absorbing action on accumulated charges in drift region during on-state. In addition, there are p^{-} buffer layer and n^{-} leakage anode regions in SAP^{-}B structure, charge density near the anode is lower, these respects are all advantageous to speed turn-off

time, which can be demonstrated from Fig. 6.

5. Conclusion

A special anode-side design SAP$^-$B of SITH has been proposed. The structure is characterized by a p^- buffer layer and lightly doped n^- type regions embedded in the p^+-emitter. Experimental results show that SAP$^-$B is a promising structure for improving the forward blocking and switching characteristics of SITH. Experimental samples adopted the SAP$^-$B DSR buried-gate structure, SAP$^-$B structure can also be applied to other basic structural types of SITH to obtain excellent forward blocking and switching properties.

References

[1] Nishizawa J, Terasaki T, Shibata J. Field effect transistor versus analog transistor (static induction transistor). IEEE Trans Electron Devices, 1975, ED-22(4): 185

[2] Shimizu N, Miyoshi M, Tange S, et al. High speed turn-on reverse conducting 4 kV static induction thyristors based on the buried gate type p-base n-emitter soft contact structure and anti-parallel diodes for solid-state power supplies in high energy accelerators. Solid-State Electron, 2006, 50: 1567

[3] Muraoka K, Kawamura Y, Ohtsubo Y, et al. Characteristics of the high-speed SITH and its application to the 60-kHz 100-kW high-efficiency inverter. IEEE Trans Power Electron, 1989, 4(1): 92

[4] Peng F Z, Akagi H, Nabae A, et al. High-frequency current-source inverters using SITHs for induction heating applications. IEEE Trans Ind Appl, 1989, 25(1): 172

[5] Nishizawa J. Application of power static induction (SI) devices. Int PCIM Proc Papers, 1988: 1

[6] Nakajrnura Y. Very high speed static induction thyristor. IEEE Trans Ind Appl, 1986, IA(22): 1000

[7] Tomoyoshi K, Hiroshi T, Shoji H, et al. Low-loss high-power static induction thyristors for complementary circuits. IEEE Trans Ind Appl, 1988, 24: 132

[8] Liu G, Yu Y H, Shi J Q, et al. Semiconductor devices. Beijing: Electronics Industry Publishing House, 2000 (in Chinese)

[9] Nishizawa J, Yukimoto Y, Kondou H, et al. A double-gate-type static-induction thyristor. IEEE Trans Electron Devices, 1987, ED-34(6): 1396

[10] Nishizawa J, Motoyan K, Itioh A. The 2.45 GHz 36 W CW Si recessed gate type SIT with high gain and high voltage operation. IEEE Trans Electron Devices, 2000, 47(2): 482

[11] Wang Y S, Li S Y, Hu D Q. A microwave high power static induction transistor with double dielectrics gate structure. Chinese Journal of Semiconductors, 2004, 25: 19

[12] Wang Y S, Li S Y, Yang J H, et al. A novel buried-gate static induction transistor with diffused source region. Semicond Sci Technol, 2004, 19: 152

[13] Wang Y S, Li H R, Wang Z T, et al. Improvements on high voltage performance of power static induction transistors. Journal of Semiconductors, 2009, 30(10): 104003