A 1.1 mW 87 dB dynamic range ΔΣ modulator for audio applications*

Liu Liyuan(刘力源)[1], Chen Liangdong(陈良栋)[2], Li Dongmei(李冬梅)[2,†], Wang Zhihua(王志华)[1], and Wei Shaojun(魏少军)[1]

(1 Institute of Microelectronics, Tsinghua University, Beijing 100084, China)
(2 Department of Electronic Engineering, Tsinghua University, Beijing 100084, China)

Abstract: This paper presents a 1.1 mW 87 dB dynamic range third order ΔΣ modulator implemented in 0.18 μm CMOS technology for audio applications. By adopting a feed-forward multi-bit topology, the signal swing at the output of the first integrator can be suppressed. A simple current mirror single stage OTA with 34 dB DC gain working under 1 V power supply is used in the first integrator. The prototype modulator achieves 87 dB DR and 83.8 dB peak SNDR across the bandwidth from 100 Hz to 24 kHz with 3 kHz input signal.

Key words: ΔΣ modulator; feed-forward; low power; low voltage; multi-bit
DOI: 10.1088/1674-4926/31/5/055003 **EEACC:** 1265H

1. Introduction

Portable consumer electronics such as mobile phones, digital hearing aids, and digital recorders, drive the development of the modern integrated circuits industry. Powerful DSP engines are integrated into these systems but high resolution interfaces are needed to digitize the signal from the real word. The oversampling and noise-shaping mechanisms make the ΔΣ modulator based interface a suitable candidate because it can achieve high resolution without stringent accuracy requirements on the analog components. Recently, the design of a ΔΣ modulator under 1-V or sub-1-V power supply with several hundred micro-watts power consumption has been the trend due to the following two reasons: firstly, the scaling down transistors must work under low voltage to ensure reliability; secondly, the circuits should consume less power to extend the battery lifetime[1−3].

But the low supply voltage has brought great difficulties in designing high resolution modulators with low power consumption. The switched capacitor integrator is a fundamental building block of the ΔΣ modulator. Normally the first stage integrator is the most important because its noise and distortion limit the overall performance of the modulator. The ideal power consumption of the switched-capacitor integrator has been derived in Ref. [4]. Although many assumptions are made, the derivation still gives us the basic relation between the power, speed, accuracy and supply voltage. If the same dynamic range is to be achieved, the design under low voltage conditions may consume more power. The best way to save power is to maximize the input signal range. The multi-bit topology which exhibits better stability than its single-bit counterpart will be a good choice.

Another bottleneck under low voltage design is that the non-linear OTA gain effect which will distort the modulator output becomes difficult to overcome. In conventional design, the non-linear gain effect is dealt with by making the DC gain of the operational trans-conductance amplifier (OTA) as high as possible, but this is not very feasible under low voltage and low power constraints. Due to the limited voltage headroom, the cascode technique can not be used to enhance the gain, and if cascade topology is used, extra currents are needed to stabilize the OTA. One way to solve the problem is finding a topology in which the signal swing of each integrator can be suppressed so that even if the gain is low, the non-linearity gain effect will not deteriorate the performance of the modulator. The topology with feed-forward path is very suitable[5−7].

In this work, a 1.1 mW 87 dB dynamic range third order ΔΣ modulator is implemented in 0.18 μm CMOS technology for audio applications. By adopting a feed-forward multi-bit topology, the signal swing at the output of the first integrator can be suppressed while only one simple current mirror single-pole OTA with 34 dB DC gain working under 1 V power supply is used in the first integrator. The prototype modulator achieves 87 dB DR and 83.8 dB peak SNDR across the bandwidth from 100 Hz to 24 kHz with 3 kHz input signal.

Section 2 discusses the details of the architecture. The non-linear OTA gain effect is modeled and simulated. Section 3 presents the circuit building block design. The noise contribution is calculated. Section 4 shows the die photograph and the experimental results. Section 5 gives conclusions and some comments on this design.

2. Architecture

The system architecture of the ΔΣ modulator is shown in Fig. 1[8]. It is a third order topology with an 18-level quantizer. The oversampling ratio (OSR) is chosen as 64. Since the audio bandwidth is from 20 Hz to 24 kHz, the sampling frequency is set to 3.072 MHz. The reasons for choosing this architecture are as follows: firstly, the distributed feedback paths help to make the overall modulator performance insensitive to the tolerance of the analog components making up every integrator. Secondly, the feed-forward paths are added in order to reduce the signal swing of the first integrator, and this will greatly relax the gain requirements of the OTA which leads to the use of

* Project supported by the National High Technology Research and Development Program of China (No. 2008AA010700).
† Corresponding author. Email: lidmei@tsinghua.edu.cn
Received 26 September 2009, revised manuscript received 4 January 2010

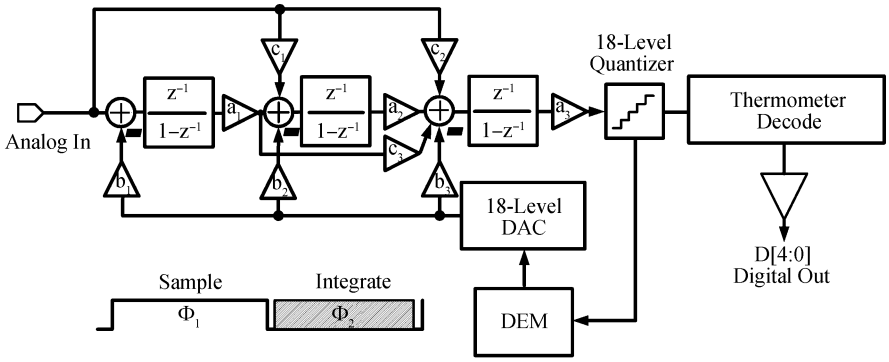

Fig. 1. System architecture.

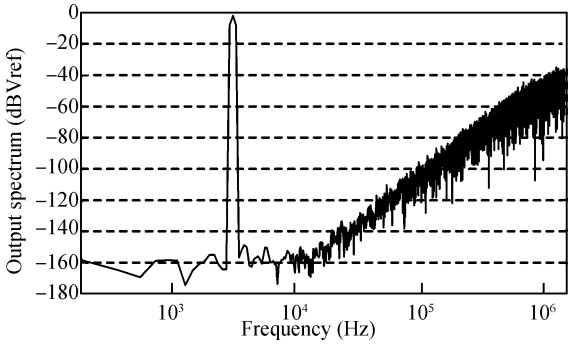

Fig. 2. Spectrum of the ideal modulator.

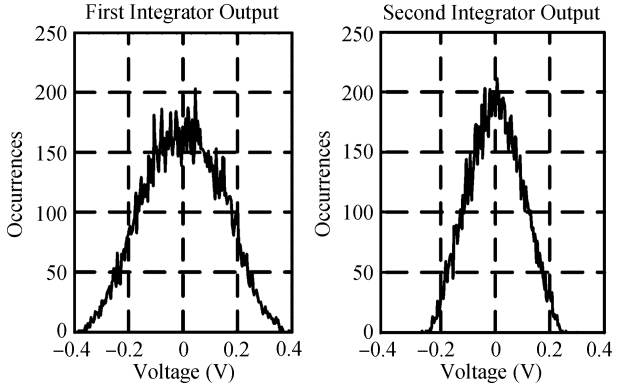

Fig. 3. Histograms of the first and second integrators.

low gain but power efficient single stage OTA . Thirdly, the use of a multi-level quantizer enhances the stability and enlarges the input overload level of the modulator; an additional benefit is that the multi-level quantizer introduces less quantization noise which is also helpful to the swing reduction.

If the coefficients of the modulator satisfy the following equations: $b_1 = (a_1a_2a_3)^{-1}$, $b_2 = (3a_2 - c_3)a_2^2a_3$, $b_3 = -3/a_3, c_1 = a_1(3a_2 - c_3)/a_2$ and $c_2 = 3a_1a_2$, the noise transfer function (NTF), the signal transfer function (STF) and the z-transform of the output of each integrator can be expressed by the following equations.

$$\mathrm{STF} = \frac{-a_1a_2a_3(-3z^2 + 3z - 1)}{z^3}, \tag{1}$$

$$\mathrm{NTF} = \frac{(z-1)^3}{z^3}, \tag{2}$$

$$O_1(z) = \frac{a_1(z-1)^2}{z^3}X(z) + \frac{a_1b_1(z-1)^2}{z^3}Q(z), \tag{3}$$

$$O_2(z) = \frac{a_2c_1(z-1)^2 + a_1a_2(z-1)}{z^3}X(z) + \frac{a_2b_2(z-1)^2 + a_1a_2b_1(z-1)}{z^3}Q(z), \tag{4}$$

$$O_3(z) = \frac{a_1a_2a_3(-3z^2 + 3z - 1)}{z^3}X(z) + \frac{(z-1)^3}{z^3}Q(z) - Q(z). \tag{5}$$

In this design, $a_1 = 1.5, a_2 = 0.7, a_3 = 5/6$ and $c_3 = 1$ are chosen. Other coefficients are obtained using the relations above. These coefficients allow the modulator to have an overload level of 0.9. 16 384 points MATLAB simulation of the system is performed. The references of the modulator are chosen as 2 $V_{pp-diff}$. The input signal is a 1.6 $V_{pp-diff}$ sine wave. The sampling clock frequency expressed as f_s is 3.072 MHz, and the frequency of the input signal is $7f_s/16384$. The output spectrum is shown in Fig. 2 and histograms of the first and second integrators are shown in Fig. 3. The simulation result indicates that the modulator can achieve an ideal 129 dB signal to quantization noise ratio.

The output of the first integrator and the second integrator are restricted to ± 0.4 V and ± 0.3 V respectively as shown in Fig. 3. From the histogram we find that the outputs exhibit a Gaussian distribution. This can be explained by Eqs. (3) and (4), in which the signal component $X(z)$ is filtered by a high pass transfer function $(z-1)^2$ or $(z-1)$. Because the spectrum of the signal concentrates in a small range from DC to $f_s/(2 \cdot \mathrm{OSR})$, it will be greatly attenuated by $(z-1)^2$ or $(z-1)$, so the signal component $X(z)$ seems to be removed from the output, and only the quantization $Q(z)$ takes effect. Because there are few signal components in the output of the first integrators, it is reasonably assumed that an OTA with low gain can be used to construct the integrator and this assumption will be proved by the following simulations.

The switched-capacitor realization of the integrator is shown in Fig. 4. If the OTA exhibits an infinite gain, the transfer function of the circuit can be expressed as

$$H(z) = \frac{C_s}{C_f}\frac{z^{-1}}{1 - z^{-1}}. \tag{6}$$

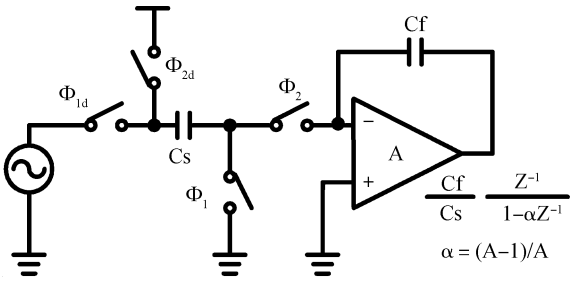

Fig. 4. Switched-capacitor realization of the integrator.

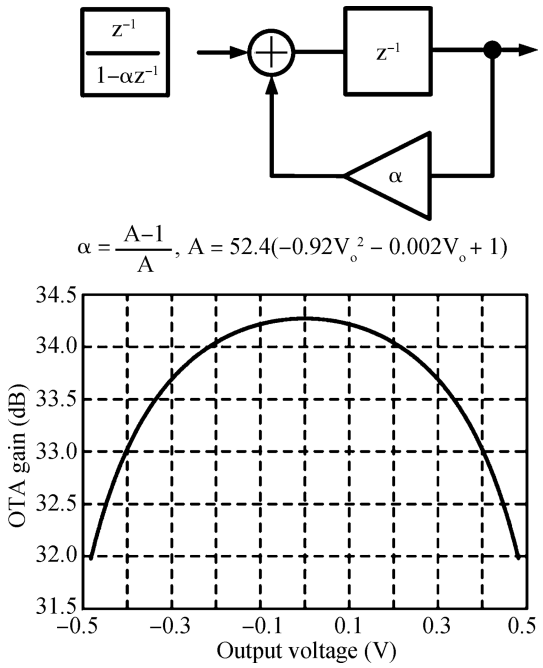

Fig. 5. Modeling of the non-linear gain effect of the integrator.

However, the OTA inside the integrator always has finite gain. Suppose the OTA has a gain of A, and the transfer function (6) can be expressed as

$$H(z) = \frac{C_s}{C_f}\frac{z^{-1}}{1-\alpha z^{-1}}, \quad \alpha = \frac{A-1}{A}. \tag{7}$$

The factor α is not constant because the OTA gain varies non-linearly with the output voltage of the OTA. To simulate the non-linear OTA gain effect of the system using MATLAB, the integrator in Fig. 4 is modeled as shown in Fig. 5. The curve in Fig. 5 reveals the relation between the gain and the output voltage of a current mirror OTA which is going to be used in the first integrator. The curve is obtained by performing a DC sweep analysis with Spectre. The polynomial fit method is adopted to find the non-linear relation between the OTA gain and the OTA output. The relation is expressed as Eq. (8). The circuit description of the OTA will be given later in Section 3.

$$A = 52.4 \times (-0.92V_o^2 - 0.002V_o + 1). \tag{8}$$

Using the above relation the modulator is simulated and the output spectrum is shown in Fig. 6. The quantization noise floor is raised compared to Fig. 2, but it still achieves 108 dB

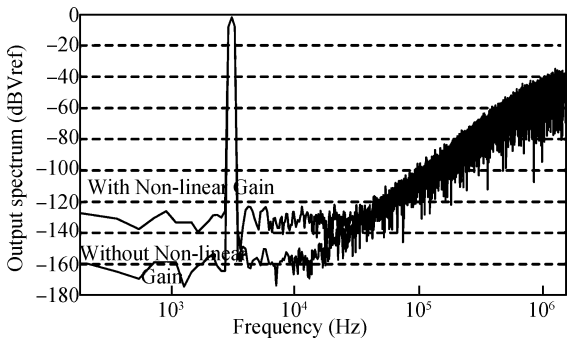

Fig. 6. Output spectrum of the modulator with non-linear OTA gain.

signal-to-quantization noise ratio. This is enough for 16-bit resolution design. The simulation result reveals the fact that the feed-forward path in the architecture alleviates the non-linear gain effect. The low-gain but power-efficient current mirror OTA can be used to construct the first integrator.

3. Circuit design

The circuit of the third-order discrete time modulator is depicted in Fig. 7. It consists of three switched-capacitor integrators, eighteen comparators, one DEM block, one two-phase non-overlapping clock generator and one switched-capacitor 18-level D/A converter. The analog part and the digital control part work at 1 V supply. The reference voltages are selected as 1 V and 0 V. Voltage shift circuits are added between the digital logic and the analog switches to shift the high level voltage from 1 to 1.8 V in order to make the switches conduct thoroughly. The unit capacitances of every integrator are $20 \times 20\ \mu m^2$, $12 \times 12\ \mu m^2$, $10 \times 10\ \mu m^2$ which are approximately 400 fF, 144 fF and 100 fF respectively. All the integrators sample at phase 1 (Φ_1) and integrate at phase 2 (Φ_2). The 18-level quantizer is flash based, which consists of 18 identical comparators. The quantizer samples the output of the last integrator at Φ_2, makes a decision at the neighboring Φ_1 and gives the corresponding thermometer code. During the rest time of Φ_1 the DEM also generates the DWA shifted code. In the next Φ_2, the switches of the D/A will turn to the positive reference or the negative reference according to the DWA shifted code.

3.1. Thermal noise

Every integrator generates thermal noise and raises the noise floor of the modulator. The noise contributed by the first integrator is the most important. In this section the thermal noise of the first integrator is calculated using the method proposed in section 8, chapter 3 of Ref. [9]. There are four noise sources. They are the noise from the sample switch and feedback switch at Φ_1 and Φ_2, the noise from the OTA and the noise from the reference voltage. In this design the reference voltages are generated by off-chip circuits, in which large titanium capacitors are used to regulate the voltage, so the noise generated by the references can be negligible and is not considered in the calculations. Normally the resistances of both the sampling and feedback switches are designed to be low enough to avoid distortion. So the time constant formed by these resistances and the sampling capacitor is much smaller than the OTA charging time constant in both states. Under this condition the noise from

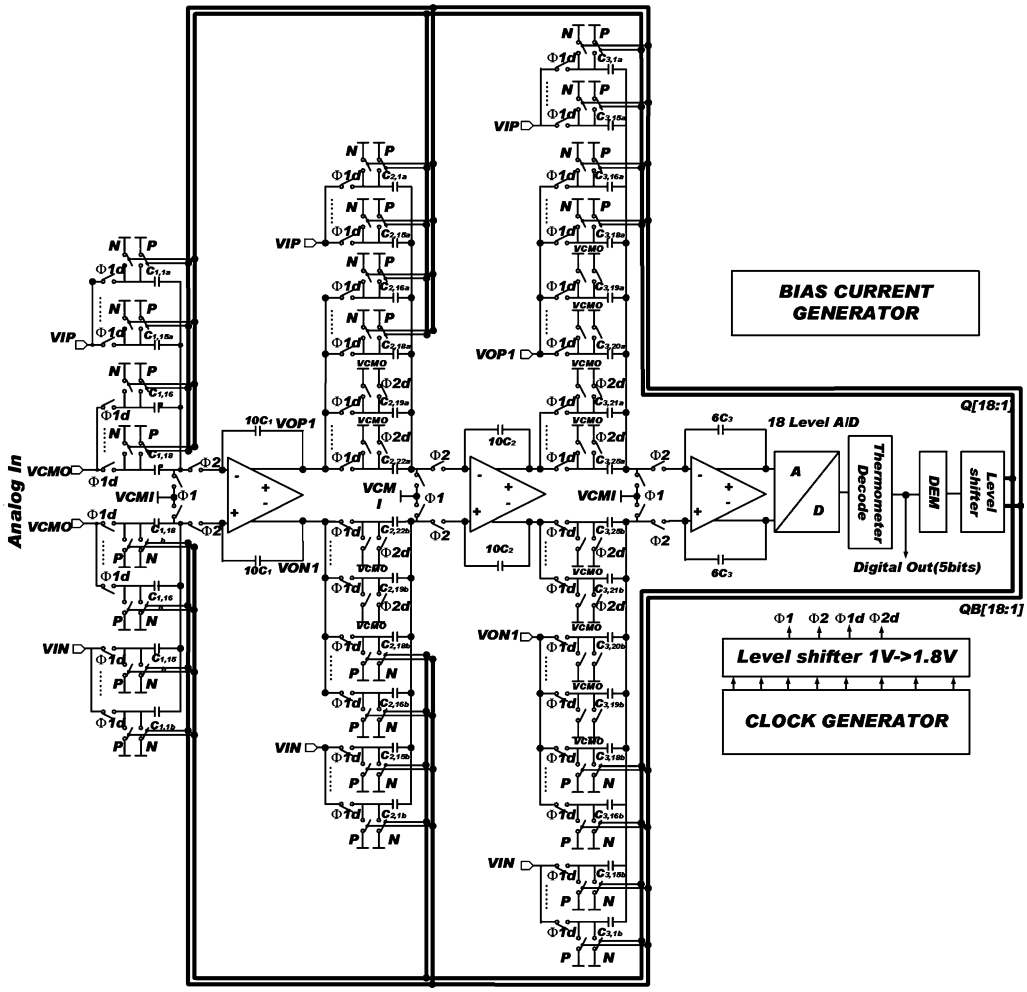

Fig. 7. Switched capacitor realization of the third-order modulator.

the above sources can be expressed by the following equations.

$$N_{\mathrm{S}} = \frac{2kT}{\mathrm{OSR}\cdot C_{\mathrm{s}}}, \tag{9}$$

$$N_{\mathrm{F}} = \frac{2kT}{\mathrm{OSR}\cdot C_{\mathrm{s}}}\frac{C_{\mathrm{eq,cl1}}}{C_{\mathrm{eq,cl2}}}\frac{\rho_1^2}{\rho_2^2}, \tag{10}$$

$$N_{\mathrm{OTA}} = \frac{2kT}{\mathrm{OSR}\cdot C_{\mathrm{s}}}\frac{C_{\mathrm{s}}}{C_{\mathrm{eq,cl2}}}\frac{2}{3}\frac{\gamma}{\rho_2}. \tag{11}$$

N_{S} is the noise generated by the switch at the sampling phase; N_{F} corresponds to the noise from the switch at phase 2; N_{OTA} is the OTA thermal noise. In these equations the factor k is Boltzmann's constant which is 1.38×10^{-23} J/K, T is the absolute temperature which is 300 K in the calculations and OSR is 64 as mentioned previously. C_{s} is the sampling capacitor. In Fig. 7 the input sampling network is composed of 18 unit capacitors corresponding to a total sampling capacitance of 7.2 pF. $C_{\mathrm{eq,cl1}}$ and $C_{\mathrm{eq,cl2}}$ are equivalent load capacitors when the integrator is at Φ_1 and Φ_2 respectively. ρ_1 and ρ_2 are factors which are very close to 1. γ is the noise excess factor for the current mirror OTA in the first integrator.

The OTA performs the function of charge transferring from the sampling capacitor to the integration capacitor on phase 2 and holds the charge on phase 1. So the equivalent capacitor during phase 2 ($C_{\mathrm{eq,cl2}}$) is approximately the value of C_{s}, which means $C_{\mathrm{eq,cl2}} \approx C_{\mathrm{s}}$, and is significant larger than $C_{\mathrm{eq,cl1}}$ of phase 1, that is $C_{\mathrm{eq,cl2}} \gg C_{\mathrm{eq,cl1}}$. Using these approximations, the noise can be expressed as:

$$N_{\mathrm{T}} = N_{\mathrm{s}} + N_{\mathrm{F}} + N_{\mathrm{OTA}} \approx \frac{2kT}{\mathrm{OSR}\cdot C_{\mathrm{s}}}\Big(1+\frac{2}{3}\gamma\Big). \tag{12}$$

The current mirror OTA shown in Fig. 8 will be used to construct the first integrator. The thermal noise power contributed from each transistor has been derived and expressed as:

$$V_{\mathrm{nOTA}}^2 = \frac{16kT}{3g_{\mathrm{m1a}}}\gamma,\ \gamma = \Big(1+\frac{g_{\mathrm{m2a}}}{g_{\mathrm{m1a}}}+\frac{(g_{\mathrm{m3a}}+g_{\mathrm{m4a}})g_{\mathrm{m2a}}^2}{g_{\mathrm{m1a}}g_{\mathrm{m3a}}^2}\Big). \tag{13}$$

In this design, all the transistors have been designed to have the same overdrive voltage of about 100 mV. In this case $g_{\mathrm{m1a}} \approx g_{\mathrm{m2a}} \approx \frac{1}{2}g_{\mathrm{m3a}} \approx \frac{1}{2}g_{\mathrm{m4a}}$ and the noise excess factor γ is about 3. The total noise can now be evaluated as:

$$N_{\mathrm{T}} \approx \frac{2kT}{\mathrm{OSR}\cdot C_{\mathrm{s}}}\Big(1+\frac{2}{3}\gamma\Big) = \frac{6kT}{\mathrm{OSR}\cdot C_{\mathrm{s}}}. \tag{14}$$

The maximum amplitude of the input signal to the modulator is determined by the overload level and the reference which is $\mathrm{OL}\cdot V_{\mathrm{r}}$, so the thermal noise determined signal to noise ratio

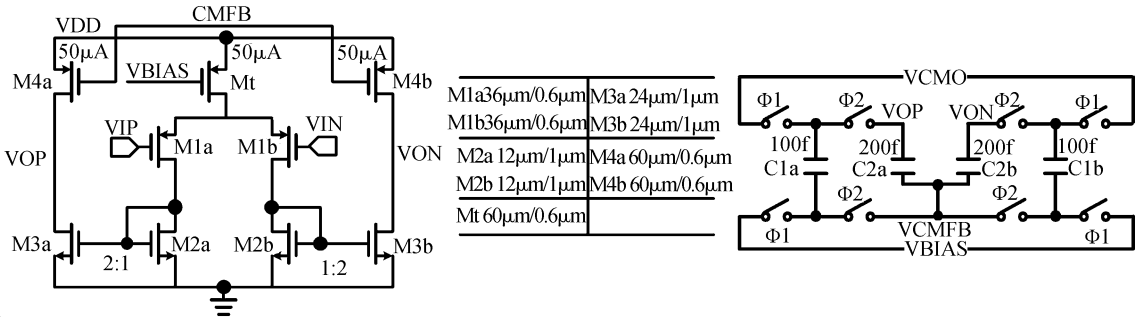

Fig. 8. Current mirror OTA for the first integrator.

Table 1. Switch size for the integrators (unit: μm).

	1st integrator	2nd integrator	3rd integrator
Φ_1	36/0.18	18/0.18	12/0.18
Φ_{1d}	36/0.18	18/0.18	12/0.18
Φ_2	2/0.18	2/0.18	2/0.18
Φ_{2d}, P, N	2/0.18	2/0.18	2/0.18

is:

$$\mathrm{SNR}_{\mathrm{KT/C}} = \frac{(\mathrm{OL}\cdot V_{\mathrm{r}})^2 \cdot \mathrm{OSR}\cdot C_{\mathrm{s}}}{12kT}. \tag{15}$$

A 7.2 pF sampling capacitor is large enough to give a 98 dB signal to thermal noise ratio with OL = 0.9, V_{r} = 1 V ($2V_{\mathrm{pp-diff}}$) and OSR = 64.

3.2. Switches

The purpose of the switch is to pass the charge to the capacitor connected to it. The non-zero resistance of the switch and the capacitor forms a time constant which will slow down the charge transferring. This on-resistance of the switch should be made small enough to ensure sufficient settling. Complementary switches are used all through the design. The standard power supply for 0.18 μm CMOS technology is 1.8 V. Since the digital part is designed to work under 1 V, the driving voltage of the switch is not enough and this will increase the on-resistance of the switch drastically. To guarantee the low on-resistance the clock boosters are added, which raise the high level voltage of the control signal from 1 to 1.8 V. The sizes of the switches are chosen according to their different purposes. In all the switches the NMOS and PMOS transistors are set to the same dimensions to reduce the clock feedthrough effect. The sizes of switches with different control signals are listed in Table 1. The sampling switches of the first integrator are the most important, and are sized to 36 μm/0.18 μm. The on-resistance is below 90 Ω, with the control signal boost driver. The sampling switches for the other two stages are scaled to small dimensions because the non-idealities caused by the switch will be suppressed by the gain of the previous stages. The dimensions of the other switches are set to 2 μm/0.18 μm which is much smaller than the sampling switches because these switches are always connected to a constant stable voltage such as the reference voltage or the common mode input voltage.

3.3. OTAs

The OTA of the first integrator shown in Fig. 8 employs simple current mirror topology with 34 dB DC gain and the quiescent current is designed to be 150 μA. The switched capacitor common mode feedback is used to stabilize the common mode voltage of the OTA. The output common mode voltage is set to be 0.5 V which is half of the supply voltage. The input common mode voltage is set to be 0.15 V. Figure 9 shows the transient settling of the first integrator. The OTA is able to settle during both phases.

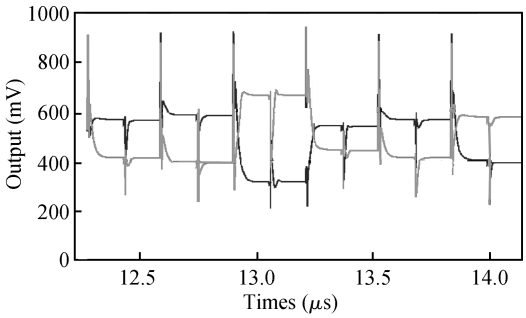

Fig. 9. Transient settling of the first stage OTA.

The OTAs for the second and third stages employ a two-stage Miller amplifier as shown in Fig. 10. Because the noise contributed by the second and third stages can be suppressed by the transfer function of the preceding stages, the capacitor sizes of these two stages are scaled down aggressively, which makes the Miller amplifiers capable of driving them with small currents. The common mode input voltage is also 0.15 V for both of the OTAs and the common mode feedback circuit is the same as that in the first OTA.

3.4. Comparator

The output of the third integrator is fed to an 18-level flash A/D shown in Fig. 7 for quantization. The output thermometer codes are generated by comparing the integrator output with 17 evenly divided decision levels between the positive reference and the negative reference. Since the minimum interval between two adjacent decision levels is only 55 mV, it will degrade the overall performance if the offset of the comparator is larger than this interval. In order to overcome this issue, the comparator shown in Fig. 11 is adopted which is reported in Ref. [10]. This structure has a pre-amplifier before the regeneration latch, which effectively reduces the offset caused by the latch. The only cost of the comparator is that there is voltage headroom consumption from the power supply to the input of the comparator which is about 0.8 V for a 0.18 μm regular threshold device. So in this design the voltage of the

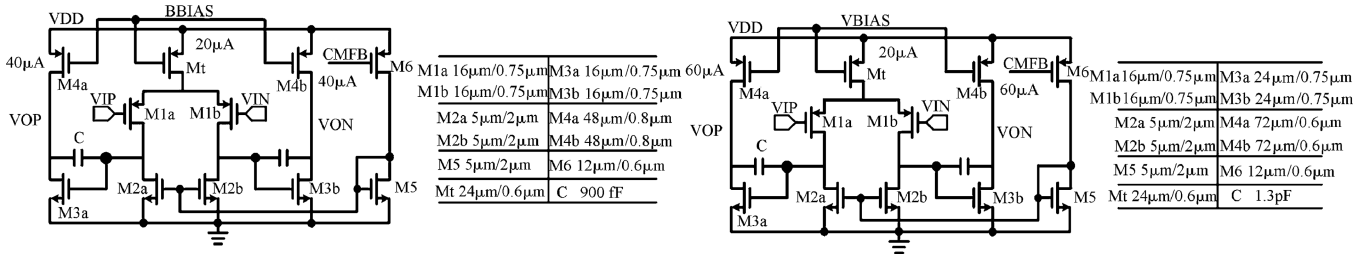

Fig. 10. OTAs for the second and third integrators.

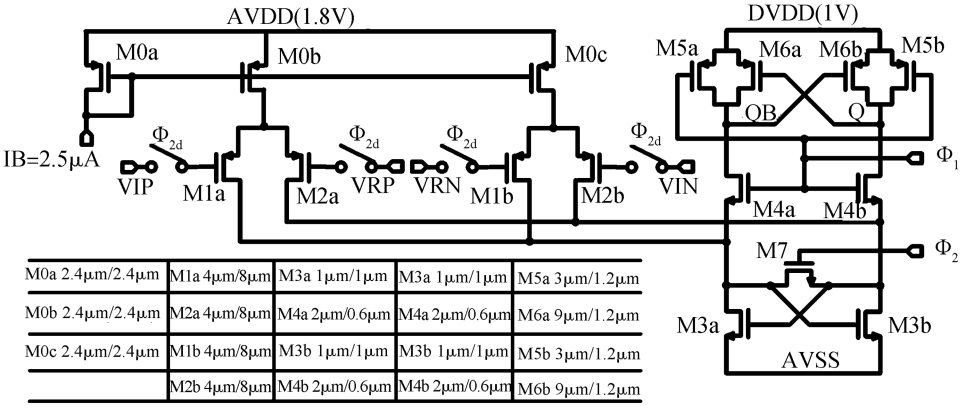

Fig. 11. Comparator.

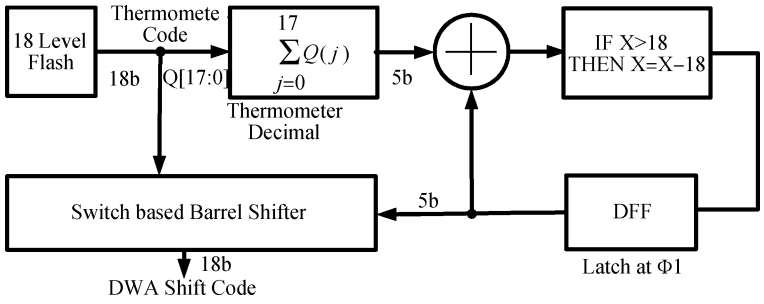

Fig. 12. Block diagram of the DWA logic block.

comparator supply is raised to 1.8 V to guarantee the operation of all the comparators.

3.5. DEM

The DEM logic is an indispensable part in the multi-bit $\Delta\Sigma$ modulator whose function is to alleviate the mismatch between the capacitors in the feedback DAC which will introduce distortion. The DEM block diagram is illustrated in Fig. 12. Thanks to the DWA method[11], the circuits for implementing such algorithms are quite simple. The 18-bit thermometer code from the 18-level quantizer is fed into a barrel shifter and a decoder. By adding all the 18-bit codes together, the decoder can convert the thermometer codes to their decimal format, which will be further accumulated. According to the final result, the barrel shifter generates the DWA shifting code which will control the feedback switches of each stage. The barrel shifter is realized using switch based logic instead of combination logic because of the low power consumption.

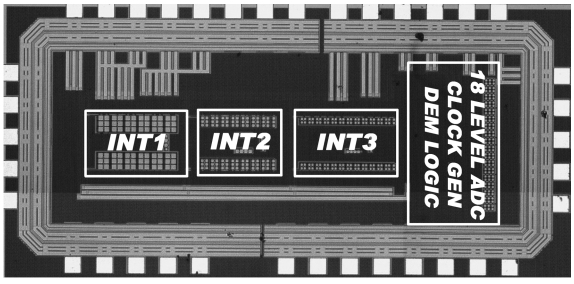

Fig. 13. Die photograph of the modulator.

4. Experimental Results

The third-order $\Delta\Sigma$ modulator was fabricated in 0.18 μm 1P6M CMOS technology. The die photograph is shown in Fig. 13. The total die area including pads is 2.2×1.0 mm^2.

The differential input sinusoidal signal is provided by a DS360 ultralow distortion function generator. The output dig-

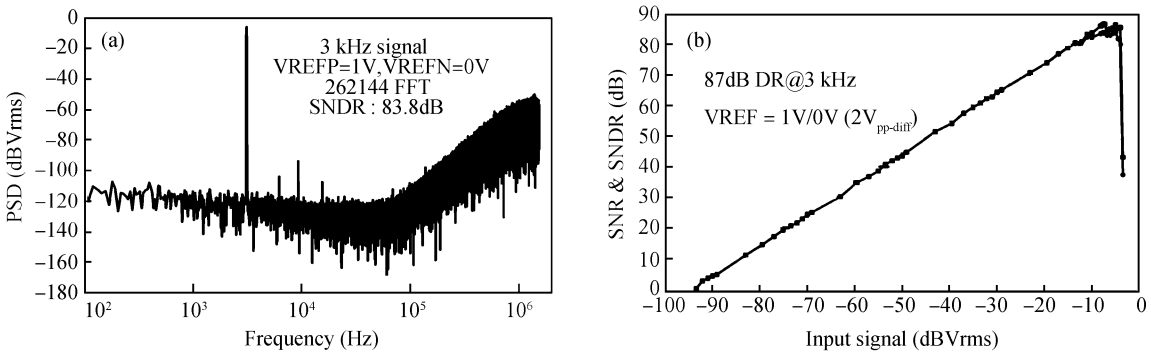

Fig. 14. (a) Measured peak SNDR and (b) SNDR plot versus input signal level.

Table 2. Measured performance summary of the $\Delta\Sigma$ modulator.

Parameter	Value
Peak SNDR	83.8 dB
Dynamic range	87 dB
Sampling rate	3.072 MHz
Over sampling ratio	64
Signal band	100 Hz–24 kHz
Supply voltage	1 V/1.8 V
Total power consumption	1.1 mW
FOM	1.8 pJ/step
Total area including pad	2.2×1.0 mm^2
Technology	UMC 0.18 μm 1P6M CMOS

ital codes are captured by an Agilent logic analyzer. The clock is generated from a 3.072 MHz crystal, the 1 V power supply is generated by LT3021, and the 1.8 V supply is generated by LT3024. The reference voltages are generated by AD780, and operational amplifier OPA350s are used as buffers. The peak SNDR measurement of the modulator is shown in Fig. 14(a). The peak SNDR reaches 83.8 dB with a 3 kHz input. The SNR and SNDR plots with input level are shown in Fig. 14(b). The dynamic range of the modulator is 87 dB. A summary of the measured performance is shown in Table 2.

5. Conclusion and future work

A 1.1 mW 87 dB dynamic range third order $\Delta\Sigma$ modulator is implemented in 0.18 μm CMOS technology for audio applications. Feed-forward topology with a multi-bit quantizer is adopted. The signal swing at the output of the first integrator is suppressed and only one simple current mirror single stage OTA with 34 dB DC gain working under 1 V power supply is used in the first integrator. The prototype modulator achieves 87 dB DR and 83.8 dB peak SNDR across the bandwidth from 100 Hz to 24 kHz with 3 kHz input signal.

According to the measurement results, the dynamic range is limited to 87 dB but the theoretical maximum signal to thermal noise ratio is 98 dB. The extra noise is mainly the flicker noise generated by the OTA of the first stage. In this design no technique is used to remove this low frequency noise. The power consumption is still high and the FOM is only 1.8 pJ/step which is not state-of-the-art. There are still some circuits working under high voltage. To solve these problems, some future work is to be done. Firstly, chopper stabilization techniques or correlated double sampling techniques should be adopted in the design to remove the flicker noise. Secondly, comparators suitable for 1 V operation with low offset should be developed. Thirdly, the building blocks should be optimized to reduce unnecessary power consumption.

References

[1] Roh J, Byun S, Choi Y, et al. A 0.9-V 60 μW 1-bit fourth-order delta–sigma modulator with 83-dB dynamic range. IEEE J Solid-State Circuits, 2008, 43(2): 361

[2] Park H, Nam K, Su D K, et al. A 0.7-V 100-dB 870 μW digital audio $\Sigma\Delta$ modulator. IEEE Symposium on VLSI Circuits, Digest of Technical Papers, 2008: 78

[3] Chae Y, Lee I, Han G. A 0.7 V 36 μW 85 dB-DR audio $\Delta\Sigma$ modulator using class-C inverter. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 2008: 490

[4] Rabii S, Wooley B. A 1.8-V digital-audio sigma–delta modulator in 0.8 μm CMOS. IEEE J Solid-State Circuits, 1997, 32(6): 783

[5] Coban A L, Allen P E. A 1.5 V 1.0 mW audio $\Delta\Sigma$ modulator with 98 dB dynamic range. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 1999: 228

[6] Gaggle R, Inversi M, Wiesbauer A. A power optimized 14-bit SC $\Delta\Sigma$ modulator for ADSL CO applications. International Solid-State Circuits Conference, Digest of Technical Papers, 2004: 82

[7] Silva J, Moon U, Steensgaard J, et al. Wideband low-distortion delta–sigma ADC topology. Electron Lett, 2001, 37: 737

[8] Liu L, Chen L, Li D, et al. A 1.1 mW 87 dB dynamic range audio $\Delta\Sigma$ modulator in 0.18 μm CMOS. The First Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics, 2009: 17

[9] Geerts Y, Steyaert M. Design of multi-bit delta–sigma A/D converters. Boston/Dordrecht/London: Kluwer Academic Publishers, 2002: 143

[10] Yin G, Eynde F, Sansen W. A high-speed CMOS comparator with 8-b resolution. IEEE J Solid-State Circuits, 1992, 27(2): 208

[11] Baird R T, Fiez T S. Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging. IEEE Trans Circuits Syst, Part II, 1995, 42(12): 753