A new SOI high voltage device based on E-SIMOX substrate*

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Abstract: A new NI (n^+ charge islands) high voltage device structure based on E-SIMOX (epitaxy-the separation by implantation of oxygen) substrate is proposed. It is characterized by equidistant high concentration n^+-regions on the top interface of the dielectric buried layer. Inversion holes caused by the vertical electric field (E_V) are located in the spacing of two neighboring n^+-regions on the interface by the force from lateral electric field (E_L) and the compositive operation of Coulomb's forces with the ionized donors in the undepleted n^+-regions. This effectively enhances the electric field of dielectric buried layer (E_I) and increases breakdown voltage (V_B). An analytical model of the vertical interface electric field for the NI SOI is presented, and the analytical results are in good agreement with the 2D simulative results. E_I = 568 V/μm and V_B = 230 V of NI SOI are obtained by 2D simulation on a 0.375-μm-thick dielectric layer and 2-μm-thick top silicon layer. The device can be manufactured by using the standard CMOS process with addition of a mask for implanting arsenic to form NI. 2-μm silicon layer can be achieved by using epitaxy SIMOX technology (E-SIMOX).

Key words: E-SIMOX; charge islands; breakdown voltage; interface charges; ENDIF
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1. Introduction

Some work has been carried out to solve the problem of low vertical breakdown voltage (V_B) of high voltage (HV) devices fabricated on SOI (silicon on insulator) substrate[1−4]. ENDIF (enhanced dielectric layer field) is summarized as a general rule to increase V_B by enhancing the electric field of the dielectric buried layer (E_I), and several new structures have been proposed[5−10], in which, implanting interface charges is effective and attractive. SOI devices can be fabricated on SIMOX substrate. The standard SIMOX contains a thin SOI layer of 1800 Å and a buried oxide (BOX) of 3800 Å[11]. V_B of HV LDMOS using SIMOX process is less than 50 V[12−15]. The thin top silicon layer can be grown epitaxially to achieve proper thickness (E-SIMOX). As far as we know, there are few work reported in the field of realization of E-SIMOX SOI high voltage.

In this paper, a new structure of the high voltage device with the n+ charge islands based on E-SIMOX is presented. Introduced interface charges can enhance E_I, resulting in a much higher V_B. This is a recently proposed and easy-realized high voltage SOI device. Compared with conventional technology of CMOS, NI SOI LDMOS only needs an additional mask and process.

2. Structure and mechanism

Device structure and mechanisms of NI SOI LDMOS are illustrated in Fig. 1. A NI layer is inserted on the top interface of the buried oxide layer. L_d, t_S and N_d are the length, thickness and doping concentration of the drift region. t_I, t_{sub} and t_C represent the thicknesses of dielectric buried layer, substrate layer, and n^+-regions, respectively. L_E and L_H are the lengths of n^+-regions and spacing of two neighboring n^+-regions. When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, the inversion holes are formed in the spacing of equidistant n^+-regions by the vertical electric field (E_V) and located on the interface by the compositive operation of Coulomb's forces with the ionized donors in the undepleted n^+-regions and the force from lateral electric field (E_L), as illustrated in Fig. 1(b).

When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, 2-D potential $\phi(x, y)$ in the drift region can be written as $\phi(x, y) = \omega(x, y) + \varphi(x, y)$, where $\omega(x, y)$ and $\varphi(x, y)$ are the contributions of V_d and are respectively depleted impurities in drift region in which, $\varphi(x, y)$ satisfies 2-D Poisson equation:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_S},$$
$$0 \leqslant x \leqslant L_S + L_d, 0 \leqslant y \leqslant t_S, \quad (1)$$

where L_S is the lengths of source (p-body) and ε_S is the permittivity of silicon.

The vertical electric field under the drain (along MN) is derived as

$$E_y(L_S + L_d, y) = [\varepsilon_I\varphi(L_S + L_d, 0) - q\sigma_i(L_S + L_d)t_I - \varepsilon_I\varphi(L_S + L_d, t_S + t_I)]\, y/\varepsilon_I t^2. \quad (2)$$

With Eq. (2) and Gauss-theory on the interface, the electric fields in silicon and dielectric buried layer (at P point) E_S and E_I are obtained as

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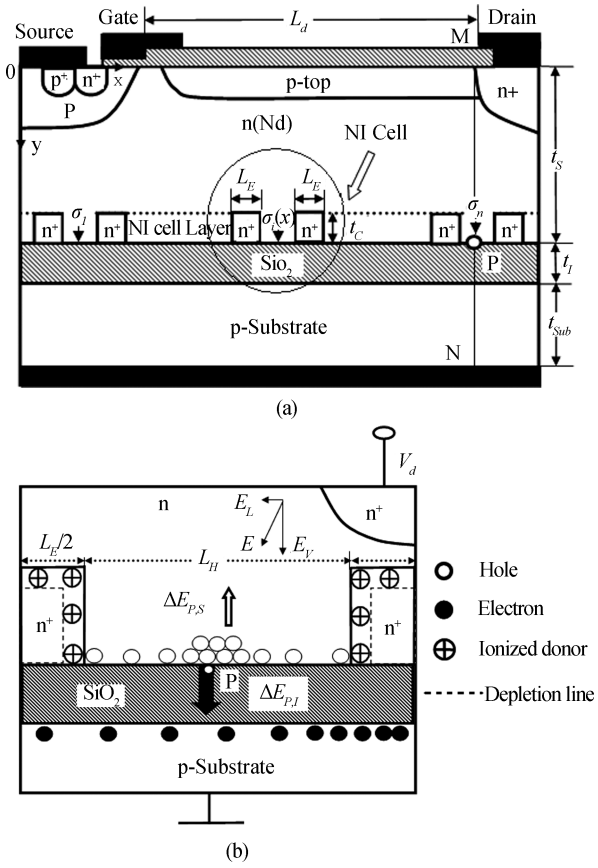


Fig. 1. Device structure and mechanism of NI SOI LDMOS. (a) Device structure. (b) A NI cell and work mechanism. E_{L} and E_{V} are the lateral and vertical electric fields, respectively.

$$E_{\mathrm{S}} = \frac{V_{\mathrm{d}} - \varphi(L_{\mathrm{S}} + L_{\mathrm{d}}, t_{\mathrm{S}} + t_{\mathrm{I}})}{t^2} t_{\mathrm{S}} - \frac{t_{\mathrm{I}} t_{\mathrm{S}} q \sigma_{\max}}{\varepsilon_{\mathrm{I}} t^2}, \qquad (3)$$

$$E_{\mathrm{I}} = \frac{\varepsilon_{\mathrm{S}} t_{\mathrm{S}}}{\varepsilon_{\mathrm{I}} t^2} [V_{\mathrm{d}} - \varphi(L_{\mathrm{S}} + L_{\mathrm{d}}, t_{\mathrm{S}} + t_{\mathrm{I}})] + \frac{t_{\mathrm{S}}^2 q \sigma_{\max}}{2\varepsilon_{\mathrm{I}} t^2}, \qquad (4)$$

where $\sigma_{\max}$ is the maximal interface charge density when $V_{\mathrm{d}} = V_{\mathrm{B}}$. From Eqs. (3) and (4), interface charge $\sigma_{\max}$ in the proposed NI SOI can enhance E_{I} in comparison with the conventional SOI ($\sigma_{\max} = 0$), while shielding the silicon layer electric field E_{S} to prevent the layer from breaking down prematurely (shown as $\Delta E_{\mathrm{P,I}}$ and $\Delta E_{\mathrm{P,S}}$ in Fig. 1(b), respectively). These all will contribute to a high V_{B}. Moreover, with $\sigma_{\max} = 0$, Equations (3) and (4) can be used for the conventional SOI.

3. Results and discussion

Figure 2 shows the charge distribution for the NI SOI LDMOS at breakdown. Figure 2(a) is the hole and electron concentrations on the both top and bottom interfaces of the buried dielectric layer. Plentiful holes are located on the top interface whose concentration increases from the source to the drain with potential. Moreover, there are electrons of $10^{18}\mathrm{cm}^{-3}$-level existing on the bottom interface. Figure 2(b) gives three-dimensional hole distribution in a NI cell, in which the highest hole concentration is in P point under drain because of the

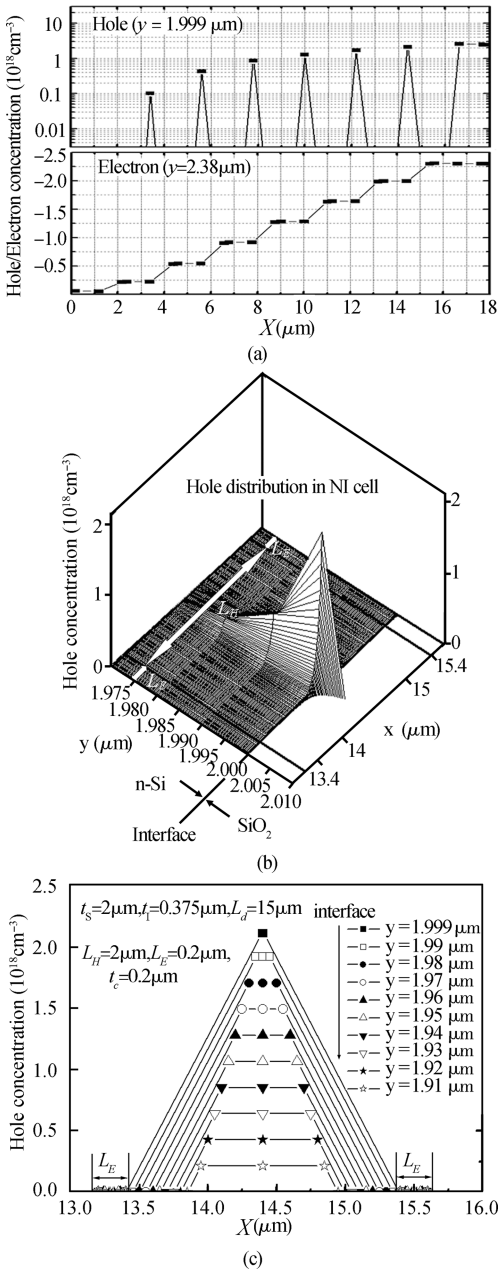


Fig. 2. Charge distribution for the NI SOI LDMOS at breakdown ($t_{\mathrm{S}} = 2\ \mu\mathrm{m}$, $t_{\mathrm{I}} = 0.375\ \mu\mathrm{m}$, $L_{\mathrm{d}} = 15\ \mu\mathrm{m}$, $t_{\mathrm{C}} = L_{\mathrm{E}} = 0.2\ \mu\mathrm{m}$, $L_{\mathrm{H}} = 2\ \mu\mathrm{m}$). (a) Hole/electron concentrations on the both top ($y = 1.999\ \mu\mathrm{m}$) and bottom ($y = 2.38\ \mu\mathrm{m}$) interfaces of the buried dielectric layer. (b) Three-dimensional hole distribution in a NI cell. (c) Hole distribution in a NI cell with different vertical distances.

maximal Coulomb force at the point. From Fig. 2(c), inversion layer is about 90 nm. Based on Eq. (4), the interface inversion layer of holes should effectively enhance E_{I} and improve V_{B}.

Figures 3(a) and 3(b) demonstrate the comparison of the equipotential contour distribution at breakdown for the proposed NI SOI and conventional SOI LDMOS. It is clear that the equipotential contour distribution of NI SOI is more uniform than that of conventional SOI and interface holes of NI SOI effectively modulate surface electric field, which means that a more uniform surface electric field is achieved for the proposed NI SOI than that of conventional as shown in Fig. 3(c).

Figure 4 illustrates the vertical electric fields and potentials

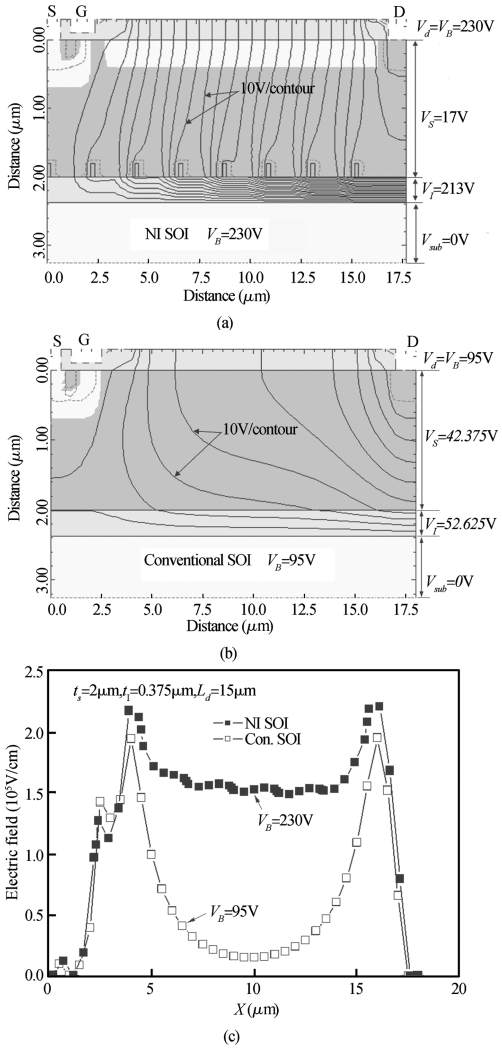


Fig. 3. Equipotential contour distribution and surface electric field profiles at breakdown. $V_{\rm S}$, $V_{\rm I}$ and $V_{\rm sub}$ which are the voltages shared by the top silicon layer, buried dielectric layer and the substrate layer, respectively. ($t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 0.375 μm, $L_{\rm d}$ = 15 μm). (a) Equipotential contour distribution of NI SOI ($t_{\rm C}$ = $L_{\rm E}$ = 0.2 μm, $L_{\rm H}$ = 2 μm, $N_{\rm d} = 1\times10^{15}$ cm^{-3}). (b) Equipotential contour distribution of the conventional SOI ($N_{\rm d} = 7.3\times10^{15}$ cm^{-3}). (c) Surface electric field profiles.

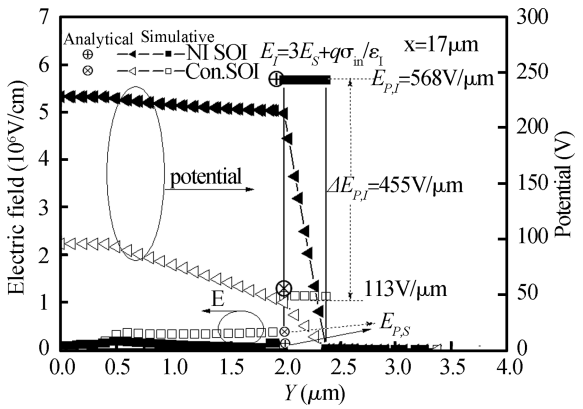
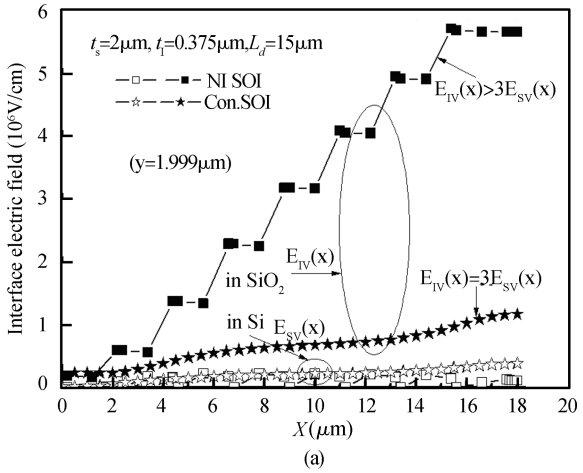


Fig. 4. Vertical electric field and potential distribution at breakdown under the drain ($t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 0.375 μm, $L_{\rm d}$ = 15 μm, $t_{\rm C}$ = $L_{\rm E}$ = 0.2 μm, $L_{\rm H}$ = 2 μm).



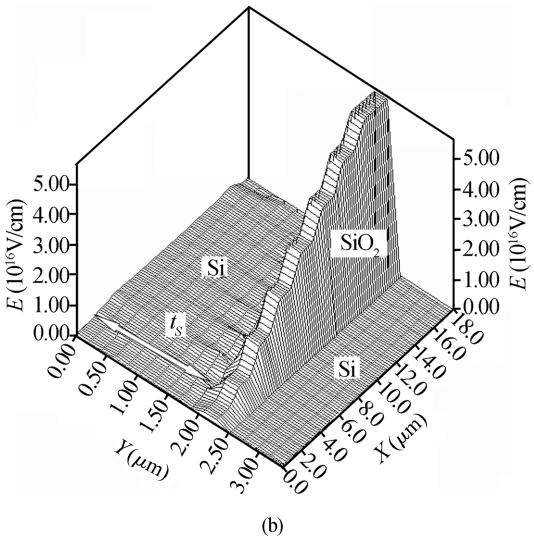


Fig. 5. Electric field distribution at breakdown ($t_{\rm S}$ = 2 μm, $t_{\rm I}$ = 0.375 μm, $L_{\rm d}$ = 15 μm, $t_{\rm C}$ = $L_{\rm E}$ = 0.2 μm, $L_{\rm H}$ = 2 μm). (a) Vertical electric fields in Si ($E_{\rm SV}$) and in SiO_2 ($E_{\rm IV}$) on the top interface. (b) Three dimensional distribution of electric fields.

distribution at breakdown for the NI SOI and the conventional SOI. It can be seen that $E_{\rm I}$ of NI SOI increases from 113 V/μm of the conventional SOI to 568 V/μm due to the enhancement effect of the inversion charges, which results in a higher $V_{\rm B}$ of 230 V for NI SOI compared to 95 V for the conventional SOI. Moreover, 92.6% above of the $V_{\rm B}$ for NI SOI is shared by the dielectric buried layer ($V_{\rm I} = t_{\rm I}E_{\rm I}$ = 213 V) from the potential distributions shown in Fig. 4, and $V_{\rm I}$ is dominant in the $V_{\rm B}$. The simulative results are in agreement with the analytical results of Eqs. (3) and (4), and it can be concluded that the interface charges accumulated by the proposed NI SOI can assuredly enhance $E_{\rm I}$ and increase $V_{\rm B}$.

Figure 5(a) shows vertical electric fields in Si ($E_{\rm SV}$) and SiO_2 ($E_{\rm IV}$) on the top interface along x-axis. For NI SOI, $\Delta E_{\rm I}(x)$ increases with the hole concentration of Fig. 2 from source to drain. Therefore, so $E_{\rm IV}$ is much larger than $3E_{\rm SV}$ under the drain in comparison with the conventional dependence of $E_{\rm IV} = 3E_{\rm SV}$. $E_{\rm SV}$ (x) for each point is almost invariable because of a series of $n^+n^-n^+$-structures (NI cell) with a sustainingly applied voltage of 30 V as shown in Fig. 3, and

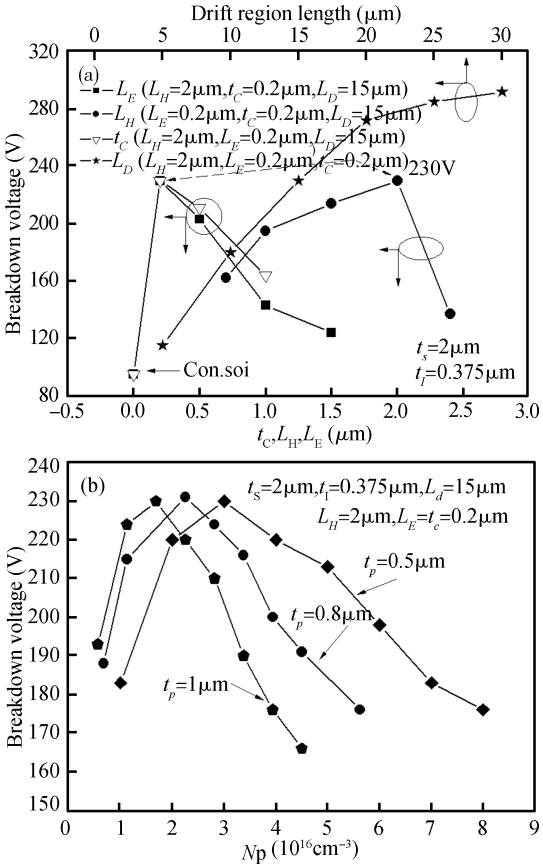


Fig. 6. Influences of structure parameters on breakdown voltage, t_S = 2 μm, t_I = 0.375 μm for all. (a) t_C, L_E, L_H and L_d. (b) P-top layer thickness t_p and concentration N_p (t_S = 2 μm, t_I= 0.375 μm, L_d = 15 μm, t_C = L_E = 0.2 μm, L_H = 2 μm).

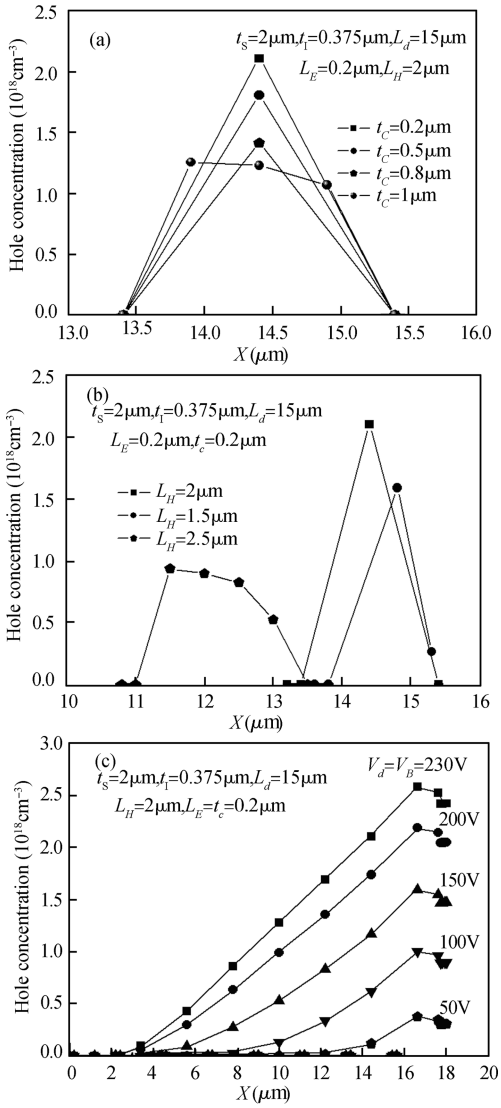


Fig. 7. Hole distribution in a NI cell with different t_C, L_H and V_d (t_S = 2 μm, t_I = 0.375 μm, L_d = 15 μm). (a) Hole concentrations versus t_C. (b) Hole concentrations versus L_H. (c) Hole concentrations versus V_d (t_S = 2 μm, t_I = 0.375 μm, L_d = 15 μm, t_C = L_E = 0.2 μm, L_H = 2 μm).

E_{SV} (x) is less than 30 V/μm due to the shielding effect of holes, whereas those of conventional SOI increase from source to drain with the potential and reach to 30 V/μm under the drain where breakdown occurs (x = 17.4 μm). Breakdown point for NI SOI is at x = 6.53 μm because of high lateral electric field. Enhancement of holes on E_I can be clearly seen from three dimensional distribution of electric field shown in Fig. 5(b).

Figure 6(a) gives the influences of t_C, L_E, L_H and L_d on V_B. It can be seen that V_B is improved with the increasing of L_d, which breaks through the V_B limitation of conventional SOI. V_B > 200 V can be obtained with L_H from 1 to 2 μm. t_C and L_E obviously effect V_B and there is a maximum V_B of 230 V when L_H = 2 μm and t_C = L_E = 0.2 μm with L_d = 15 μm. Figure 6(b) shows the dependence of V_B on thickness t_p and concentration N_p of the p-top layer. V_B is almost invariable with t_p from 0.5, 0.8 to 1 μm, and for each t_p, the maximal V_B appears when t_pN_p is about 1.5 × 10^{12} cm^{-2} which satisfies the RESURF (reduced surface field) condition, and after that, V_B sharply decreases because of premature breakdown at n^+–p junction of drain side.

The dependences of hole concentration on the structure parameters of the NI Cell are illustrated in Figs. 7(a) and 7(b). It can be found that compared to L_E, L_H and t_C generate stronger effect on the hole concentration, the reason of which is that the hole concentration decreases when L_H and t_C both are over the optical values, or that holes in the inversion layer will be extracted by lateral electric field (E_L) while L_H and t_C are small. Figure 7(c) gives the dependences of hole concentration on applied voltages. With adding V_d from 50 V to V_B (230 V), hole concentration increases, and for each V_d, hole concentration is enhancive from source to drain with potential. This shows that interface holes have the self-adaptive characteristic and ability which are automatically varied with the applied voltage and effective enhancement on E_I to make the device endurable to the applied voltages.

Figure 8 shows the influences of N_{n+} (concentration of n^+-regions) on V_B, E_I and the maximal hole concentration $N_{h,m}$. It can be seen that when N_{n+} is larger than 2.5 × 10^{18} cm^{-3}, V_B is invariable as well as E_I and $N_{h,m}$. When N_{n+} is less than 2.5 × 10^{18} cm^{-3}, V_B decreases with the decreasing N_{n+}. The reason can be explained as the following: when N_{n+} is larger than 2.5 × 10^{18} cm^{-3}, the n^+-regions under the drain are undepleted and the ionized donors are invariable which is independent on N_{n+}.

Table 1. Summary of process flow.

Process flow	Parameter	SOI wafer	Unit
Arsenic implantation	n^+ islands dose	2×10^{13}	cm^{-3}
	n^+ islands energy	180	keV
	n^+ islands thickness	0.2	μm
High-temperature annealing	Annealing temperature	1000	°C
	Annealing time	2.37	h
Epitaxial growth	n-type Si layer doping	1×10^{15}	cm^{-2}
	n-type Si layer thickness	1.8	μm
	Epitaxial time	50	min
	Epitaxial temperature	1150	°C
P-body implantation	Boron-dose	1×10^{13}	cm^{-3}
	Boron-energy	150	keV
P-top implantation	Boron-dose	1.05×10^{12}	cm^{-3}
	Boron-energy	50	keV
P-body & P-top drive in	Time	1.3	h
	Temperature	1138	°C

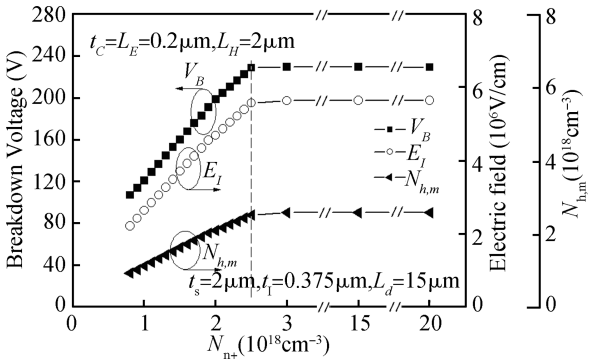


Fig. 8. Influences of interface n+-region concentration N_{n+} on breakdown voltage, E_I and the maximal hole concentration $N_{h,m}$

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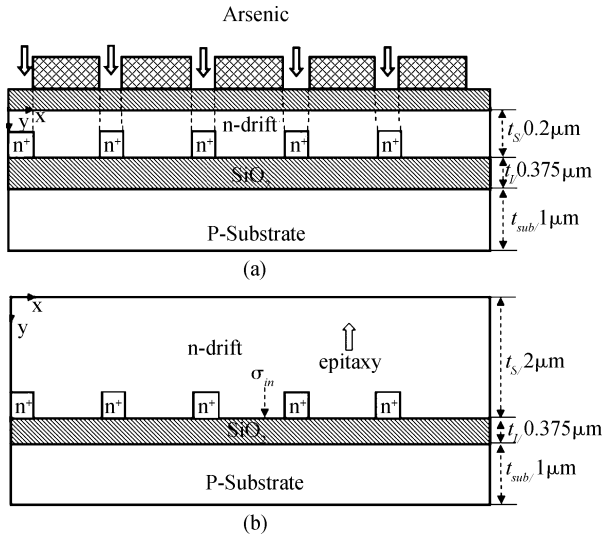

Fig. 9. Schematic principle of E-SIMOX NI SOI technology. (a) Implanting As to form NI. (b) Silicon layer epitaxy to 2 μm.

The major steps of the process flow are depicted in Table 1, and the associated device cross sections are shown in Fig. 9 for the NI SOI LDMOS, which is fabricated on a SIMOX substrate with n+-regions formed by implanting 2×10^{13} cm^{-3} arsenic at 180 keV and subsequently annealing in the same conditions (shown in Table 1). The thickness of the n^+-regions after masked implantation processing is estimated as 200 nm. Then the 2-μm silicon layer can be achieved by using epitaxy technology at 1150 °C with 1×10^{15} cm^{-2} for 0.8 h. P-body and P-top uses boron ions beam implantation process, followed by high temperature driving in to create the P-body and P-top regions (shown in Table 1, too). Therefore, only an additional process of arsenic implantation before bonding is needed to form NI SOI. Other fabrication processes are fully compatible with conventional CMOS/SOI technology.

4. Conclusion

In this research, the NI SOI LDMOS based on E-SIMOX high-voltage device structure is introduced and simulated. The processes are compatible with conventional CMOS/SOI technology. The proposed NI-structure increases significantly the V_B because of the modulation effect of interface charges on the electric fields in the spacing of equidistant n+-regions. NI-structure is a brand-new concept for SOI high voltage device used to accumulate and utilize the interface charges. Therefore, NI SOI has the potential for applications in high voltage and power integrated circuits because of their favorable performances and easy fabrication processes.

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