Mixed-integrator-based bi-quad cell for designing a continuous time filter

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Abstract: A new mixed-integrator-based bi-quad cell is proposed. An alternative synthesis mechanism of complex poles is proposed compared with source-follower-based bi-quad cells which is designed applying the positive feedback technique. Using the negative feedback technique to combine different integrators, the proposed bi-quad cell synthesizes complex poles for designing a continuous time filter. It exhibits various advantages including compact topology, high gain, no parasitic pole, no CMFB circuit, and high capability. The fourth-order Butterworth lowpass filter using the proposed cells has been fabricated in 0.18 μm CMOS technology. The active area occupied by the filter with test buffer is only 200×170 μm^2. The proposed filter consumes a low power of 201 μW and achieves a 68.5 dB dynamic range.

Key words: bi-quad cell; negative feedback technique; continuous time filter; CMOS
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1. Introduction

The increasing demand of portable wireless communication systems forces the development of better system-level and circuit-level solutions. For example, the small area and low power consumption of the entire wireless system and, especially of each singular block in the circuit-level become important, since the amount of saved area and power would be available for reduction of cost and longer battery life[1]. Integrated continuous time baseband filters are essential building blocks in the receiver path. Traditional implementations of these filters are based on active elements such as active-RC, MOSFET-C, and G_m–C techniques[2]. However, the trend towards small area and low power will be confronted with new challenges in the realization of these filter techniques. So some novel filter structures have been proposed exhibiting excellent advantages[1, 3–5].

CMOS novel filter architectures have attracted much attention in RF/IF circuit design owing to their compact topology and ultra-low power. In Ref. [1] the key idea of source-follower-based (SFB) bi-quad cells is the positive feedback in two medium cascode MOS devices, which allow synthesis of two complex poles. The positive feedback technique is also applied to the continuous time filter based on current driving[3]. The former processes the signal in the voltage mode, and the latter processes the signal in the current mode. In Ref. [4] a source single-loop continuous time filter architecture is made by alternately cascading first-order positive and negative buildings. In the negative block, the drain and gate of two MOS devices with cross coupling connection create the negative resistor used to synthesis complex poles. In addition, all the above bi-quad cells consist of the same first-order integrators.

In this paper, a new bi-quad cell with negative feedback technique for designing a low power continuous time filter is proposed. The proposed bi-quad cell combines a first-order SFB integrator with a first-order G_m–C integrator by applying the negative feedback technique (hence the name mixed-integrator-based bi-quad cell (MIB-BC)).

2. Integrators

Figure 1 shows the basic idea of this work, which is based on the two different types of integrators. First, a common drain MOS device (Mp1) and load capacitor (C_L) consist of a first-order SFB integrator, as shown in Fig. 1(a), and this is a CMOS lossy integrator. The input and output nodes are the gate and source terminals of the MOS device (Mp1), respectively, and the transfer function of the integrator is given by

$$H(s) = G_{m1}/(G_{m1} + sC_L). \tag{1}$$

Second, Figure 1(b) shows that a common source MOS device (Mp1) and load capacitor (C_L) consist of a first-order G_m–C integrator, and this is a CMOS lossless integrator. The transfer characteristic of the integrator is given by

$$H(s) = G_{m1}/(sC_L), \tag{2}$$

where G_{m1} is the transconductance of Mp1, and C_L is the total grounded capacitances at the transistor Mp1's sources. These two integrators are essential blocks for implementing the MIB continuous time filter.

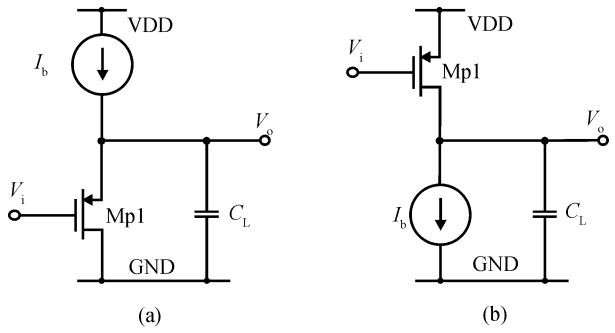

Fig. 1. Basic integrator.

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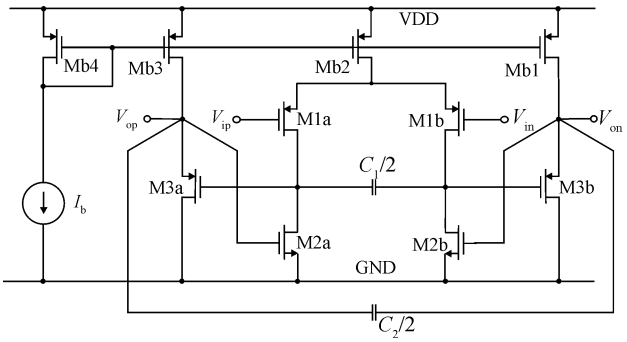

Fig. 2. Proposed lowpass bi-quad cell.

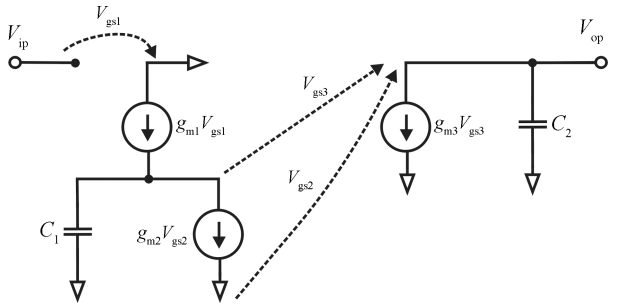

Fig. 3. Half small signal equivalent circuit.

3. Circuit analysis and design

3.1. Proposed bi-quad cell

To synthesize complex poles with different types of integrators, a pair of negative feedback transistors (M2a and M2b) is used to combine the source-follower-based integrator (M3a, M3b and C_2) with the G_m–C integrator (M1a, M1b and C_1) in MIB-BC, as shown schematically in Fig. 2. Assuming that the MIB-BC is perfectly symmetrical, the bi-quad cell transfer function can be simply derived using a half small-signal equivalent circuit (Fig. 3), given by

$$H(s) = \frac{\dfrac{g_{m-M1a}g_{m-M3a}}{C_1C_2}}{s^2 + s\dfrac{g_{m-M3a}}{C_2} + \dfrac{g_{m-M2a}g_{m-M3a}}{C_1C_2}}, \tag{3}$$

where g_m is the transconductance of the corresponding transistors, and C_1 and C_2 are the total grounded capacitances at the transistors M1a and M1b's sources and at the output nodes, respectively. The bi-quad cell parameters are concluded as follows:

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{g_{m-M2a}g_{m-M3a}}{C_1C_2}}, \tag{4}$$

$$Q = \sqrt{\frac{C_2}{C_1}\frac{g_{m-M2a}}{g_{m-M3a}}}, \tag{5}$$

$$K = \frac{g_{m-M1a}}{g_{m-M2a}}, \tag{6}$$

where K is the DC gain, f_0 is the pole frequency, and Q is the quality factor. The proposed bi-quad cell exhibits the following advantages:

(1) Compact structure: only ten transistors and two capacitors are used.

(2) Gain: from Eq. (6), the K of the MIB-BC can be larger than the unity gain.

(3) Accurate transfer function: at the first order, no parasitic pole is present, which avoids additional power to push non-dominant poles to high frequency.

(4) No CMFB circuit: the output common-mode voltage is fixed by the negative feedback mechanism.

(5) High drive capability: low output impedance makes the bi-quad cell driving the following stages.

3.2. Noise analysis

The proposed bi-quad cell noise contribution has been modeled as current noise power density, as shown in Eq. (7). The MOS thermal noise is a major contribution due to the large bandwidth (10 MHz) to be processed by the proposed bi-quad cell.

$$\frac{\langle i_n^2\rangle}{\Delta f} = \frac{2}{3} \times 4kT \times g_m. \tag{7}$$

The input-referred noise spectral density at low frequency is derived as follows:

$$\mathrm{IRN}^2 = \frac{16}{3}\frac{kT}{g_{m1-M1a}}\left(1 + \frac{g_{m2-M2a}}{g_{m1-M1a}} + \frac{g_{m2-M2a}}{g_{m3-M3a}}\right). \tag{8}$$

This gives an integrated input-referred noise $V_{in,\,noise}$:

$$V_{in,\,noise}^2 = \frac{16}{3}\frac{kT}{g_{m1-M1a}}\left(1 + \frac{g_{m2-M2a}}{g_{m1-M1a}} + \frac{g_{m2-M2a}}{g_{m3-M3a}}\right) \times \sqrt{\frac{g_{m-M2a}g_{m-M3a}}{C_1C_2}}. \tag{9}$$

If $g_{m1-M1a} = g_{m3-M3a} = 2g_{m2-M2a}$, Equation (8) is simply calculated as follows:

$$V_{in,\,noise}^2 = \frac{16\sqrt{2}}{3}\frac{kT}{\sqrt{C_1C_2}}. \tag{10}$$

An analog filter has a maximal signal level that can be set by a specified amount of distortion. Furthermore, minimum signal level processing by the analog filter is determined by a certain noise level. The ratio of these two levels can be defined as the dynamic range (DR) of the analog filter. If the maximal RMS signal level at the input of the analog filter is denoted by V_{RMS} and the RMS noise level at the same terminal is defined as $V_{in,\,noise}$, the dynamic range is given by

$$\mathrm{DR} = \frac{3\sqrt{2}}{32}\frac{\sqrt{C_1C_2}}{kT}V_{RMS}^2. \tag{11}$$

To obtain an optimal dynamic range, scaling internal signal levels (increasing V_{RMS}) and increasing the area of the capacitors are design freedom degrees for the analog filter.

3.3. Minimum supply voltage

Supposing that the drain-source dropping voltage PMOS transistor (Mb1 and Mb3) of the proposed bi-quad is at least V_{sat}, the minimum supply voltage $V_{dd,\,mim}$ is

$$\begin{aligned} V_{dd,\,min} &= V_{sat} + V_{swing} + V_{GS-M3a} + V_{sat} \\ &= 3V_{sat} + V_{th} + V_{swing}. \end{aligned} \tag{12}$$

For a 0.18 μm CMOS technology, assuming V_{sat} = 200 mV, V_{th} = 500 mV, V_{swing} = 400 mV, $V_{dd,\,mim}$ = 1.5 V is needed. The fold structure can reduce the supply voltage.

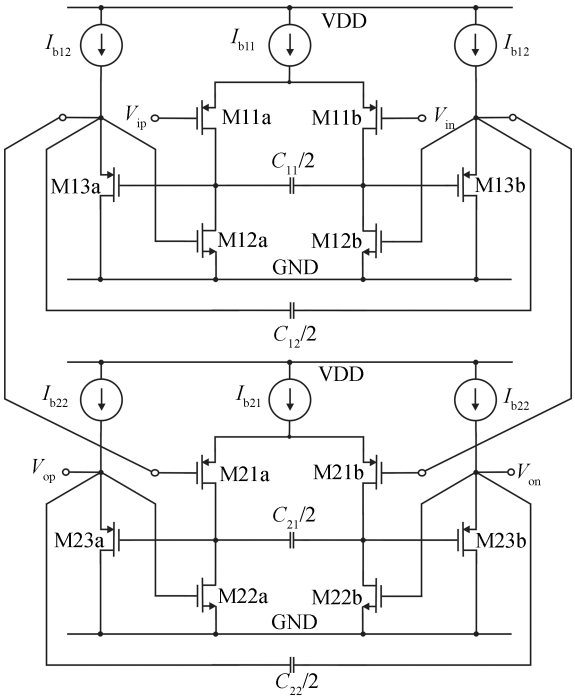

Fig. 4. Fourth-order Butterworth lowpass filter.

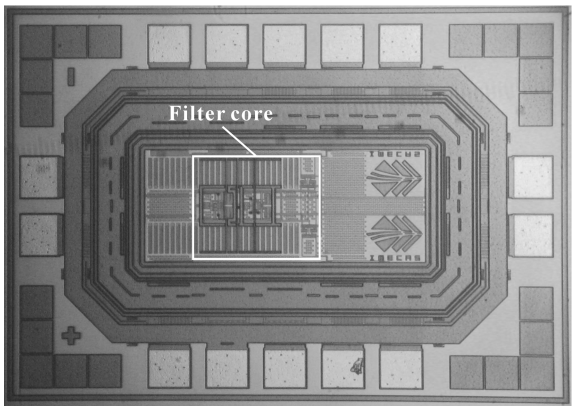

Fig. 5. Die photograph of the fourth-order Butterworth lowpass filter.

4. Experimental results

A cascade of two proposed cells is used to implement a fourth-order fully differential Butterworth lowpass filter, as shown in Fig. 4. This fourth-order Butterworth lowpass filter is designed and fabricated in SMIC 0.18 μm CMOS technology. The active area occupied by the MIB filter with test buffer is only 200 × 170 μm^2. The small chip area of the filter is determined by the MOS transistors and by the small area of the capacitors; the total capacitor value is 6 pF. Its die photograph is shown in Fig. 5.

Figure 6 shows the measured and simulated frequency response of the Butterworth lowpass filter, which exhibits a 10-MHz cut-off frequency with 7.5-dB gain. The passband ripple of the filter is less than 0.8 dB. The result of an in-band IM3 distortion test is −48 dB with two-tone at 3 MHz and 4 MHz of −26 dBm each at the inputs, as shown in Fig. 7, so the calculated in-band IIP3 of the filter is -4 dBm. The linearity has

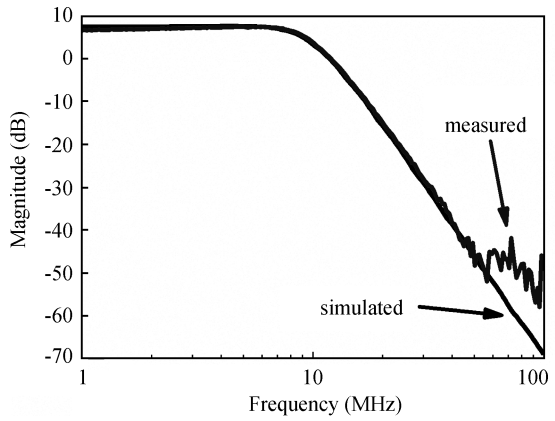

Fig. 6. Filter frequency response.

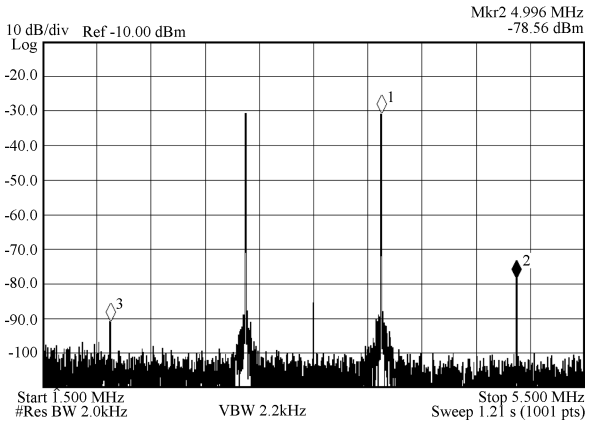

Fig. 7. In-band IM3.

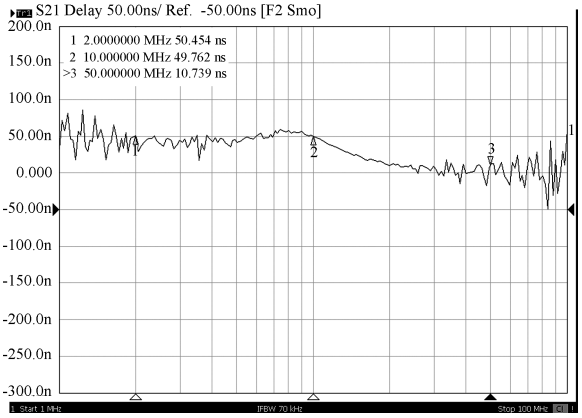

Fig. 8. Measured group delay.

been evaluated also in terms of HD3, which is −40 dB for a 140-mV$_{pp}$ input amplitude. The integrated input-referred spectral density noise is equal to 37.1 μV$_{rms}$. This gives a 68.5-dB dynamic range (DR), for −40-dB HD3, while the power consumption is 201 μW at 1.5-V supply. The deviation of the in-band group delay is within the range of 50 ns, as shown in Fig. 8. Table 1 summarizes the filter characteristics.

5. Conclusion

Using the negative feedback technique to combine different integrators, a novel mixed-integrator-based bi-quad cell is pre-

Table 1. Summary of the filter's measured results.

Parameter	Value
Technology	CMOS 0.18 μm
Power supply	1.5 V
Power consumption	201 μW
DC-gain	7.5 dB
-3 dB cut-off frequency	10 MHz
$V_{\text{in, noise}}$	37.1 μV_{rms}
DR (HD3 = -40 dB)	68.5 dB
In-band IM3 ($f_1 = 3$ MHz, $f_2 = 4$ MHz)	−48 dB
In-band IIP3 ($f_1 = 3$ MHz, $f_2 = 4$ MHz)	−4 dBm
HD3 (140 mV_{pp} @ 3 MHz)	−40 dB
In-band group delay variation	50 ns

sented. The proposed bi-quad cell synthesizes complex poles for designing a continuous time filter. The fourth-order Butterworth lowpass filter using a cascade of two proposed cells has been designed in 0.18 μm CMOS technology. The expected transfer function characteristics of this filter can be measured. The proposed filter consumes a low power of 201 μW and achieves a 68.5 dB dynamic range, for –40 dB HD3.

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