A high-speed and high-resolution CMOS comparator with three-stage preamplifier*

Jiang Li(江利)[1,2,†], Xu Weisheng(许维胜)[1,2], and Yu Youling(余有灵)[1,2]

(1 School of Electronics and Information, Tongji University, Shanghai 201804, China)
(2 Research Institute of Semiconductor, Tongji University, Shanghai 201804, China)

Abstract: The accuracy of A/D and D/A converters depend largely upon their inner comparators. To guarantee 12-bit high resolution for an A/D converter, a precise CMOS comparator consisting of a three-stage differential preamplifier together with a positive feedback latch is proposed. Circuit structure, gain, the principle of input offset voltage storage and latching time constant for the comparator will be analyzed and optimized in this article. With 0.5 μm HYNIX mixed signal technology, the simulation result shows that the circuit has a precision of 400 μV at 20 MHz. The test result shows that the circuit has a precision of 600 μV at 16 MHz, and dissipates only 78 μW of power dissipation at 5 V. The size of the chip is 210 $\times$ 180 μm^2. The comparator has been successfully used in a 10 MSPS 12-bit A/D converter. The circuit can be also used in a less than 13-bit A/D converter.

Key words: high speed comparator; CMOS comparator; input offset storage; latch
DOI: 10.1088/1674-4926/31/4/045006 **EEACC:** 1265H; 2570D

1. Introduction

In analog-to-digital converters, the comparator plays a crucial role in the overall performance. An accurate and fast comparator is a key element in any high-resolution and high-speed data converter. The performance of the comparator, especially speed, power dissipation and offset voltage may have an important effect on the whole performance of ADC[1]. Moreover, the specifications must be met in the presence of non-idealities such as those arising from device mismatch in VLSI technology. A commonly used topology for realizing high-speed and high-resolution comparators consists of a preamplifier employing offset voltage storage, followed by a regenerative latch. The preamplifier in the comparator typically consists of an identical single-pole amplifier with sufficient gain, high-speed and low power dissipation[2].

The design of the preamplifier is described and simple equations are introduced to calculate gain, residual input offset voltage and converting time in the article. In this design, preamplifier gain is sensitive to residual input offset voltage and converting time. Increasing the bandwidth of the preamplifier and reducing the time constant can speed up the comparator, but they can also reduce the equivalent input signal strength because of the increased noise bandwidth and the residual error from incomplete settling[3]. As a result, more gain is required for the preamplifier. In the design with constrained power dissipation, it is likely to apply to narrow bandwidth. Thus, there exists a complex trade-off between various parameters in the preamplifier design. In this paper a three-stage preamplifier with input offset voltage storage serves as a vehicle for exploring these trade-offs[4].

This paper analyzes the systemic structure of the comparator, describes the circuit structure of the preamplifier, optimizes the gain and offset voltage, and designs the latch comparator.

2. Principle of the preamplifier-latch

The principle of the preamplifier-latch is that the preamplifier amplifies the input signal and the amplified signal is inputted into the latch comparator. For high accuracy application, an effective way of reducing the DC offset voltage due to the feedthrough charge is to use a fully differential scheme for the comparator. In such circuits, not only are clock-feedthrough effects reduced, but power supply noise and $1/f$ noise also tend to be cancelled. A single-stage high-gain and offset-cancelling comparator will have a long response time. Therefore, high-resolution and high-speed comparators use a multistage design. Each stage of the multistage design uses one of the low-gain amplifier stages. Figure 1 depicts a three-stage fully differential comparator with input offset storage (IOS). Each stage is coupled to the next one with the capacitor. By closing the feedback loop around each stage independently, the possible instability problem of a three-stage amplifier with one feedback loop is eliminated. The circuit operates as follows. During the offset storage mode, the feedback switches are closed, a unity-gain feedback loop is established around each gain stage, and the offset voltage of the comparators is stored on the input capacitors. In the tracking mode, the feedback around the comparators is opened and the input differential voltage is sensed and amplified by A^3, where A is the voltage gain of each amplifier stage. The output of the comparator is stored by a latch that produces a logic level at its output.

If $V_{\rm offA}$ and $V_{\rm offL}$ represent the input offset voltage of the first comparator and the latch respectively, the residual input referred offset voltage is given by

$$V_{\rm offset} \approx \frac{V_{\rm offA}}{1+A} + \frac{Q_0 - Q_1}{C_1} + \frac{V_{\rm offL}}{A^3}. \quad (1)$$

From Eq. (1), if the charge injected by switch S_0 is Q_0

* Project supported by the National High Technology Research and Development Program of China (No. 2006AA05Z211).
† Corresponding author. Email: river0556@163.com
Received 7 October 2009, revised manuscript received 25 November 2009

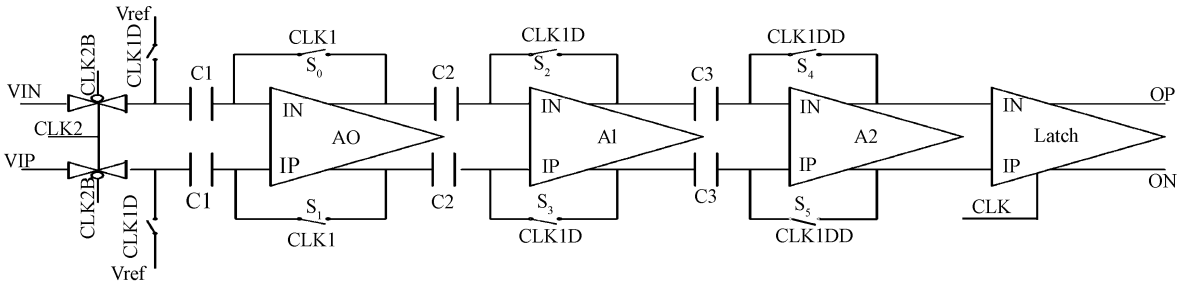

Fig. 1. System schematic of the comparator.

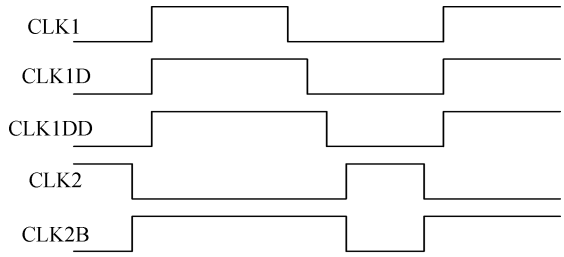

Fig. 2. Timing chart of the comparator.

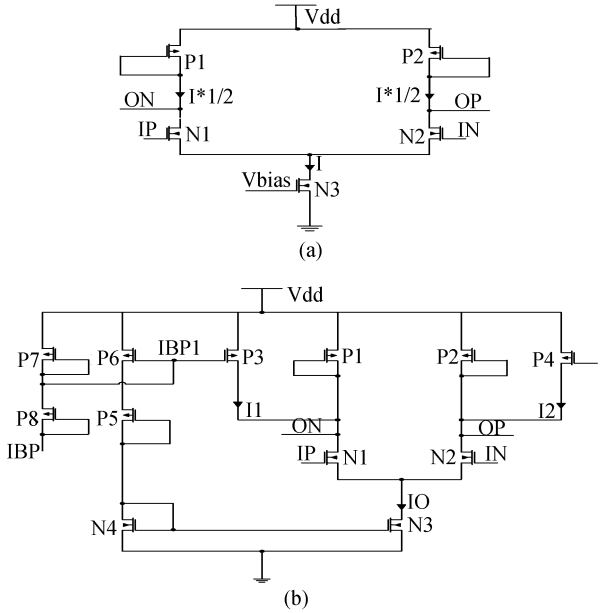

Fig. 3. (a) Gain block with diode-connected load devices. (b) Gain-enhanced differential pair.

and the charge injected by switch S_1 is Q_1, the common-mode voltage will be slightly affected by an amount equal to $(Q_0 + Q_1)/2C_1$. The different input voltage $\Delta Q/C_1 = (Q_0 - Q_1)/C_1$ will be zero if Q_0 is equal to Q_1. In practice, the charge injected by the two switches will never match. The residual offset voltage due to the mismatch in the fully differential case will be less than that in the single-ended case. For this reason most advanced integrated comparators use the fully differential design technique[5].

From Eq. (1), there are three methods to reduce the residual offset voltage: (1) improve the gain of the preamplifier; (2) enlarge the input capacitor; (3) reduce the offset voltage of the preamplifier and latch. When the gain of the preamplifier is improved, the bandwidth is depressed and the speed of the comparator cannot be improved. If the input capacitor is augmented, the charge and discharge time is longer and it also affects the speed of the comparator. For the third method, increasing the size of the input transistors can reduce the offset voltage of the preamplifier and latch, but the parasitical capacitor also is enlarged so that the speed cannot be improved. Therefore, there is a trade-off between the gain of the preamplifier, the size of input transistor and input capacitor and the speed of the comparator.

The mismatch between the channel charges injected from the feedback switches introduces an unmoved offset voltage at the input of each gain stage. The total DC offset voltage is dominated by the offset voltage of the first stage. It is possible to reduce this type of error by implementing the sequential clocking scheme shown in Fig. 2. The gain stages are brought sequentially with the offset cancellation mode, A0 first and A2 last. From Fig. 2, the rising edge has no delay for clock CLK1, CLK1D, CLK1DD. That is to say, switches S_0, S_1, S_2, S_3, S_4, and S_5 are closed synchronously. The falling edge has a delay between the CLK1 and CLK1D and also has a delay between CLK1D and CLK1DD. Switches S_0 and S_1 are opened firstly and the charge injection for switches S_2, S_3, S_4, and S_5 has not affected the input stage. The offset voltage which is produced by charge injection from the mismatch of switches S_0 and S_1 on capacitor C_1 is amplified by the first stage and stored on capacitors C_2 and C_3 before the other feedback switches are opened. In order to cancel its charge injection error, this can be repeated for the opening of switches S_2 and S_3. Therefore, the offset voltage due to charge injection error is in storage on capacitors by this method. To ensure proper operation, the delay between the clock edges shown in Fig. 2 should be long enough to allow the input capacitors of the next stage to fully absorb the offset voltage of the previous stage.

3. Multistage preamplifier

Figure 3(b) shows a differential amplifier that can be used as the input stage of the comparator. Diode-connected transistors P1 and P2 are aimed to attain the output common-mode voltage. For Fig. 3(a), the different gain of the source coupled pair is given by

$$A_{\mathrm{d}} = g_{\mathrm{mn1}}/g_{\mathrm{mp1}} = \sqrt{\frac{\mu_{\mathrm{n}}(W/L)_{\mathrm{N1}}}{\mu_{\mathrm{p}}(W/L)_{\mathrm{P1}}}}. \tag{2}$$

For Eq. (2), the expressions of μ_{n} and μ_{p} are the mobility of the NMOS and PMOS devices, respectively. The expression of

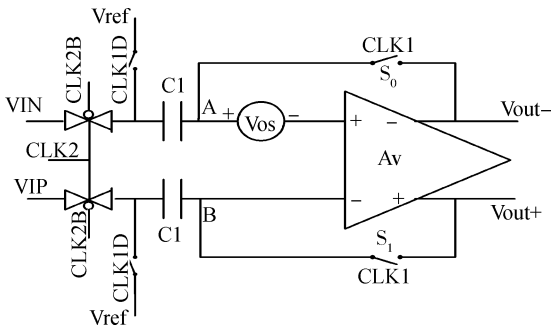

Fig. 4. Schematic of offset voltage cancellation.

g_{mn1} is the transconductance of MOSFET N1 and the expression of g_{mp1} is the transconductance of MOSFET P1. Equation (2) shows the dependence of the differential gain on the square root of the device dimensions. Higher-mobility NMOS transistors are used as input devices to achieve higher gain. Diode-connected loads consume the voltage margin; therefore there is a trade-off between output voltage swing, voltage gain and input voltage range. From Eq. (2), for a given bias current and input MOSFET size, the gain A_d shows an approximately inverse ratio to $(W/L)_{P1}$. For attaining larger circuit gain, the size of $(W/L)_{P1}$ can be reduced, which is equal to increasing the voltage $\left|V_{gsp} - V_{thp}\right|$; therefore common mode voltage for node ON and OP is dropped. In order to alleviate this problem, the bias current of the input MOSFET is partly supplied by currents I_1 and $I_2 (I_1 = I_2 = I)$ which come from the p-channel current sources P3 and P4, as shown in Fig. 3(b). The g_m of diode-connected loads is decreased by depressing the current through them, but not by reducing the size of $(W/L)_{P1}$. The gain of the modified circuit is now given by

$$A_d = \sqrt{\frac{\mu_n (W/L)_{N1} (I_0/2)}{\mu_p (W/L)_{P1} (I_0/2 - I)}} = \sqrt{\frac{\mu_n (W/L)_{N1}}{\mu_p (W/L)_{P1} (1 - 2I/I_0)}}. \quad (3)$$

If $I = 0.9I_0/2$, the gain of the preamplifier is increased by a factor of $\sqrt{10}$.

Because the manufacturing process has uncertainty, mismatch always exists. Mismatch affects the performance of the circuit and brings out the offset voltage. The offset voltage of difference input MOFET is expressed as follows[6]:

$$V_{os} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R}{R} + \frac{\Delta W/L}{W/L}\right] - \Delta V_{TH}. \quad (4)$$

In Eq. (4), R is the load resistor, and ΔR is the error value for the mismatch. The expressed $\Delta(W/L)$ is the error value of W/L. For Eq. (4), ΔV_{TH} has an important impact on V_{os}. Increasing the size of the MOSFET can decrease the offset voltage. If the size of the MOSFET is too large, it will degrade the speed of the amplifier. Therefore, the structure of offset voltage storage is adopted and this does not affect the speed of the amplifier. Figure 4 shows the simplified structure of offset voltage storage.

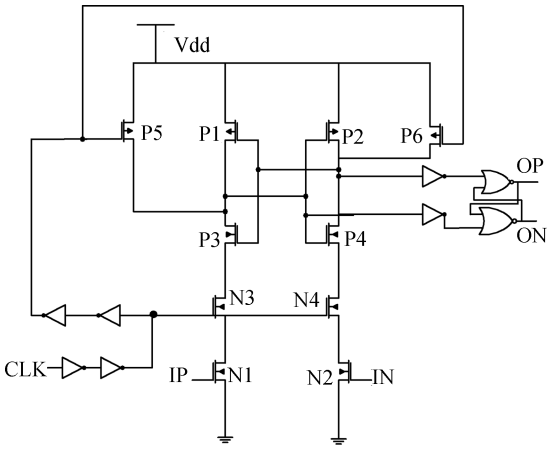

Fig. 5. Schematic of the latch.

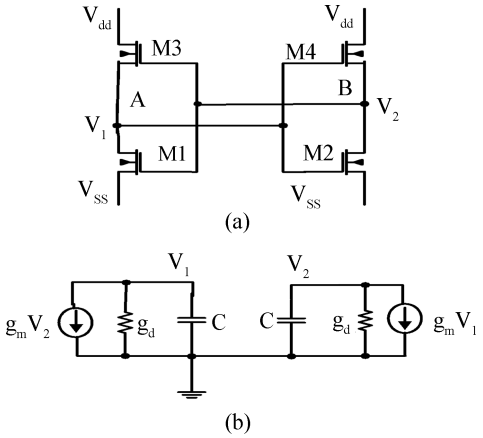

Fig. 6. (a) Simplified schematic of the latch. (b) The small signal model for the simplified schematic of the latch.

When switches S_0 and S_1 are closed, the amplifier shows unit gain negative feedback.

$$V_{out} = V_{out+} - V_{out-} = V_{BA}, \quad (5)$$

$$(V_{out} - V_{os})(-A_V) = V_{out}. \quad (6)$$

From Eq. (5), the next equation can be drawn:

$$V_{out} = V_{BA} = \frac{A_V}{1 + A_V} V_{os} \approx V_{os}. \quad (7)$$

From Eq. (7), points A and B copy the offset voltage of the amplifier. Therefore, the offset voltage is in storage on capacitor C_1.

4. Structure of the latch

Figure 5 shows the structure of the latch. It is a simple multivibrator. When clock CLK is low, the latch closes. When clock CLK is high, the latch works. The latch shows positive feedback and the rise and fall times of the latch are shorter than those of the amplifier. In order to understand the phenomenon, Figure 6 depicts the simple multivibrator. Figures 6(a) and 6(b) show the simplified positive feedback and its small-signal equivalent circuit with all devices in the saturation region respectively. In Fig. 6(a), $g_m = g_{m1} + g_{m3} = g_{m2} + g_{m4}$

Table 1. Performance comparison of the proposed comparators.

Performance	Ref. [2]	Ref. [5]	Ref. [7]	Ref. [8]	Ref. [9]	This design
Architecture	Preamp + Latch	Preamp + Latch	Dynamic + Latch	Dynamic + Latch	Preamp + Latch	Preamp + Latch
Technology (μm)	0.4 CMOS	0.35 CMOS	1.0 CMOS	0.35 CMOS	0.35 CMOS	0.5 CMOS
Supply voltage (V)	2.5	3.3	5	1.5	2	5
Offset (μV)	200	1000	3000	< 35000	469	600
Power consumption (μW)	250	200	–	69	3300	78
Speed (MHz)	13	> 10	50	25	1200	16
Area (μm^2)	140×100	300×28	–	–	4900	210×180

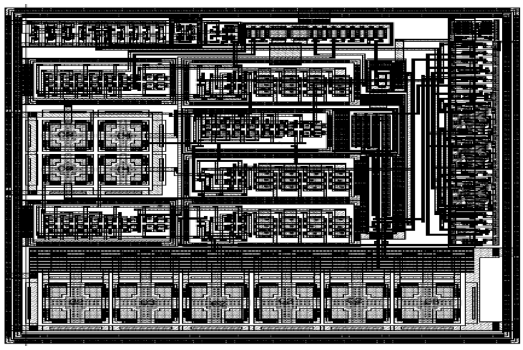

Fig. 7. Chip photograph of the comparator.

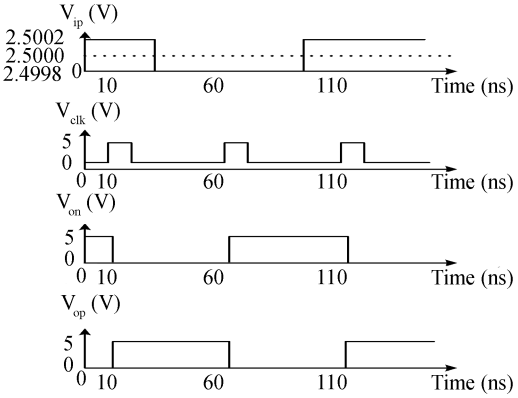

Fig. 8. Simulation result of the comparator.

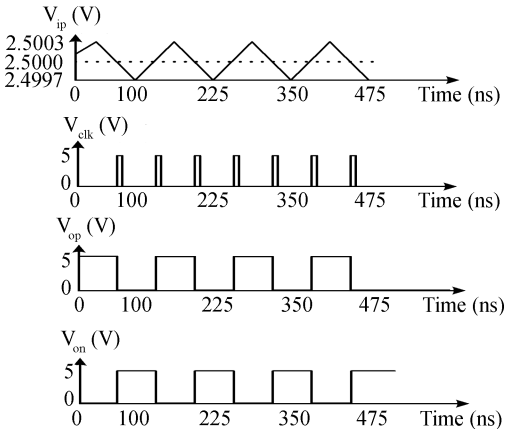

Fig. 9. Test result of the comparator.

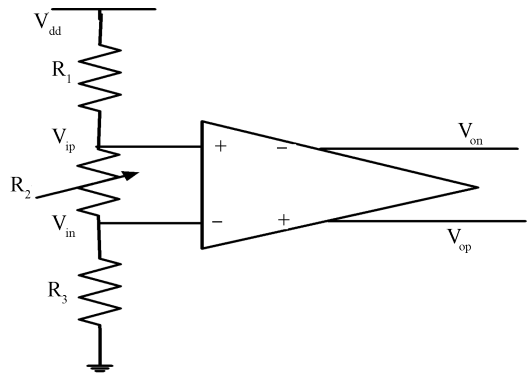

Fig. 10. Test schematic of offset voltage for the comparator.

and $g_d = g_{d1} + g_{d3} = g_{d2} + g_{d4}$. C is the capacitance loading of nodes A and B. It can easily be shown that the natural poles of the circuit are $s_{1,2} = \pm g_m/C$. Hence its transients are exponential functions with a time constant $\tau = C/g_m$. In the absence of positive feedback, if the inverter MOSFETs M1–M3 and MOSFETs M2–M4 are simply cascaded in an amplifier, the time constant is $\tau' = C/g_d$. The ratio of the time constant is $\tau/\tau' = g_d/g_m = 1/A$, where A is the gain of the inverter. Since typically $A = 10$, the latch can be about an order of magnitude faster than the amplifier.

5. Simulation and experiment results

The comparator was fabricated with 0.5 μm HYNIX mixed signal technology. The chip photograph is shown in Fig. 7. The size of the circuit was 210×180 μm^2.

Figure 8 shows the simulation result of the comparator with 0.5 μm HYNIX mixed signal technology. The signal between 2.4998 and 2.5002 V is introduced to V_{ip} and reference voltage 2.5 V, which is the dotted line, is applied to V_{in}. When the latch signal (CLK) changes from low-state voltage to high-state voltage, V_{on} changes to low-state voltage from high-state voltage. V_{op} transits to high-state voltage from low-state voltage if V_{ip} is larger than 2.5 V. The period of latch signal (CLK) is 20 MHz.

Figure 9 shows that typical operation waveforms are obtained from the measurement of the fabricated test chip. A ramp signal between 2.4997 and 2.5003 V is introduced to input port V_{ip} and the reference voltage 2.5 V is applied to another input port V_{in}. The polarity of the comparator for output ports V_{op} and V_{on} changes around $V_{ip} = 2.50$ V. From Fig. 9, it is shown that the function of the comparator is correct. The period of the ramp signal is 125 ns. In one period of ramp signal the latch signal (CLK) is two periods and the comparator changes twice. Therefore, the period of conversion for the comparator is 62.5

ns (16 MHz).

The test schematic of offset voltage for the comparator is presented in Fig. 10. When V_{ip} is larger than V_{in}, V_{op} is high level voltage and V_{on} is low level voltage. The adjustable resistor R_2 is regulated until voltage V_{op} is low level and voltage V_{on} is high level. At this time voltage V_{R2} is equal to the offset voltage. The test result of the offset voltage for this comparator is 600 μV.

Table 1 compares the performance of various comparators in the world. It can be seen from Table 1 that much performance already attains the advanced level for the design of this paper.

6. Conclusion

In this paper, a high speed comparator with three stage amplifier structure is developed. The test result shows that the circuit has an accuracy of 600 μV at 16 MHz, and dissipates only 78 μW of power dissipation at 5 V. The size of the chip is 210×180 μ m^2. The comparator has been successfully used in a 10 MSPS 12-bit A/D converter. The circuit can be also used in a less than 13-bit A/D converter.

References

[1] Pierluigi N, Fernando D, Pierangelo T. Noise analysis of regenerative comparators for reconfigurable ADC architectures. IEEE Trans Circuits Syst, 2008, 55(5):1441

[2] Shirai E. CMOS multistage preamplifier design for high speed and high resolution comparators. IEEE Trans Circuits Syst, 2007, 54(2):166

[3] Razavi B. Principles of data conversion system design. New York: IEEE Press, 1995

[4] Gregorian R. Introduction to CMOS op-amps and comparators.1999

[5] Degerli Y, Fourches N, Rouger M, et al. Low-power auto zeroed high-speed comparator for the readout chain of a CMOS monolithic active pixel sensor based vertex detector. IEEE Trans Nucl Sci, 2003, 50(4): 1709

[6] Razavi B. Design of analog CMOS integrated circuit. NY: Wiley, 2002

[7] Cusinato P, Bruccoleri M, Caviglia D D, et al. Analysis of the behavior of a dynamic latch comparator. IEEE Trans Circuits Syst, 1998, 45(3): 294

[8] Amaral P, Goes J, Paulino N, et al. An improved low voltage and low power CMOS comparator to be used in high speed pipeline ADCs. IEEE International Symposium on Circuits and Systems, 2002, 5: 26

[9] Wong Y L, Cohen M H, Abshire P A. A 1.2 GHz comparator with adaptable offset in 0.35 μm CMOS. IEEE Trans Circuits Syst, 2008, 55(9): 2584