Off-state avalanche breakdown induced degradation in 20 V NLDMOS devices*

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Abstract: Degradation behaviors of 20 V NLDMOS operated under off-state avalanche breakdown conditions are presented. A constant current pulse stressing test is applied to the device. Two different degradation mechanisms are identified by analysis of electrical data, technology computer-aided design (TCAD) simulations and charge pumping measurements. The first mechanism is attributed to positive oxide-trapped charges in the N-type drift region, and the second one is due to decreased electron mobility upon interface state formation in the drift region. Both of the mechanisms are enhanced with increasing avalanche breakdown current.

Key words: NLDMOS; avalanche breakdown; degradation; charge-pumping
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1. Introduction

Lateral-double-diffused-MOS (LDMOS) devices are often implemented in the standard CMOS process as high-voltage devices. They have advantages over vertical DMOS (VDMOS) devices as they can be easily integrated into the CMOS process without significant process changes, and the drift region can be easily optimized for different operating voltage requirements.

When LDMOS is used in switching applications, an unclamped inductive load would force the device to reach avalanche breakdown during on-to-off-state transient[1]. Operating under avalanche breakdown repeatedly may lead to device degradation, and even device failure. Although hot-carrier reliability (under saturation conditions) of LDMOS devices has widely attracted attention recently[2−7], much less attention has been paid to address the reliability of the device under off-state avalanche breakdown conditions[1, 8].

In this paper, the off-state avalanche breakdown induced degradation of 20 V NLDMOS is studied by a constant current pulse stressing test, TCAD simulations, and charge pumping measurements. The degradation behaviors under various current levels are analyzed and two different mechanisms are presented.

2. Device description

A schematic cross section of the NLDMOS transistor studied in this paper is shown in Fig. 1. The device was processed in 0.35 μm CMOS compatible BCD technology. The NDD and N^+ regions were implanted self-aligned to the poly-gate. The p-type channel region was also formed by self-aligned implantation to the poly-gate for a better process control of the channel length. Thick gate oxide was used to form a step for the field plate. The thickness of the thin gate oxide and the thick gate oxide is 7 nm and 50 nm, respectively. As can be seen, the drift of the device can be divided into three parts: accumulation region (acc), thick gate oxide overlapped region (to), and spacer region.

The width of the device is 20 μm. The operational voltages of the device are 20 V for drain (V_d) and 3.3 V for gate (V_g). The device has a threshold voltage of 0.7 V, off-state avalanche breakdown voltage of 28 V, and on-state resistance of 310 Ω.

3. Stressing test

To evaluate the damage created during fast on–off transient, a constant current pulse stressing test was performed on the drain with various current levels ranging from 1 to 100 μA, while other terminals were grounded. The width of the pulse is 0.05 s. During the stressing test, on-state resistance (R_{on}) was measured at V_{gs} = 3.3 V, V_{ds} = 0.1 V and saturation current (I_{dsat}) at V_{gs} = 3.3 V, V_{ds} = 20 V.

Figure 2 shows R_{on} degradation during the constant current pulse stressing under various current levels. As can be seen, R_{on} decreases significantly during the first few pulses, but then begins to increase, which is different from the phenomenon described in Ref. [1]. A higher current level leads to larger R_{on} reduction in the beginning, but eventually also greater degradation. After about 100 pulses, R_{on} degradation does not saturate.

The I_{dsat} degradation characteristic is shown in Fig. 3. The degradation behavior of I_{dsat} is not as obvious as R_{on}. When the current level is 1 μA, I_{dsat} increases a little at first, and then remains almost constant as the number of pulse increases. When

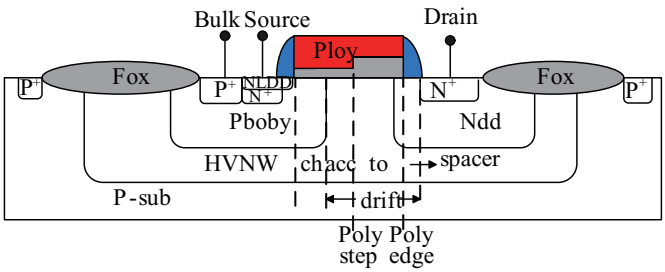

Fig. 1. Structure of LDMOS transistors used in this work.

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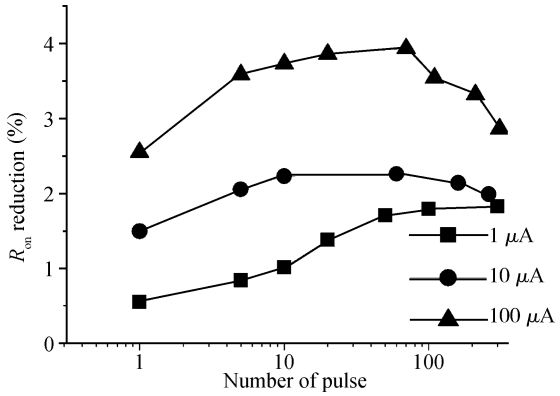


Fig. 2. Relationship between R_{on} reduction and number of pulses.

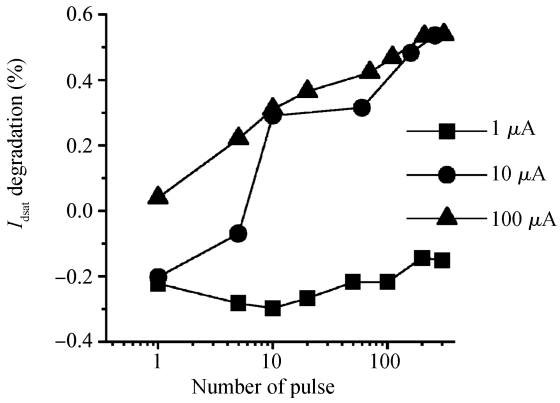


Fig. 3. Relationship between I_{dsat} degradation and number of pulses.

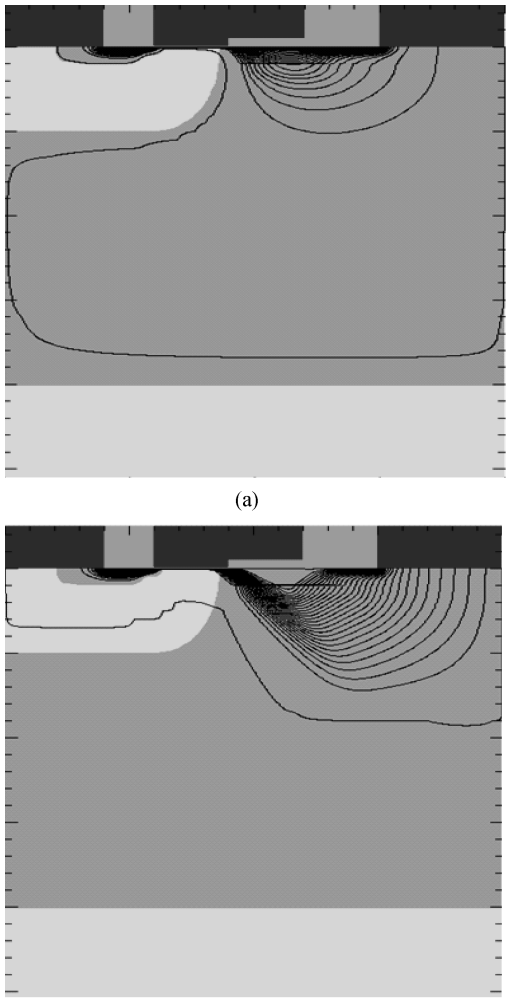
the current level is 100 μA, I_{dsat} decreases gradually. A higher current level leads to larger degradation. The I_{dsat} degradation at high current level does not show signs of saturation, either.

The threshold voltage (V_t) shift of this device is small, which indicates that the degradation in the channel is negligible.

4. TCAD simulations

TCAD simulations were performed to identify the degradation mechanism using Medici. As shown in Fig. 4(a), the current flow distribution for the R_{on} condition (V_{gs} = 3.3 V, V_{ds} = 0.1 V) is mainly confined to the surface. So R_{on} is the most critical electrical parameter to sense damage at the Si/SiO_2 interface[9]. Figure 4(b) shows the current distribution under I_{dsat} test conditions: V_{ds} = 20 V, V_{gs} = 3.3 V. The current flows out of the channel into the accumulation region and then drops into the N-drift before it is again collected at the drain contact at the surface. This depletion area pushes the current path away from the Si/SiO_2 interface, so that I_{dsat} will not be influenced unless damage at the Si/SiO_2 interface occurs in the channel or in the front part of the drift region. It makes sense that I_{dsat} changes much less than R_{on}. R_{on} is the most relevant parameter for switching applications.

The simulated distribution of impact ionization and perpendicular electric field along the surface of the device is depicted in Fig. 5, with V_{ds} = 28 V, V_{gs} = 0 V and I_d = 10 μA/μm. As can be seen in Fig. 5(a), two peaks of impact ionization are identified in the drift. The first region is located at the boundary of the accumulation and thick gate oxide overlapped regions, beneath the poly step in Fig. 1. The second one is at the boundary of the thick gate oxide overlapped region and spacer region, beneath the poly edge in Fig. 1.



(a)

(b)

Fig. 4. (a) Current distribution of R_{on}. (b) Current distribution of I_{dsat}.

The direction of the perpendicular electric field in the drift favors hole injection, as shown in Fig. 5(b). The peaks of perpendicular electric field also lie under the poly step and poly edge. The injection of hot holes may result in the generation of positive oxide-trapped charges, or interface states. Generally, interface states are generated in the high impact ionization region. So interface states may generate in the whole drift region, especially beneath the poly step and poly edge.

5. Charge pumping measurements

Charge pumping (CP) measurements were performed to verify the assumption, by measuring I_{cp} at the body contact while pulsing the gate and grounding source and drain. The base voltage of the pulse is swept from –4 to 0.5 V with the pulse amplitude fixed at 1.5 V and the frequency at 5 MHz. The rise and fall times of the pulse train are 0.1 μs.

For the structure shown in Fig. 1, the poly gate overlapped regions of the device, including both channel and drift, are

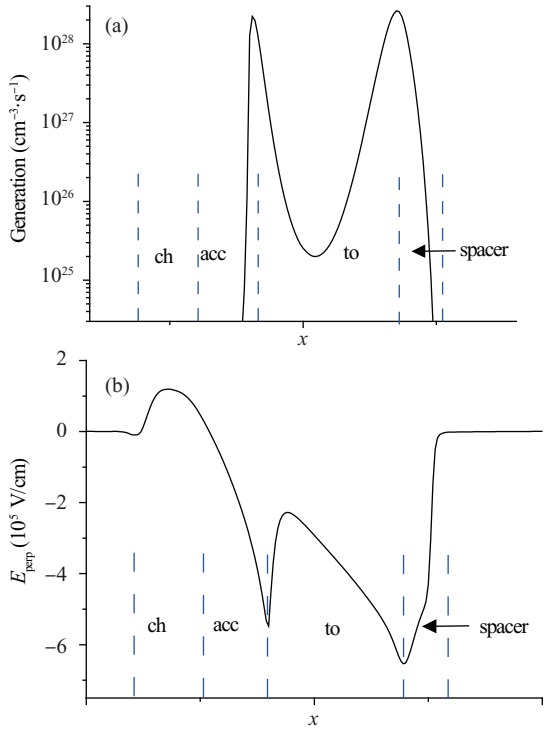


Fig. 5. (a) Simulated distribution of impact ionization along the surface of NLDMOS at V_{ds} = 28 V, V_{gs} = 0 V, I_d = 10 μA/μm. (b) Simulated distribution of perpendicular electric field along the surface of NLDMOS at V_{ds} = 28 V, V_{gs} = 0 V, I_d = 10 μA/μm.

pumped. The channel region is like a standard NMOS with thin gate oxide and the drift region is somewhat like a PMOS with thick gate oxide.

Figure 6 shows the CP curves of a fresh device with the drain closed and open. When the drain is closed, the left component of the CP signal at low base level originates from the drift region, and the right component is due to both channel and drift regions. This can be verified by leaving the drain floating open. As can be seen in Fig. 6, the left part of the CP signal completely disappears when the drain is left open. Because all necessary electrons have to be supplied by the source, no CP current will flow as long as the channel region is not inverted. When the channel region is inverted, the drift region can be filled with electrons from the source. So the two curves coincide with each other at high base level.

The charge pumping curves before and after 100 current pulses are shown in Fig. 7. After the stress, the left component of the curves shows an obvious negative shift, indicating positive charge trapped in the oxide of the drift region. Additionally, the left component shifts upwards after stressing, proving the generation of interface states in the drift region. As the current level increases, the negative and upward shifts of the curves become more obvious, suggesting the increase of both positive oxide-trapped charges and interface state generation. The CP curve in the channel seldom changes, in accordance with the fact that the threshold voltage changes little.

6. Results and discussions

Based on analysis of the electrical data, simulation results and charge pumping measurements, two degradation mecha-

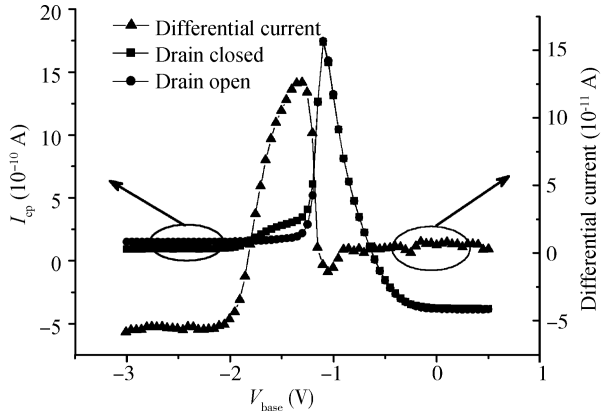


Fig. 6. Charge pumping curves of a fresh device with drain closed and drain left open.

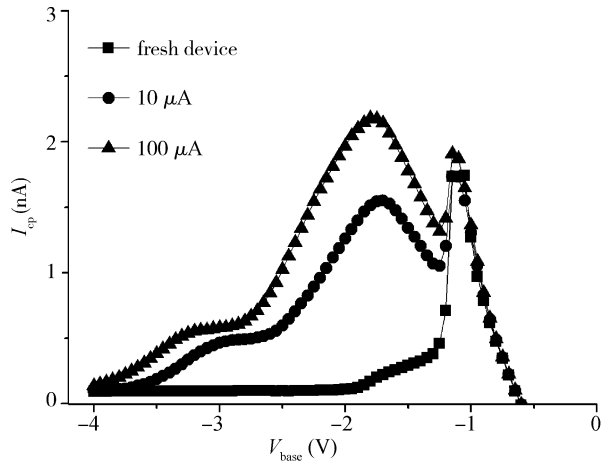


Fig. 7. Charge pumping curves of NLDMOS with increasing number of pulses under various current levels.

nisms are identified as follows:

(1) Mechanism 1: Positive oxide-trapped charge in the drift region

This mechanism plays the leading role at the beginning of the stressing, and comes to saturation later, as R_{on} reaches its minimum value after dozens of pulses. The mechanism is confirmed by the negative shift of the left component of CP curves in Fig. 7. Negative mirror charge will be formed in the top silicon of the drift region, resulting in an effective increase of the top N-drift concentration, so that R_{on} decreases.

The mechanism increases when the avalanche breakdown current increases. As the current increases, the impact ionization becomes more serious, and more hot holes can be injected into the oxide.

(2) Mechanism 2: Interface state formation in the drift region

The second mechanism becomes obvious as the number of pulses increases, and does not saturate after over 100 pulses. This mechanism is verified by the increase of the amplitude of the CP curves attributed to the drift region, shown in Fig. 7. Due to the increased scattering of the carriers at the interface states, the mobility of carriers is reduced, hence R_{on} will increase. The interface state generation can take place in the whole drift re-

gion, with two peaks located under the poly step and poly edge (Fig. 1). This mechanism also increases with stressing current.

7. Conclusions

It has been clearly demonstrated that two competing degradation mechanisms are present in 20 V NLDMOS transistors under avalanche breakdown conditions. Analysis of the stressing test results, TCAD simulations and charge pumping measurements indicates two mechanisms: positive oxide-trapped charge in the drift region and interface state formation in the drift region. The hot hole trapping mechanism is the primary effect at the beginning. This mechanism leads R_{on} to decrease. As the number of pulses increases, interface state formation in the drift becomes more obvious. The second mechanism will increase R_{on}. Both mechanisms are enhanced with the increase of avalanche breakdown current.

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