Exponential dependence of potential barrier height on biased voltages of inorganic/organic static induction transistor

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Abstract: The exponential dependence of the potential barrier height ϕ_c on the biased voltages of the inorganic/organic static induction transistor (SIT/OSIT) through a normalized approach in the low-current regime is presented. It shows a more accurate description than the linear expression of the potential barrier height. Through the verification of the numerical calculated and experimental results, the exponential dependence of ϕ_c on the applied biases can be used to derive the I–V characteristics. For both SIT and OSIT, the calculated results, using the presented relationship, are agreeable with the experimental results. Compared to the previous linear relationship, the exponential description of ϕ_c can contribute effectively to reduce the error between the theoretical and experimental results of the I–V characteristics.

Key words: SIT; OSIT; potential barrier height; normalized approach; I–V characteristics
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1. Introduction

The static induction transistor (SIT) features vertical shorter and narrower multi-channels, lower channel doping concentration and smaller size compared to those of the BJT and FET. Due to the excellent performances of its high voltage, high frequency operation, small series of resistance and low noise, it always attracts people's great attention. For the basic inorganic SIT and the organic SIT (OSIT), many works focus on optimizing the structures and analyzing the operational mechanisms[1−9]. In the low-current regime, the device operation can be understood by considering the dependence of the potential barrier into the channel from the applied biases. As a first-order approximation, the potential barrier height ϕ_c is considered as a linear of the gate voltage V_{GS} and the drain voltage V_{DS} [5]. Furthermore, Strollo *et al.* developed a self-consistent model for analyzing the direct current characteristics of SIT, and noted that the relationship between ϕ_c and applied biases should be more accurate than linear. However, they didn't show details about this accurate description[6]. At the same time, the first-order analytical description based on some assumptions may limit its validity, such as simplifying gate geometries. Especially to OSIT, there is no effective analysis model to describe its operational mechanism.

In this paper, based on the numerical simulated results, an exponential relationship between ϕ_c and the applied voltages to analyze the I–V characteristics of SIT/OSIT through a normalized approach in the low-current regime is investigated. Employing this exponential relationship, which is verified extensively by numerical calculations and theoretical analysis, the detailed I–V characteristics are derived. For SIT and OSIT, the calculated results agree well with the experimental ones. The validity of the detailed I–V characteristics of SIT/OSIT in the low-current regime can be proved well.

2. Brief descriptions of device structures

In this work, we will focus on three device structures, namely surface-gate SIT (SGSIT), buried-gate SIT (BGSIT) and OSIT, which are on the behalf of the high-frequency, high-power and high-transfer characteristics. The traditional SITs including SGSIT and BGSIT are fabricated in our group[2−4]. However, for OSIT, a numerical simulation is carried out, in which the device structural parameters come from Ref. [7]. Figure 1(a) shows a cross section and dimensions of SGSIT, fabricated using conventional Si processes. The n^--substrate is single-crystal silicon lightly-doped with donor concentration of 5×10^{13} cm^{-3}. The p^+–n^- gate-junction is formed by diffusing acceptor impurities into the n^--substrate, with a surface concentration of 5×10^{18} cm^{-3}, a junction depth of about 7 μm, and the gate-to-gate space of 2.4 μm. The n^+-source contact layer is doped with a surface concentration of 1×10^{19} cm^{-3} and a depth of 1 μm.

As shown in Fig. 1(b), the gate stripes of BGSIT are buried under the epitaxial layer in the channel. The channel, source, drain and gate are doped at impurity concentrations of $N_{Sub} = 5 \times 10^{13}$ cm^{-3}, $N_S = 1 \times 10^{19}$ cm^{-3}, $N_D = 1 \times 10^{19}$ cm^{-3}, and $N_A = 1 \times 10^{19}$ cm^{-3}, respectively. A 15-μm-thick n-type epitaxial layer with donor concentration of 5×10^{15} cm^{-3} is grown on the wafer to bury the gate stripes. The diffusion depth in the source region is 1.5 μm and the depth of a p^+–n^- gate-junction is 7 μm with a width of 1 μm. The distance between gate and gate is 2 μm.

The cross section and dimensions of OSIT are reported in Fig. 1(c). Firstly, a CuPc film with a thickness of approximately 100 nm is deposited on the source electrode Au formed glass substrate. Secondly a grid-type gate electrode Al with a thickness of 25 nm is formed on the CuPc film by a shadow evaporation technique[7]. Thirdly, the second CuPc film of approximately 100 nm is deposited. Finally, the drain electrode Au (30 nm thickness) is fabricated. The channel length is 200 nm, and

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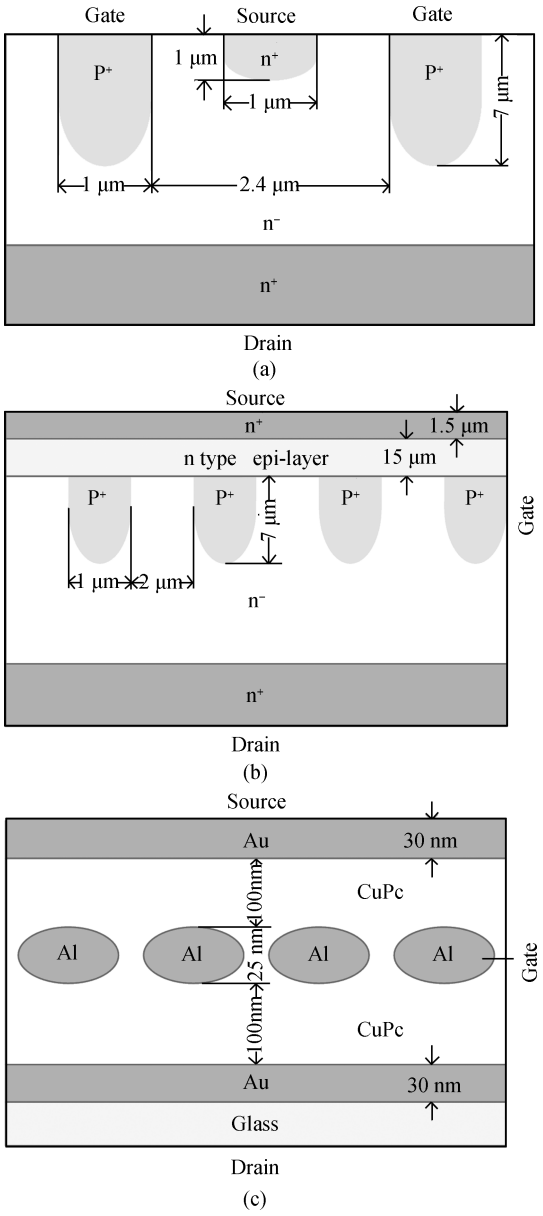

Fig. 1. Cross-section and dimensions of (a) SGSIT, (b) BGSIT, and (c) OSIT.

the gate gap is 7 μm. The channel width is 100 nm estimated by the simulated results which keep the good accordance with the experimental data as shown in Ref. [7].

3. Exponential dependence of potential barrier height on biased voltages

3.1. Current analysis

The numerical device simulations have been carried out by using the numerical simulator SG-framework based on the finite-difference method. The gate junction boundaries have been assumed of cylinder shape as shown in Fig. 1, which are suited for the practical situation when the standard diffusion technology is employed to fabricate the device. SGSIT is taken as the first example to derive its exponential relationship between ϕ_c and biased voltages. Similarly, the exponential relationship of BGSIT and OSIT are also proposed as well.

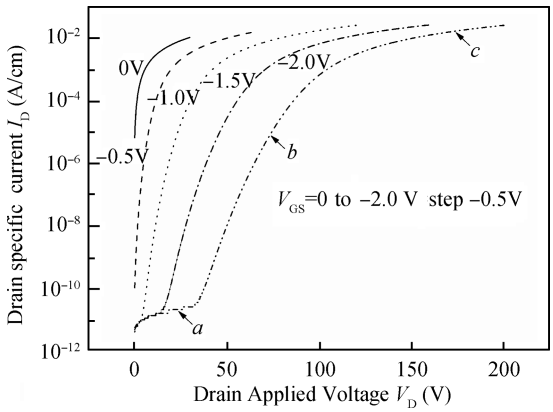

Fig. 2. I_D–V_D curves of the SGSIT in log scales.

The I_D–V_D curves of SGSIT in log scales obtained with the numerical simulations are reported in Fig. 2. It can be clearly seen that in the lower-current range (up to point a), I_D is negligible small due to the thermal generation of carriers in the space charge region of the gate junction. In other words, the device operates in a "dead region" because the currents are limited by the thermal generation. For a normally-off SIT, the barrier can be sufficient to block the source to the drain current flow even at zero gate bias. With the increasing of V_{DS}, conduction is then achieved by the application of a reverse bias to V_{GS}, lowering the potential barrier in the channel and allowing the electronics from the source to pass to the drain. The high-current range (up to point c) where the carrier feedback on the potential distribution at the saddle point causes the potential minimum to be pinned and the effective channel to increase, with a triode-like shape. However, in the low-current range (up to point b), the electrons transport from source to drain is modulated by ϕ_c, and I_D is exponentially related to the saddle potential. As a result, the exponential branch of the SIT characteristics in the low-current regime is due to an almost linear lowering of the potential barrier by the drain and the gate voltages. I_D can be expressed by:

$$I_D = I_S = I_0 \exp\left(-\frac{q\phi_c}{kT}\right) = \frac{qW_C N_{Sub} D_n}{L_C} \exp\left(-\frac{q\phi_c}{kT}\right), \quad (1)$$

$$\phi_c = \eta^* \left(V_{GS} + \frac{1}{\mu^*} V_{DS}\right), \quad (2)$$

where W_C is the effective channel width, L_C is the effective channel length, D_n is the electron diffusion coefficient, N_{Sub} is the n^--substrate doping concentration, and η^* and μ^* mean the effective applied gate biases and the voltage amplification factor, respectively. They are related to the device geometrical parameters. W_C, L_C, D_n and N_{Sub} remain constant for the same device structure and I_D will be controlled by ϕ_c. As a first-order approximation, ϕ_c is expressed as Eq. (2). In practice, a more accurate dependence of ϕ_c on the drain and gate biases can be obtained from Fig. 3.

3.2. Exponential relationship of potential barrier height and normalized approach

As the mentioned of Strollo in Ref. [6], ϕ_c is a non-linear function of the applied voltages. The same changing regularity of the relationship between ϕ_c and applied biases of SGSIT

with the numerical calculations is shown in Fig. 3(a). Through normalizing ϕ_c and V_{DS}, the dependence of ϕ_c on V_{DS}at different V_{GS} can be obtained.

It is known that ϕ_c is modulated by the combined effect of V_{DS}, V_{GS}, V_{Sbi} and V_{Gbi}, where $V_{Sbi} = (kT/q)\ln(N_S/N_{Sub})$ is the build-in potential barrier between the n^+-source and the n^--substrate, and $V_{Gbi} = (kT/q)\ln\left(N_G N_{Sub}/n_i^2\right)$ is the build-in potential barrier of the p^+–n^- gate-junction. As shown in Fig. 3(a), ϕ_c decreases very quickly and eventually becomes pinned with increasing V_{DS}. When ϕ_c decreases to V_{Sbi} (0.318 V) of SGSIT, there is a turning point and the decreasing becomes slow. Since the negative V_{GS} and positive V_{DS} have a contrary effect on controlling ϕ_c, ϕ_c can drop to equal to V_{Sbi} when the interaction between V_{GS} and V_{DS} has been cancelled out.

In the normalized process, we need to define two normalized factors V_{D0} and ϕ_{c0}. Here, V_{D0} equals V_{DS} when ϕ_c drops to V_{Sbi} at different V_{GS}. And ϕ_{c0} can be expressed as:

$$\phi_{c0} = V_{GS} + V_{Cbi} = V_{GS} + V_{Gbi} - \frac{qN_{Sub}}{2\varepsilon_0\varepsilon_{Si}}\left(\frac{W_C}{2}\right)^2, \quad (3)$$

where V_{Cbi} is the potential barrier height of the channel in the intrinsic condition (without any applied biases), which consists of two parts: the build-in potential barrier height V_{Gbi} of p^+–n^- and the voltage drop of the depletion region between the channel and gate junction. Then the normalized curves of $(\phi_c - V_{Sbi})/\phi_{c0}$ versus V_{DS}/V_{D0} at different V_{GS} are shown in Fig. 3(a). It is found that the normalized curves are overlapped at different V_{GS}, which means the normalized ϕ_c/ϕ_{c0} are unaffected by the applied voltages for the same device structure. The normalized curves can be described as an exponential relationship as follows:

$$(\phi_c - V_{Sbi})/\phi_{c0} = f(V_{DS}/V_{D0}), \quad (4)$$

$$f(x) = A_1 \exp(-x/B_1), \quad (5)$$

where A_1 and B_1 are the constants with related to the same device structure. Furthermore, the potential barrier height ϕ_c can be expressed by:

$$\phi_c = \phi_{c0} f\left(\frac{V_{DS}}{V_{D0}}\right) + V_{Sbi} = A_1(V_{GS} + V_{Cbi}) \times \exp\left(-\frac{V_{DS}}{B_1 V_{D0}}\right) + V_{Sbi}. \quad (6)$$

An exponential relationship between ϕ_c and applied biases through the normalized approach has been presented from Eq. (6).

In order to verify the relationship being universal, the exponential relationship of ϕ_c for BGSIT and OSIT with the same geometrical and material parameters as shown in Figs. 1(b) and 1(c) will be derived. Their potential barrier height distributions with different V_{GS} and V_{DS}, and normalized curves are shown in Figs. 3(b) and 3(c), respectively. Through the same processes as the above-described, finding V_{D0} at the different V_{GS} and calculating ϕ_{c0}, the normalized procedures to ϕ_c and V_{DS} in different V_{GS} can be done.

For BGSIT, V_{Sbi} is equal to 0.359 V by calculation. And for OSIT, CuPc films show p-type semiconducting properties,

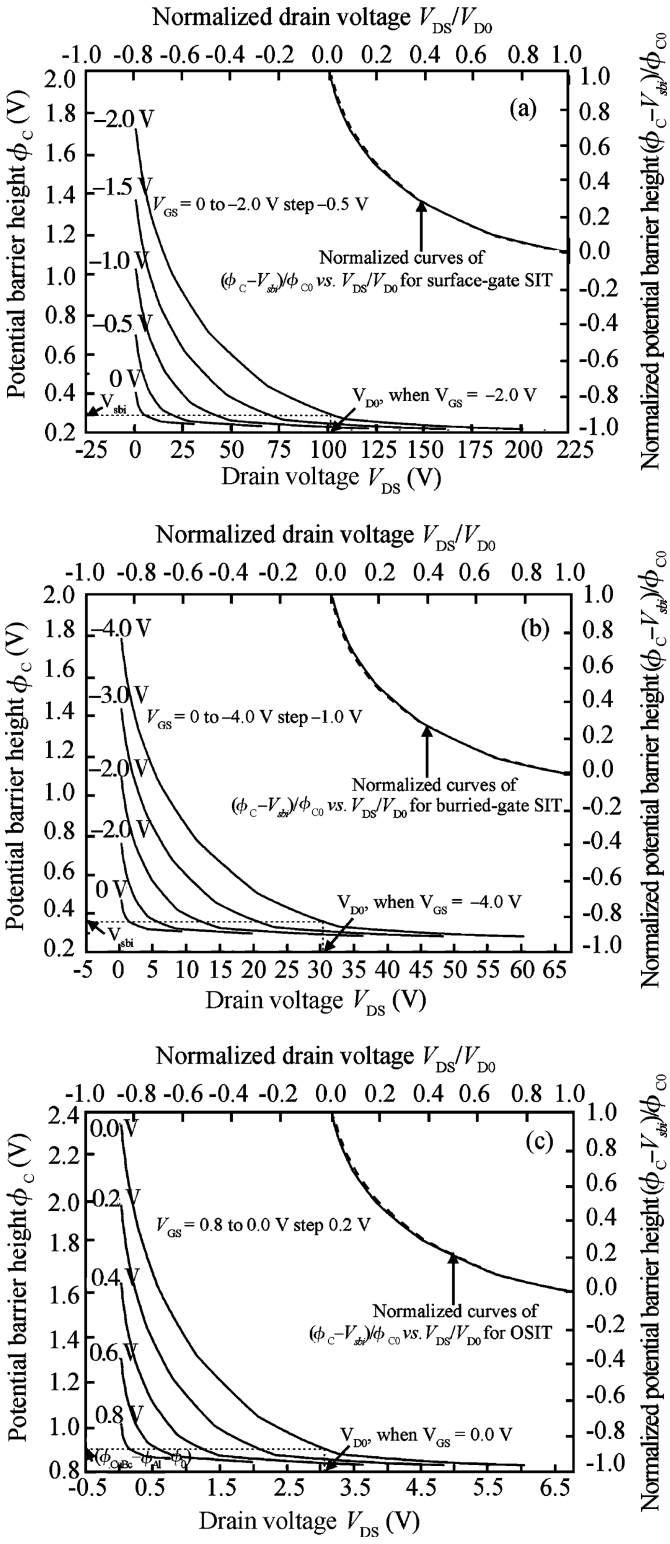

Fig. 3. Potential barrier height ϕ_c versus drain voltage I_{DS} in different gate voltage V_{GS} and their normalized curves of (a) SGSIT, (b) BGSIT, and (c) OSIT. The left is ϕ_c distributions and the right shows the normalized curves.

make an ohmic contact with Au electrodes and form a Schottky barrier contact with Al gate electrode. The injected hole carriers from the source flow toward the drain region through the potential barrier near the gate electrode. The carrier flow is controlled by the potential barrier height depending on the

Table 1. Comparisons between normalized parameters and first-order approximated parameters of SGSIT, BGSIT and OSIT.

	Simulated results					Calculated results		Compared results	
	A_1	B_1	m	n	l	η^*	μ^*	$-B_1 n \approx \mu^*$	$A_1 \approx \eta^*$
Surface-gate SIT									
$L_C/W_C = 2.9$	0.95	0.34	12.90	−22.90	4.40	0.79	7.74	8	1
Buried-gate SIT									
$L_C/W_C = 3.59$	1.0	0.37	9.0	−36.60	13.80	0.87	13.64	14	1
OSIT									
$L_C/W_C = 2.0$	0.89	0.42	2.50	−5.60	3.0	0.58	2.71	3	1

gate voltage[7]. Since the highest occupied molecular orbital (HOMO) levels of CuPc is 5.2 eV below the vacuum level and the work function of Al is 4.25 eV[8], the build-in potential barrier height of OSIT can be approximately calculated by $\phi_{\mathrm{CuPc}} - \phi_{\mathrm{Al}} - \phi_0 = 0.91$ V, where $q\phi_0$ is the energy level of surface state of CuPc with about 0.04 eV[9]. Thus we can find V_{D0} of OSIT at the different V_{GS}, which equals V_{DS} when ϕ_{c} drops to the build-in potential barrier height of OSIT (0.91 V). And the normalized potential barrier height is also calculated in different applied gate biases by $\phi_{\mathrm{c0}} = V_{\mathrm{GS}} + V_{\mathrm{Cbi}} = V_{\mathrm{GS}} + (\phi_{\mathrm{CuPc}} - \phi_{\mathrm{Au}} - \phi_0) = V_{\mathrm{GS}} + 0.36$ V, where the work function of Au ϕ_{Au} is 4.8 eV[9]. For the different device structure, the exponential relationship between ϕ_{c} and applied voltages are coincident with Eq. (6).

3.3. Discussions

Figure 4 shows the normalized curves of the potential barrier height versus drain voltages of SGSIT, BGSIT and OSIT at different gate voltages. It is clear that though the normalized curves are different for different device structures, the shapes are similar and the potential barrier height is exponentially related to applied biases as described in Eq. (6).

Figure 5 shows the curves of the normalized values of drain voltages various with V_{GS}. From the fitted curves, V_{D0} is a quadratic function of V_{GS}, which can be concluded as:

$$V_{\mathrm{D0}} = V_{\mathrm{D0}}(V_{\mathrm{GS}}) = mV_{\mathrm{GS}}^2 - nV_{\mathrm{GS}} + l, \tag{7}$$

where m, n, l are all constants with related to the device structures. Substituting Eq. (7) into Eq. (6), a detailed expression of ϕ_{c} with applied biases is achieved as:

$$\phi_{\mathrm{c}} = A_1 (V_{\mathrm{GS}} + V_{\mathrm{Cbi}}) \exp\left(-\frac{V_{\mathrm{DS}}}{B_1 \left(mV_{\mathrm{GS}}^2 + nV_{\mathrm{GS}} + l\right)}\right) + V_{\mathrm{Sbi}}. \tag{8}$$

Equation (8) can be simplified based on the Taylor expansions as ($V_{\mathrm{GS}} >> V_{\mathrm{Cbi}}$):

$$\phi_{\mathrm{c}} = A_1 V_{\mathrm{GS}} \exp\left(-\frac{V_{\mathrm{DS}}}{B_1 n V_{\mathrm{GS}}}\right) + V_{\mathrm{Sbi}}. \tag{9}$$

As the first-order approximation of Eq. (9), ϕ_{c} shows linear with applied voltages as the expression of Eq. (1). Comparing Eq. (9) with Eq. (2), we define A_1 as $\partial\phi_{\mathrm{c}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})/\partial V_{\mathrm{GS}}$ meaning the effective applied gate biases η^*, and $-1/B_1 n$ as $\partial\phi_{\mathrm{c}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})/A_1\partial V_{\mathrm{DS}}$ representing the voltage amplification factor $1/\mu^*$. In the first-order approximation, $\eta*$ and μ^* are calculated as $\eta^* = 1 - 2\sqrt{\mu_0}/(\mu_0 + 1)$ and $1/\mu^* = \sqrt{\mu_0}/\left(\mu_0 + 1 - 2\sqrt{\mu_0}\right)$, respectively, where $\mu_0 = \exp(\pi L_{\mathrm{C}}/2W_{\mathrm{C}})$ is decided by the channel length and width.

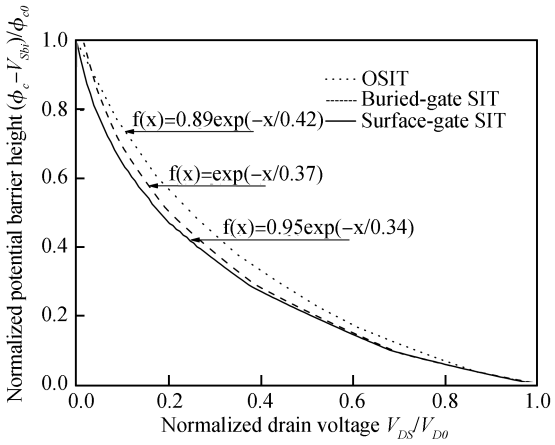

Fig. 4. Normalized potential barrier height versus normalized drain voltage for the different devices.

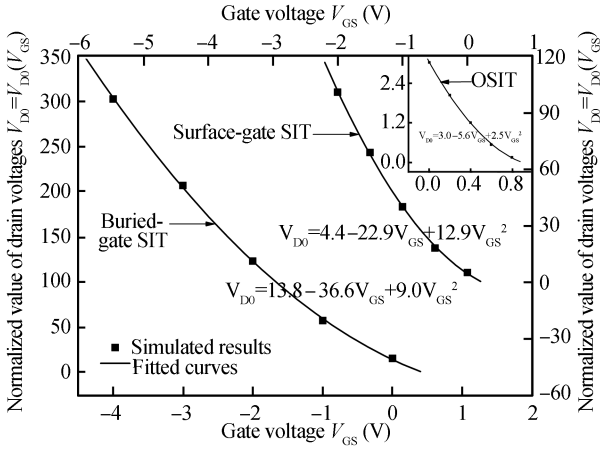

Fig. 5. Normalized value of drain voltage $V_{\mathrm{DS}}/V_{\mathrm{D0}}$ various with gate voltage V_{GS} for the different devices.

Table 1 reports the values of A_1, B_1, m, n and l of SGSIT, BGSIT and OSIT, and their η^* and μ^* in the first-order approximation. The simulated results show few differences with the calculated results ($A_1 \approx \eta^*$ and $-B_1 n \approx \mu^*$).

3.4. Verifications of exponential relationship of potential barrier height

Based on the exponential dependence of ϕ_{c} on the bias voltages in Eq. (9), the detailed description of the I–V characteristics for SIT/OSIT is concluded as:

$$I_{\mathrm{D}} = I_{\mathrm{S}} = I_0 \exp\left(-\frac{q\phi_{\mathrm{c}}}{kT}\right) = I_0 \exp\left\{-\frac{q}{kT}\left[\eta^* V_{\mathrm{GS}}\right.\right.$$

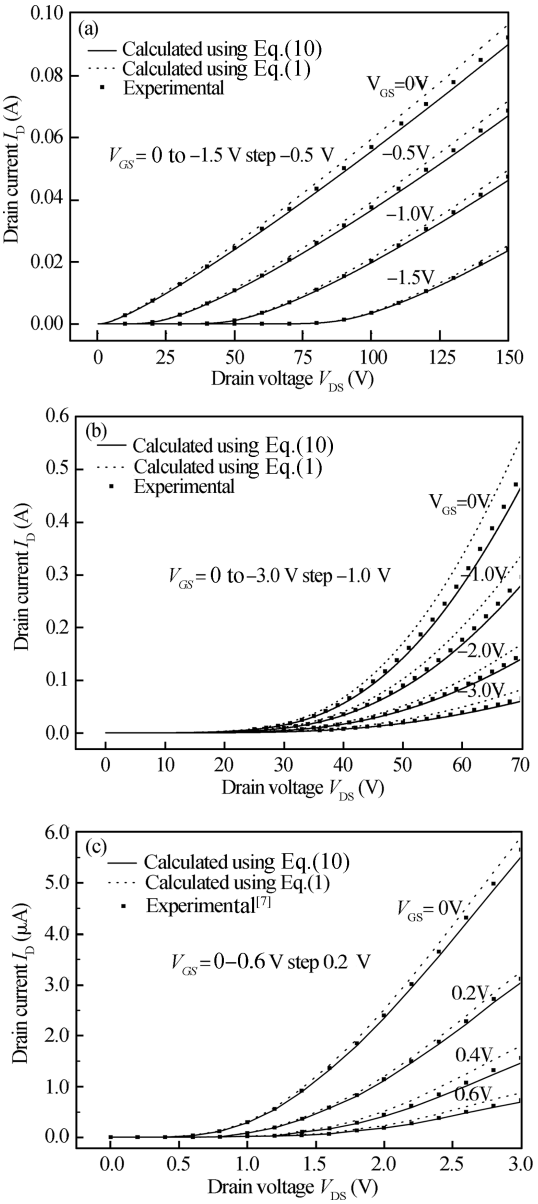

Fig. 6. I–V characteristics of (a) SGSIT, (b) BGSIT and (c) OSIT.

$$\times \exp\left(\frac{V_{\mathrm{DS}}}{\mu^* V_{\mathrm{GS}}}\right) + V_{\mathrm{Sbi}}\Bigg]\Bigg\}, \qquad (10)$$

where $I_0 = qW_{\mathrm{C}}N_{\mathrm{Sub}}D_{\mathrm{n}}/L_{\mathrm{C}}$ is the saturated current, and η^* and μ^* both have the same definitions as the above-mentioned. For OSIT, the drain current is approximately two the carrier density, n, and field effective mobility μ can be estimated as $n = 8 \times 10^{15}$ cm^{-3} and $\mu = 6 \times 10^{-7}$ cm^2/(V·s), respectively[7]. Figure 6 show the I–V characteristics of SGSIT, BGSIT and OSIT, which are calculated by Eq. (10), Eq. (1) and compared with the experimental data, respectively. The results calculated by Eq. (10) have a much better agreement with the experimental data than the calculated by Eq. (1). The error between the experimental and theoretical data using Eq. (10) is around 2.5%, smaller than 5.0% using Eq. (1). It indicates that Equation (10) is more accurate in describing the operational mechanism of SIT/OSIT in the low-current regime.

4. Conclusion

Exponential dependence of the potential barrier height ϕ_{c} on the biased voltages of SIT/OSIT has been presented as $\phi_{\mathrm{c}} = \eta^* V_{\mathrm{GS}} \exp(-V_{\mathrm{DS}}/\mu^* V_{\mathrm{GS}}) + V_{\mathrm{Sbi}}$ which provides a detailed description of the exponential relationship between the potential barrier height and applied biases in the low-current regime. The exponential relationship can be used to derive the detailed I–V characteristics of SIT/OSIT. Based on the verification of the numerical calculation and experimental results, the description of the I–V characteristics using the exponential relationship between ϕ_{c} and applied biases is more accurate, and can contribute effectively to reduce the error between the theoretical and experimental data (around 2.5%). The discussions above are universal and applicable to the SIT/OSIT operated in unipolar mode in the low-current regime.

References

[1] Henning J P, Przadka A, Melloch M R, et al. A novel self-aligned fabrication process for microwave static induction transistors in silicon carbide. IEEE Electron Device Lett, 2000, 21(12): 578

[2] Yang Jianhong, Wang Zaixing, Li Siyuan. An SIT-BJT operation model for SITs in the blocking state. Journal of Semiconductors, 2008, 29(4): 645

[3] Wang Yongshun, Wu Rong, Liu Chunjuan, et al. Researches on the injected charge potential barrier occurring in the static induction transistor in the high current region. Semicond Sci Technol, 2008, 23(2): 025005

[4] Wang Yongshun, Li Hairong, Wang Ziting, et al. Improvements on high voltage performance of power static induction transistors. Journal of Semiconductors, 2009, 30(10): 104003

[5] Mochida Y, Nishizawa J I, Ohmi T, et al. Characteristics of static induction transistors: effects of series of resistance. IEEE Trans Electron Devices, 1978, 25(7): 761

[6] Strollo A G M, Spirito P. A self-consistent model for the SIT DC characteristics. IEEE Trans Electron Devices, 1991, 38(8): 1943

[7] Kudo K, Iizuka M, Kuniyoshi S, et al. Device characteristics of lateral and vertical type organic field effect transistors. Thin Solid Films, 2001, 393: 362

[8] Fujimoto K, Hiroi T, Kudo K, et al. High-performance, vertical-type organic transistors with build-in nanotriode arrays. Adv Mater, 2007, 19: 525

[9] Horowitz G. Organic thin film transistors: from theory to real devices. Journal Materials Research, 2004, 19(7): 1946