Low power CMOS preamplifier for neural recording applications*

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Abstract: A fully-differential bandpass CMOS (complementary metal oxide semiconductor) preamplifier for extracellular neural recording is presented. The capacitive-coupled and capacitive-feedback topology is adopted. The preamplifier has a midband gain of 20.4 dB and a DC gain of 0. The –3 dB upper cut-off frequency of the preamplifier is 6.7 kHz. The lower cut-off frequency can be adjusted for amplifying the field or action potentials located in different bands. It has an input-referred noise of 8.2 μVrms integrated from 0.15 Hz to 6.7 kHz for recording the local field potentials and the mixed neural spikes with a power dissipation of 23.1 μW from a 3.3 V supply. A bandgap reference circuitry is also designed for providing the biasing voltage and current. The 0.22 mm^2 prototype chip, including the preamplifier and its biasing circuitry, is fabricated in the 0.35-μm N-well CMOS 2P4M process.

Key words: neural signal amplifier; low noise; low power; subthreshold circuit design
DOI: 10.1088/1674-4926/31/4/045002 **PACC:** 2960C; 8700 **EEACC:** 1220; 1130; 7510D

1. Introduction

Simultaneously recording the activity of neurons is of great interest to neuroscientists and clinicians currently[1, 2], and implantable MEMS multi-channel microelectrodes have been used to capture the field or action potentials of many neurons in a localized region of tissue[3, 4]. Due to the high impedance of the interface between tissue and electrodes[3–5], the environmental electrical noise readily couples to the weak neural signals[5–7]. To minimize this noise, preamplifiers have been designed to be placed close to the recording electrodes. Additionally, in order to provide the researchers an access to observe thousands of neurons simultaneously, circuitry for multichannel neural signal acquisition or processing must be integrated with such implantable recording arrays[7–11]. Therefore, a robust integrated preamplifier, as the front-end module before any further signal processing, is highly required by these hybrid devices.

In order to capture the neural potentials in the range of tens of microvolts to hundreds of microvolts in the frequency band of sub-hertz to several kilohertz, many integrated neural signal amplifiers have been designed with different constraints such as low noise, low power, low supply voltage and low cut-off frequency[6–16]. Wise's group designed the first integrated amplifier in 1971[5] and have contributed significantly to the development of this field in the past thirty years[3, 7, 8, 11, 12]. The integrated amplifier with capacitive-couple and capacitive-feedback topology was originally proposed by Harrison[6], which might be the most successful work until now and has been widely cited in past years[12, 15, 16]. For this topology, the input coupled capacitors are in combination with the large equivalent input impedance to suppress the DC-offset of hundreds of microvolts at the electrode–electrolyte interface. The capacitive feedback configuration can make the gain of this preamplifier independent of process variations.

In this paper, we present a CMOS fully-differential integrated preamplifier with the capacitive-couple and capacitive-feedback topology for extracellular neural recording. The functionality of the fabricated chip is proved by amplifying the prerecorded neural signals from the cortex of a Wistar rat.

2. Circuit design

The overall architecture of our integrated preamplifier is shown in Fig. 1(a). The bio-potentials from the electrode are AC coupled to the amplifier through the input capacitor C_1 to eliminate the DC offset voltage which was caused by elec-

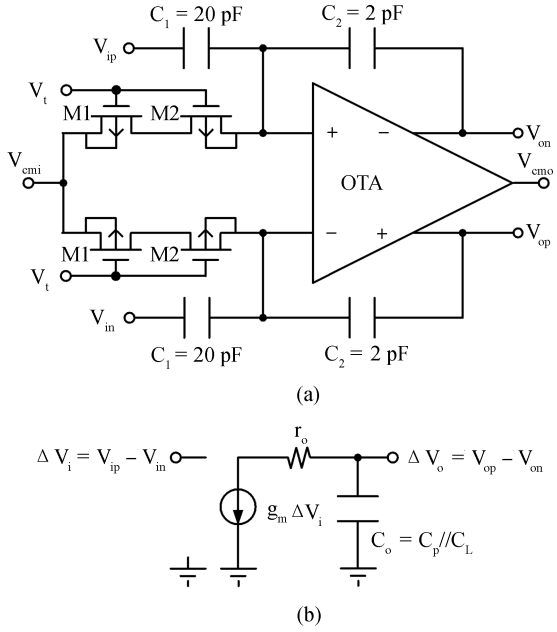

Fig. 1. (a) General block of the preamplifier. (b) Ideal single-pole OTA model.

* Project supported by the National Natural Science Foundation of China (Nos. 60776024, 60877035, 60976026, 90820002) and the National High Technology Research and Development Program of China (Nos. 2007AA04Z329, 2007AA04Z254).
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Received 15 October 2009, revised manuscript received 3 November 2009

trochemical effects at the tissue–electrode interface. The high-gain OTA converts the probe voltage at the negative input terminal into a picoampere-sized current. The current first passes through C_1 and then through the output capacitor C_2. If we use the structure with single-ended output, the output signal will contain unwanted signals caused by picoampere sources that capacitively couple to the OTA's negative input[5]. The fully-differential structure can eliminate the common-mode interference of these unwanted sources. Additionally, this structure also has good performance on power-supply rejection and common-mode rejection.

The transfer function of the proposed preamplifier with capacitive-couple and capacitive-feedback topology can be described as

$$H(s) = \left[\frac{C_2}{C_1} + \left(1 + \frac{C_2}{C_1} + \frac{1}{sR_{\rm eq}C_1}\right) A^{-1}(s)\right]^{-1}, \quad (1)$$

where

$$A(s) = \frac{g_{\rm mo}r_{\rm o}}{1 + sr_{\rm o}C_{\rm o}} = \frac{A_{\rm o}}{1 + s(2\pi f_{\rm OL})^{-1}}. \quad (2)$$

$R_{\rm eq}$ is the equivalent resistor of the subthreshold biased PMOS transistors M1 and M2 in Fig. 1(a). $A(s)$ is the transfer function of an ideal single-pole operational transconductance amplifier (OTA) in Fig. 1(b) with open-loop midband gain $A_{\rm o}$ and pole at $f_{\rm OL}$. $g_{\rm mo}$ is the transconductance of OTA. $r_{\rm o}$ and $C_{\rm o}$ are individually the output impedance and capacitor. $C_{\rm o}$ consists of transistor's parasitic capacitor $C_{\rm P}$ and load capacitor $C_{\rm L}$.

The capacitive feedback formed by C_1 and C_2 sets the midband gain of the preamplifier $A_{\rm p}$ to approximately C_1/C_2. In this paper, the value of the preamplifier's close-loop gain $A_{\rm p}$ is set to 10 (20 dB). Using capacitive feedback is advantageous because high-value capacitors can be realized easily in the standard CMOS process and draw no DC voltage gain. MOSFET pseudo-resistor element (M1, M2) provides the DC feedback path for the input-stage of the OTA and forms a highpass pole $f_{\rm HP}$ with the feedback capacitor C_2.

From Eq. (1), the lower cut-off frequency ($f_{\rm HP}$) of the preamplifier is expressed as

$$f_{\rm HP} = \frac{1}{(2\pi A_{\rm o}R_{\rm eq}C_2 + R_{\rm eq}C_1 + R_{\rm eq}C_2)} \approx \frac{1}{2\pi A_{\rm o}R_{\rm eq}C_2}. \quad (3)$$

Thus, the low-frequency corner of preamplifier's passband can be configured for either recording the action or field potentials by adjusting the gate voltage of pseudo-resistor element.

The upper cut-off frequency (–3 dB lowpass pole) of the preamplifier $f_{\rm LP}$ is approximately equal to its bandwidth, which is the product of OTA's intrinsic cut-off frequency and the ratio of OTA's open-loop gain to the preamplifier's closed-loop gain. $f_{\rm LP}$ is given by

$$f_{\rm LP} = \frac{A_{\rm o}}{A_{\rm p}} f_{\rm OL} = \frac{g_{\rm mo}C_2}{2\pi C_1 C_{\rm o}}. \quad (4)$$

For a given closed-loop gain, the upper cut-off frequency is determined by the OTA's transconductance $g_{\rm mo}$ and output capacitor $C_{\rm o}$.

The OTA is a typical telescopic fully-differential operational amplifier with a PMOS differential pair input M3–M4.

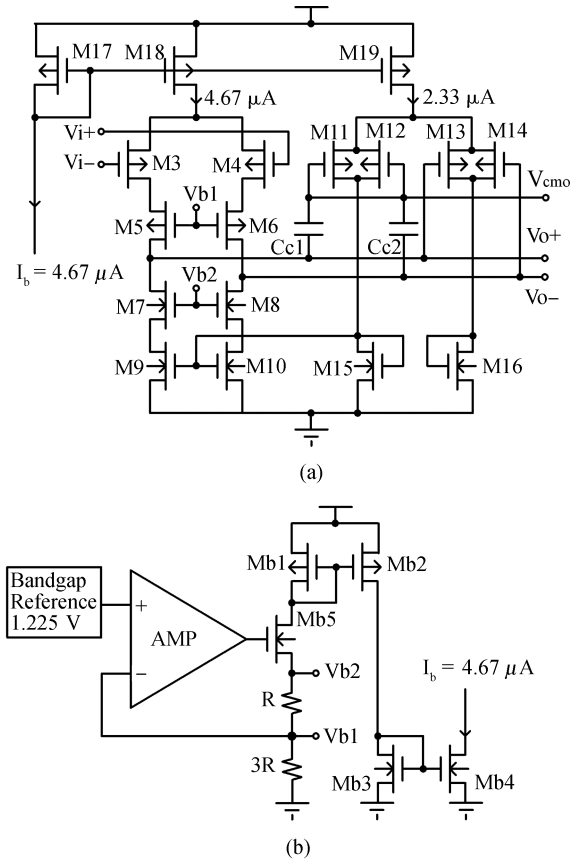

Fig. 2. (a) Schematic of OTA. (b) Schematic of biasing circuitry.

This type of OTA has the characteristics of high open-loop gain and low power dissipation. However, the fully-differential OTA has a limited output swing, and requires an additional circuitry for common-mode feedback (CMFB). Because the neural signals captured by implanted mirco-electrodes are usually weaker than 500 μV, a relatively medium dynamic range can meet our requirements. The CMFB circuitry provides an accurate common-mode output level, so the preamplifier's output signal can be directly amplified by the second-stage through the DC couple. Therefore, a carefully designed CMFB circuitry is highly required by the fully-integrated system, though it occupies more chip-area and consumes extra power.

In the telescopic operational amplifier of Fig. 2(a), the transconductance of four transistors pairs M3–M10 is denoted as $g_{\rm m3,\,4}$, $g_{\rm m5,\,6}$, $g_{\rm m7,\,8}$, $g_{\rm m9,\,10}$, and the channel resistance is $r_{3,\,4}$, $r_{5,\,6}$, $r_{7,\,8}$, $r_{9,\,10}$. The CMFB circuitry consisting of M13–M16 senses the output common-mode levels of the two outputs and accordingly adjusts the bias voltages of M9 and M10. The open-loop gain of OTA can be expressed as

$$A = -(g_{\rm m3,\,4} + g_{\rm mb3,\,4})(r_{\rm p}//r_{\rm n}), \quad (5)$$

where

$$r_{\rm p} = r_{3,\,4} + r_{5,\,6} + r_{3,\,4}r_{5,\,6}(g_{\rm m5,\,6} + g_{\rm mb5,\,6}), \quad (6)$$

$$r_{\rm n} = r_{7,\,8} + r_{9,\,10} + r_{7,\,8}r_{9,\,10}(g_{\rm m7,\,8} + g_{\rm mb7,\,8}). \quad (7)$$

The impedance seen at the output net $r_{\rm p}$ //$r_{\rm n}$ is quite large, because of the cascode structure. Thus, if the OTA's input transistors have large value of transconductance, a high open-loop

gain will be achieved. The simulation result shows that our OTA's open-loop gain is about 82 dB.

A bandgap reference circuitry is also designed for providing the biasing voltage V_{b1}, V_{b2} and current I_b, as is shown in Fig. 2(b). By carefully setting the values of V_{b1}, V_{b2} and I_b, the input transistors M3 and M4 are made to operate in a weak inversion region, while M5–M10 are in a strong inversion region. The preamplifier's input and output common voltages are also generated by this circuitry.

3. Noise analysis

For noise analyzing, we build a single-ended equivalent model in Fig. 3, which has the same noise characteristic as our fully-differential preamplifier. There are two main noise sources, the pseudo-resistor element R_{eq} and the OTA. Most reported papers concentrate on analyzing the noise from the OTA, but the noise of the pseudo-resistor is rarely noticed[5−13, 15, 16].

We take the pseudo-resistor element as a passive device, and only consider its thermal noise. Because the thermal noise source R_{eq}, the preamplifier's input capacitor C_1 and OTA's input capacitor C_{in} is in parallel, the noise spectrum density of R_{eq} contributed component seen at the input net of OTA can be described as

$$\overline{v^2_{ni,\,R'}} = \frac{4KTR_{eq}}{4\pi^2 R^2_{eq}(C_1 + C_{in})^2 f^2 + 1}. \tag{8}$$

Integrating $\overline{v^2_{ni,\,R'}}$ from the lower cut-off frequency f_{HP} to the upper f_{LP}, yields the input-referred noise power of R_{eq} contributed component.

$$\begin{aligned} E[\overline{v^2_{ni,\,R'}}] &= \int_B \frac{4KTR_{eq}}{4\pi^2 R^2_{eq}(C_1 + C_{in})^2 f^2 + 1} \mathrm{d}f \\ &\approx \frac{2KT}{\pi(C_1 + C_{in})}(\tan^{-1} f_{LP} - \tan^{-1} f_{HP}). \end{aligned} \tag{9}$$

Thermal noise current spectrum density of the input transistors M3–M4 and M9–M10 are denoted as $\overline{i^2_{n3,\,4\_th}}$ and $\overline{i^2_{n9,\,10\_th}}$ respectively. The input-referred thermal noise spectrum density of OTA is given by

$$\begin{aligned} \overline{v^2_{ni,\,OTA\_th'}} &= \frac{\overline{i^2_{n3,\,4\_th'}} + \overline{i^2_{n9,\,10\_th'}}}{(g_{m3,\,4} + g_{mb3,\,4})^2} \\ &\approx 4KT\gamma\Big(\frac{1}{g_{m3,\,4}} + \frac{g_{m9,\,10}}{g^2_{m3,\,4}}\Big), \end{aligned} \tag{10}$$

where γ is constant with the value of 2/3[17]. To achieve a low thermal noise, we should maximize $g_{m3,\,4}$ and minimize $g_{m9,\,10}$. Therefore, in our circuit, $1/g_{m3,\,4} \gg g_{m9,\,10}/g^2_{m3,\,4}$, and the input-referred thermal noise spectrum density of OTA is reduced to

$$\overline{v^2_{ni,\,OTA\_th'}} = \frac{4KT\gamma}{g_{m3,\,4}}. \tag{11}$$

The input-referred $1/f$ noise spectrum density of OTA is

$$\begin{aligned} \overline{v^2_{ni,\,OTA\_1/f'}} &= \frac{\overline{i^2_{n3,\,4\_1/f'}} + \overline{i^2_{n9,\,10\_1/f'}}}{(g_{m3,\,4} + g_{mb3,\,4})^2} \\ &\approx \frac{1}{C_{OX}}\Big(\frac{K_{b\_sub} I^2_{ds}}{W_{3,\,4}L_{3,\,4}g^2_{m3,\,4}} + \frac{K_{b\_sat} I_{ds}}{L^2_{9,\,10}g^2_{m3,\,4}}\Big)\frac{1}{f}, \end{aligned} \tag{12}$$

where K_{b_sub} is the process-dependent parameter of a PMOS transistor operating in the subthreshold region, and K_{b_sat} is the parameter of a NMOS transistor operating in the saturate region[18].

$\overline{v^2_{ni,\,OTA\_1/f'}}$ is inversely proportional to the gate area of transistors M3, M4, and the channel length of M9, M10. In our design, the length and width of M3, M4 and the length of M9, M10 are set to large values for lower $1/f$ noise. However, we cannot make the sizes of these transistors as much as is possible, partly because of the area limitation and stability requirement. Additionally, an over-large gate area of input transistors may increase the preamplifier's overall noise. A global optimization design will be required.

If $(K_{f\_sub} I^2_{ds})/(W_{3,\,4}L_{3,\,4}g^2_{m3,\,4}) \gg (K_{f\_sat} I_{ds})/(L^2_{9,\,10}g^2_{m3,\,4})$, only considering the noise of the input stage, the expression for input-referred $1/f$ noise spectrum density of OTA can be reduced to

$$\overline{v^2_{ni,\,OTA\_1/f'}} \approx \frac{K_{b\_sub} I^2_{ds}}{C_{OX}W_{3,\,4}L_{3,\,4}g^2_{m3,\,4}f}. \tag{13}$$

Combining the OTA's thermal noise equation (11) and its $1/f$ noise equation (13), the input-referred noise power of OTA contributed component can be expressed as

$$\begin{aligned} E\big[\overline{v^2_{ni,\,OTA'}}\big] &= E\big[\overline{v^2_{ni,\,OTA\_th'}}\big] + E\big[\overline{v^2_{ni,\,OTA\_1/f'}}\big] \\ &= \frac{4KT\gamma}{g_{m3,\,4}} f_{LP} + \frac{\lambda K_{b\_sub} I^2_{ds}}{C_{in}g^2_{m3,\,4}} \ln\frac{f_{LP}}{f_{HP}}, \end{aligned} \tag{14}$$

where

$$C_{in} \approx C_{gs} \approx \lambda C_{OX} W_{3,\,4}L_{3,\,4}. \tag{15}$$

λ is related to the inversion depth of MOSFET[19]. The input parasitic capacitance C_{in} is approximately equal to the gate capacitance of input transistors M3–M4. Therefore, if M3 and M4 are biased in sub-threshold region, C_{in} can be expressed as Eq. (15). From Eqs. (9) and (14), any increase in C_{in} decreases the input-referred noise power of R_{eq} and OTA. However, the overall noise power of preamplifier is also related to the noise of OTA and R_{eq}.

$$E[\overline{v^2_{ni,\,AMP}}] = 2\left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 E[\overline{v^2_{ni,\,OTA'}}] + E[\overline{v^2_{ni,\,R'}}]. \tag{16}$$

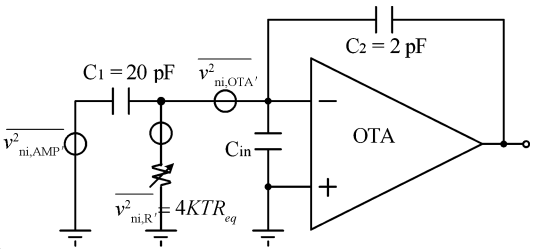

Fig. 3. Single-ended equivalent model of the preamplifier for noise analyzing.

An optimum input capacitor C_{in} can be found to minimize the total noise of preamplifier. We can choose an optimum size of input differential-pair transistors M3, M4 and make M3, M4 biased in deep weak inversion regime.

4. Low power design

Low power dissipation is one of the critical requirements for implantable neural recording applications. In order to reduce the power consumption and optimize the noise performance, the input transistors of OTA (M3, M4) are made to operate in a weak inversion region. Therefore, we use the EKV model to analyze the operating condition of these transistors[6, 20], which is valid in both the weak and strong regions of inversion. The transconductance of the input transistors can be expressed as

$$g_{\mathrm{m}} \approx \frac{\kappa I_{\mathrm{ds}}}{v_{\mathrm{t}}} \frac{2}{1+\sqrt{1+4I_{\mathrm{ds}}/I_{\mathrm{S}}}}, \tag{17}$$

where

$$I_{\mathrm{S}} = \frac{\mu C_{\mathrm{OX}} v_{\mathrm{t}}^2}{\kappa} \frac{W}{L}, \tag{18}$$

in which κ is the subthreshold gate coupling coefficient, having a typical value of 0.7. In deep weak inversion, a low biasing current I_{ds} can force g_{m} to reach its maximum value of $\kappa I_{\mathrm{ds}}/v_{\mathrm{t}}$, while $E[\overline{v_{\mathrm{ni,\ OTA'\_th}}^2}]$ in Eq. (14) will reduce to

$$\mathrm{Min}(E[\overline{v_{\mathrm{ni,\ OTA\_th'}}^2}]) = \frac{4KT\gamma}{g_{\mathrm{m,\ max}}} f_{\mathrm{LP}} = \frac{4KT\gamma v_{\mathrm{t}}}{\kappa I_{\mathrm{ds,\ min}}} f_{\mathrm{LP}}, \tag{19}$$

where $I_{\mathrm{ds,min}}$ is the minimum drain current of single input transistor (M3 or M4 in Fig. 2(a)), which is expressed as

$$I_{\mathrm{ds,\ min}} = \frac{4KT\gamma v_t}{\kappa} \frac{f_{\mathrm{LP}}}{\mathrm{Min}(E[\overline{v_{\mathrm{ni,\ OTA\_th'}}^2}])}. \tag{20}$$

From Eq. (20), we can get a theoretical limit of the drain current through one input transistor with a specific noise and bandwidth requirement. For example, if the frequency of neural signals is high to 7 kHz with a required OTA's thermal noise level of 1 μVrms, the theoretical minimum I_{ds} is computed to be about 0.36 μA. Frankly, using the applied 0.35 μm CMOS manufacturing process, it seems impossible to get the bandwidth of integrated preamplifiers to reach 7 kHz with a 0.36 μA bias current I_{ds}. Anyway, Equation (20) exhibits the end-point for the low-power design of integrated preamplifiers with the widely used topology of capacitive-coupled and capacitive-feedback. In this paper, we set the I_{ds} of 2.33 μA to reach a 6.7 kHz bandwidth when the input transistors operate in the weak inversion region.

5. Chip measurements

The proposed circuit has been designed and fabricated using a standard 2P4M CMOS process of 0.35 μm. This chip occupies 0.22 mm^2 (without pads), which dominated by the preamplifier's two input capacitors and input transistors. Figure 4 shows the microphotograph of the prototype chip. The measurement results below are obtained from a 3.3 V power supply.

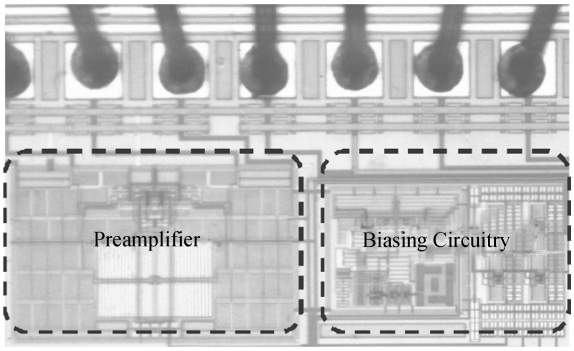

Fig. 4. Microphotograph of the proposed chip

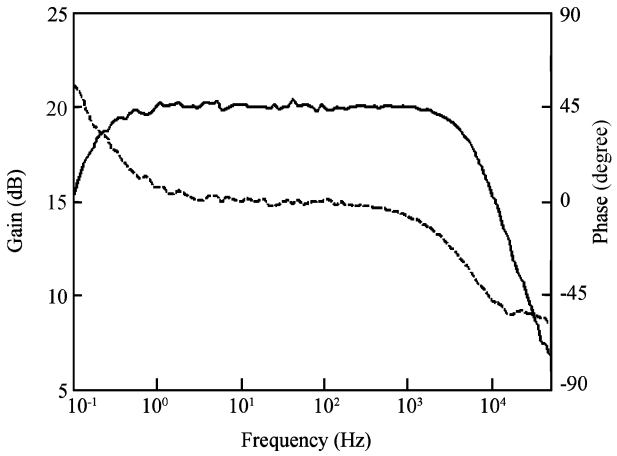

Fig. 5. Measured frequency response.

The resistance of the subthreshold biased M1 and M2 are measured with 50 mV drain-source voltage. The value of the equivalent resistance can be accurately configured in the range of 10^6–10^{11} Ω by controlling the gate voltage V_{t}.

We designed the preamplifier for a closed-loop gain of 20 dB, and the experimental results show a mid-band gain of approximately 20.4 dB. The lower cut-off frequency of the preamplifier is controlled by the gate voltage V_{t} of the pseudo-resistor element. Figure 5 shows the frequency response of the preamplifier. The lower corner is 0.15 Hz when V_{t} is set to 1.35 V for recording the local field potentials (LFPs) and the mixed neural spikes. The measured upper cut-off frequency is 6.7 kHz with a 7 μA bias current. In Ref. [6], the power consumption of the additional biasing circuit is not included in the power measurements since the biasing circuit can be shared by an arbitrary number of preamplifiers. We adopt this method, and only consider the power consumption of OTA and CMFB module, which is measured to be 23.1 μW.

The input-referred noise is calculated from measured output noise spectrum divided by the measured gain-frequency function, as shown in Fig. 6. The preamplifier has an input-referred noise of 8.2 μVrms integrated from 0.15 Hz to 6.7 kHz. The typical background noise is 5–10 μV for the extracellular neural recording applications, and the bio-amplifier's noise lower than typical noise level is hardly noticed. Thus, the small-amplitude neural spikes as weak as twenty microvolts can be captured by our preamplifier. The 1% total harmonic distortion (THD) at 1 kHz is measured to be 5 mV, which re-

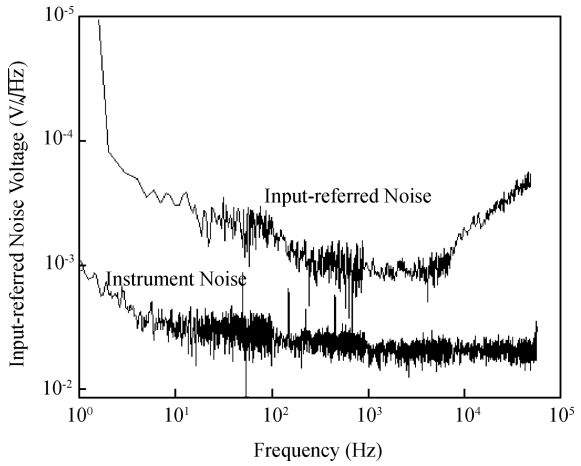

Fig. 6. Measured input-referred voltage noise spectra.

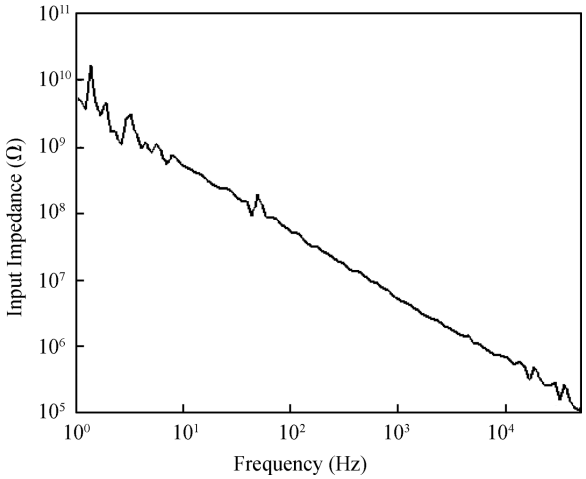

Fig. 7. Measured input impedance of the preamplifier.

sults in a 47 dB dynamic range.

The measured input impedance of the preamplifier is shown in Fig. 7. The value of impedance at 1 kHz is about 5 MΩ, which only results in no more than 10% signal attenuation with a 0.5 MΩ silicon-based neural electrode.

Figure 8 shows the preamplifier's output signals in response to a pre-recorded spikes train from the somatosensory cortex of a Wistar rat. The in-vitro test is performed in the saline environment. Pre-recorded signals train is applied to saline and amplified by our preamplifier through a silicon-based neural electrode. The output signals of our preamplifier are recorded by a 24-bit dynamic data acquisition (DAQ) instrument with 32 kSps. Due to the relatively high electrode impedance, the amplitude of the amplified spikes is lower than 10 times input.

6. Conclusion

A fully-differential preamplifier with capacitive-couple and capacitive-feedback topology has been designed and manufactured in a 0.35-μm CMOS process for neural recording applications. The preamplifier has a bandwidth of 6.7 kHz with a 20.4 dB midband gain, and its lower cut-off frequency can be adjusted from sub-Hertz to hundreds-Hertz by controlling the gate voltage of the pseudo-resistor element. Input-referred rms noise voltage is measured to be 8.2 μVrms (0.15 Hz–6.7 kHz). The in-vitro test of amplifying the pre-recorded neural signals demonstrates the functionality of our preamplifier. Due to the properties of fully-difference and fully-integration, it will be possible to reproduce the preamplifier in the same die and be integrated with the multi-channel microelectrodes arrays with the capability of recording a large number of neurons simultaneously.

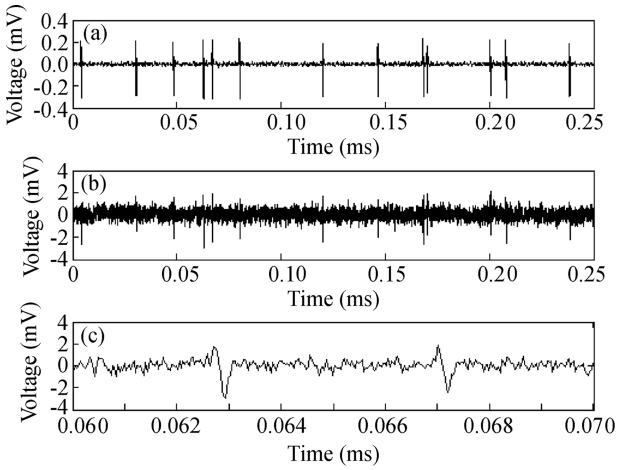

Fig. 8. Measured responses to pre-recorded Wistar rats' cortical spikes. (a) Input signal train. (b) Output signal train. (c) Output spike signals.

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