A dual VCDL DLL based gate driver for zero-voltage-switching DC–DC converter*

Tian Xin(田鑫), Liu Xiangxin(刘祥昕), and Li Wenhong(李文宏)†

(State Key Laboratory of ASIC & System, Fudan University, Shanghai 201203, China)

Abstract: This paper presents a dual voltage-controlled-delay-line (VCDL) delay-lock-loop (DLL) based gate driver for a zero-voltage-switching (ZVS) DC–DC converter. Using the delay difference of two VCDLs for the dead time control, the dual VCDL DLL is able to implement ZVS control with high accuracy while keeping good linearity performance of the DLL and low power consumption. The design is implemented in the CSM 2P4M 0.35 μm CMOS process. The measurement results indicate that an efficiency improvement of 2%–4% is achieved over the load current range from 100 to 600 mA at 4 MHz switching frequency with 3.3 V input and 1.3 V output voltage.

Key words: voltage-control-delay-line; delay-lock-loop; delay-unit; zero-voltage-switching; pseudo-current-control-inverter

DOI: 10.1088/1674-4926/31/7/075012 **EEACC:** 1280; 2560; 2570D

1. Introduction

The synchronous rectifier buck converters are at present widely used in battery-powered portable devices owing to their ability to achieve high efficiency under low voltage conditions. The power stage of the synchronous rectifier buck converter is shown in Fig. 1 with shade, where L and C are respectively the inductor and capacitor of output filter of the buck converter, V_{PM} is the driving signal of power PMOSFET (PM), V_{NM} is the driving signal of power NMOSFET (NM), V_{SW} is the drain voltage of NM, C_{SW} is the parasitic capacitor at V_{SW}, and D_1 is the parasitic diode of NM. Two input bypass capacitors C_{i1} and C_{i2} are generally used to provide a pulsating input current. In order to avoid a shortcut path from V_{DD} to ground, an interval named dead time should be inserted into V_{PM} and V_{NM}. On account of process and temperature variations, the dead time should be set long enough, usually more than 10 ns[1]. During this period of time, both PM and NM are turned off, and V_{SW} will be pulled below –0.7 V to turn on D_1 to conduct the inductor current, which introduces a great power loss. This power loss is proportional to the switching frequency and the turning on duration of D_1. If NM is turned on simultaneously when V_{SW} reaches 0 V, the dead time reaches an optimal value t_{dopt}, this part of the power loss can be minimized, and this is the case of ZVS[2].

When PM is turned off, V_{SW} is very close to V_{DD}, and V_{SW} is discharged by the inductor current which can be seen as constant during such a short time. Since the inductor current is roughly equal to the load current I_0, t_{dopt} is load dependent. The range of t_{dopt} is normally from several to tens of nanoseconds.

Various techniques have been reported to control the dead time in recent years. In Ref. [3] V_{SW} is feedback to control V_{NM} to adjust the dead time in real time, but the delay from V_{SW} to V_{NM} restricts the minimization of power loss on the diode. A current sensor based circuit is proposed in Ref. [4] to implement ZVS control, however, the resolution of current sensor limits the dead time resolution, and a complicated calibration process is required. DLL is a better solution for ZVS control due to its high accuracy and insensitivity to process and temperature variations. A DLL based gate driver has been presented in Ref. [5], but it exploited a comparator which consumes static power as VCDL. For low power consideration, it is more appropriate to use a pseudo-current-control-inverter (PCCI), which only consumes dynamic power, as the delay-unit (DU) of VCDL. However, PCCI has a poor linearity when its delay varies several times. Therefore, this paper presents a dual VCDL DLL gate driver which settles down the linearity issue of PCCI for ZVS control. In Section 2, the principle and architecture of the proposed gate driver is described. Section 3 illustrates the circuit implementation. The experiment result is shown in Section 4. Finally, the conclusion is given in Section 5.

2. Architecture of the proposed dual VCDL DLL based gate driver

The architecture of the proposed dual VCDL DLL gate driver for ZVS DC–DC converters is shown in Fig. 2 with shade. It consists of a start-up circuit, a phase detector & charge pump (PD&CP), a transconductor, two VCDLs, a buffer, two

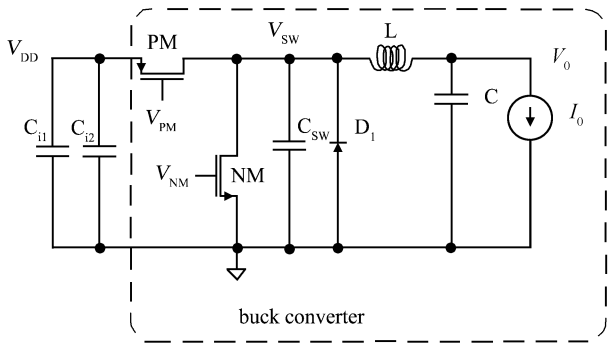

Fig. 1. The synchronous rectifier buck converter.

* Project supported by the National Natural Science Foundation of China (No. 60676013).

† Corresponding author. Email: wenhongli@fudan.edu.cn

Received 16 October 2009, revised manuscript received 11 February 2010

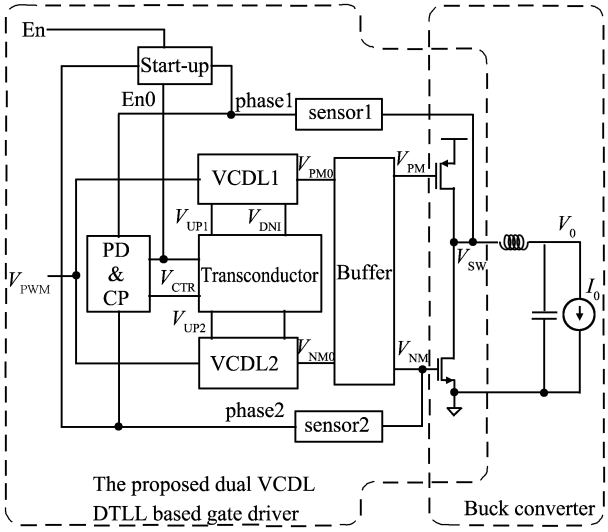

Fig. 2. Architecture of the dual VCDL DLL based gate driver.

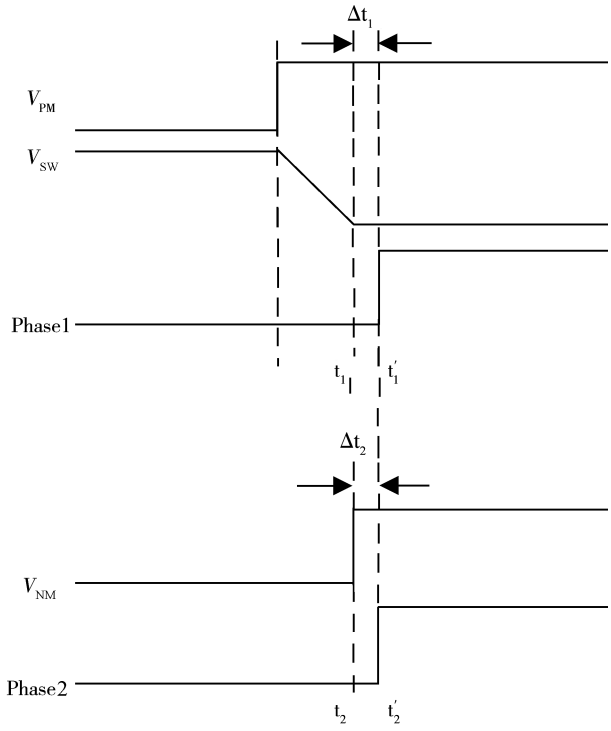

Fig. 3. Waveforms of V_{SW},V_{NM}, phase1 and phase2 in steady state.

sensors and parts of buck DC–DC. V_{PWM} is the output signal of the pulse width modulation (PWM) controller, and V_{NM0} and V_{PM0} are signals delayed from V_{PWM}. The buffer including logics and two scaled inverter chains strengthens the driven capacities of V_{PM0} and V_{NM0}. Sensor1 and sensor2 sense the falling edge of V_{SW} and the rising edge of V_{NM} respectively, and send their output signal phase1 and phase2 into the PD&CP.

Functioning like a delay-lock-loop, DLL is also able to synchronize its two input signal phase1 and phase2, which means $t_1' = t_2'$ in Fig. 3. If the delay of sensor1 (Δt_1) and sensor2 (Δt_2) can be matched carefully, then $t_1 = t_2$ and the ZVS control is realized.

As mentioned in Section 1, the PCCI can be a candidate of DU of VCDL, however, it suffers linearity problem. The circuit of PCCI is shown in Fig. 4(a)[6]. The delay of PCCI is inversely proportional to its control current I_{CTR}. And since the transconductor linearly converts the control voltage to current, the delay of VCDL is consequently inversely proportional to the control voltage, which can be given by:

$$t_d = \frac{K_1}{I_{CTR}} = \frac{K_1}{I_{CTR0} + \hat{I}_{CTR}} = \frac{K_1}{I_{CTR0} + g_m(V_{CTR} - V_0)}, \tag{1}$$

where K_1 is a constant, g_m is the transconductance of the transconductor, V_{CTR} is the control voltage, V_0 is the DC operating point of the transconductor, I_{CTR} is the control current while I_{CTR0} is its DC part and I_{CTR} which equals $g_m(V_{CTR}-V_0)$ is its AC part. The relationship between t_d and V_{CTR} is illustrated in Fig. 4(b) with V_0 and $\max(|\hat{I}_{CTR}|) = 0.5I_{CTR0} \cdot V_{CTR}$ has been normalized to I_{CTR0}/g_m and t_d to K_1/I_{CTR0}. From Fig. 4(b), it can be seen that it has been difficult for PCCI to keep good linearity when t_d varies only three times. Since the rest blocks are all linear circuits, the linearity of the whole closed loop system is poor. It leads to inconstancy of loop gain of DLL. In detail, the loop gain increases with t_d. Too high a loop gain leads to the instability of DLL, but too low loop gain deteriorates the locking speed of DLL. To insure the stability of DLL when t_d is big and keep locking speed high when t_d is small, this paper proposes a dual VCDL architecture to improve the linearity of DLL.

Instead of single VCDL, the proposed DLL uses two VCDLs. The transconductor converts V_{CTR} into two differential currents to control VCDL1 and VCDL2, and t_d is now the delay difference of VCDL1 and VCDL2, which can be expressed as

$$\begin{aligned} t_d &= \frac{K_1}{I_{CTR0} + g_m(V_{CTR} - V_0)} - \frac{K_2}{I_{CTR0} - g_m(V_{CTR} - V_0)} \\ &= \frac{(K_1 - K_2)I_{CTR0} - (K_1 + K_2)g_m(V_{CTR} - V_0)}{I_{CTR0}^2 - g_m(V_{CTR} - V_0)^2}. \end{aligned} \tag{2}$$

The DC value of t_d can be adjusted by setting K_1 and K_2 by adopting different numbers of DUs of VCDL1 and VCDL2. When $K_1 = K_2$, Equation (2) can be simplified to:

$$t_d = \frac{-2K_1 g_m(V_{CTR} - V_0)}{I_{CTR0}^2 - g_m(V_{CTR} - V_0)^2}. \tag{3}$$

Having the same condition that $\max(|\hat{I}_{CTR}|) = 0.5I_{CTR0}$, the linearity of Eq. (4) is much better than Eq. (2). Simulated t_d–V_{CTR} curves of single VCDL and dual VCDL are given in Fig. 5. Here we set $K_1 = K_2$, V_{CTR} changes from 1.2 to 2.2 V, $V_0 = 1.7$ V and g_m at a proper value that $\max(|\hat{I}_{CTR}|) = 0.5I_{CTR0}$. From the simulation results, it is obvious that the slope of t_d–V_{CTR} curve of single VCDL changes greatly when t_d varies from 5 to 14 ns. By contrast, the slope of t_d–V_{CTR} curve of dual VCDL is nearly constant as t_d changes from 0 to 8 ns, and the linearity is kept till the condition that $\max(|\hat{I}_{CTR}|) = 0.5I_{CTR0}$ unchanged. If a greater max (t_d) is needed, we merely need to increase the number of DUs of each VCDL. In Fig. 6(b), t_d could be negative because it is the delay difference of VCDL1 and VCDL2 and the number of DUs of VCDL1 and VCDL2 are set to be equal.

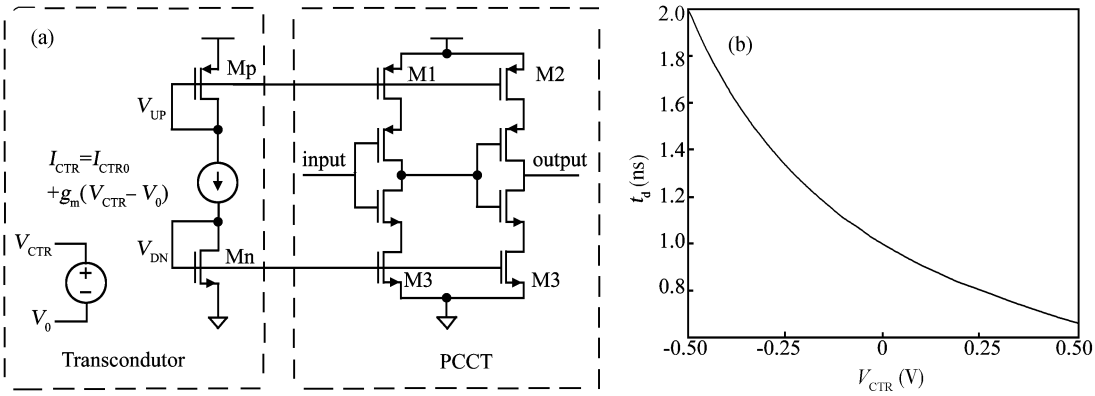

Fig. 4. (a) Circuit of PCCI. (b) Simulation curve of t_d–V_{CTR}.

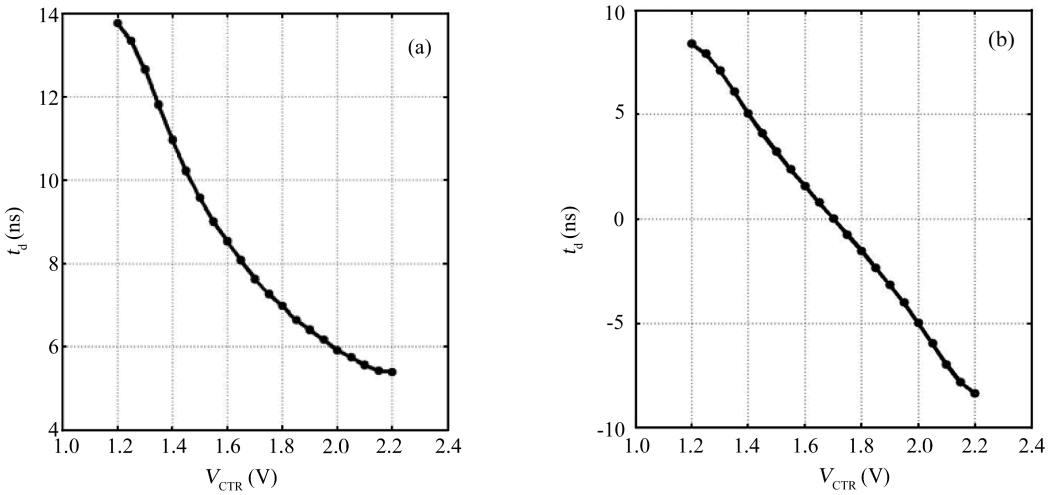

Fig. 5. (a) t_d–V_{CTR} curve of single VCDL. (b) t_d–V_{CTR} curve of dual VCDL.

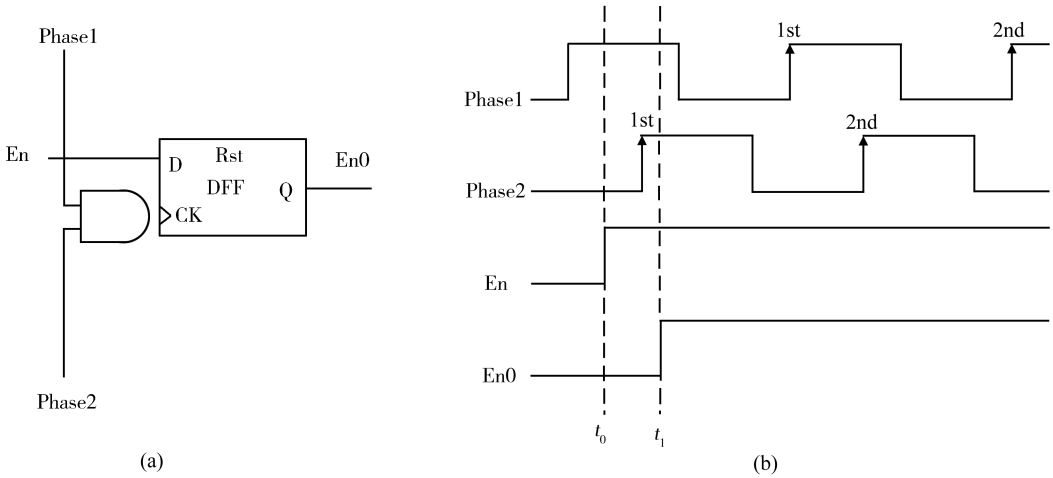

Fig. 6. (a) Start-up circuit. (b) Start-up process.

3. Circuit implementation

3.1. Start-up circuit

The start-up circuit is shown in Fig. 6(a), which is used for three reasons as follows.

(1) The analog circuits can operate correctly only when reference current and reference voltage have been stable so DLL should start to work some time after power on.

(2) The gate driver should be able to shift between fixed dead time control mode and ZVS control mode for comparison.

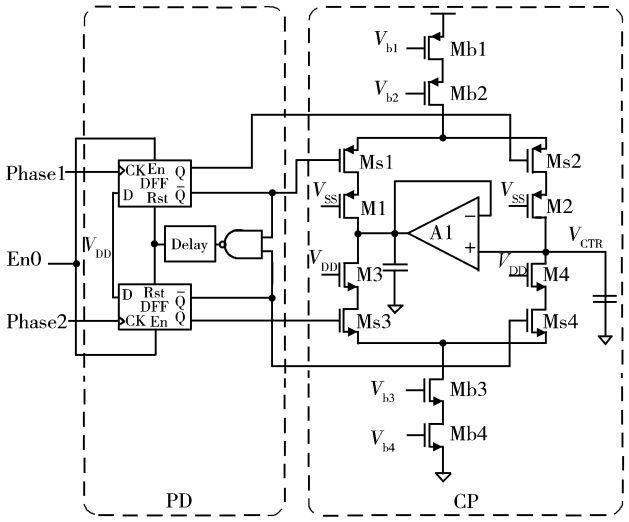

Fig. 7. Circuit of PD & CP.

When En is '0', the DLL is turned off and unable to lock the loop, and t_d holds on a certain value

(3) To ensure PD start up correctly: In Fig. 6(b), phase1 should have a leading phase to phase2, but if PD start to work at t_0 when phase1 is '1' and phase2 is '0', PD would meet the rising edge of phase2 first and after that meet the rising edge of phase1, as a result PD would wrongly judge that phase2 has a leading phase to phase1. If PD starts to work at t_1 when both phase1 and phase2 are '1', this mistake can be avoided. The proposed start-up circuit is able to delay the rising edge of En right after both phase1 and phase2 becoming '1' as shown in Fig. 6(b), and the delayed signal is En0.

3.2. PD&CP

The circuit of PD&CP is shown in Fig. 7. A DFF based PD is proposed in this design. To eliminate the charge sharing issues which cause a large steady state error[7], a redundant current path including Ms1, M1, M3, Ms3, and an amplifier A1 are added into the traditional CP[8]. M1, M2, M3 and M4 are used to alleviate the clock feed through problem and further reduce the steady state error. When EN0 is '0', the switching actions of DFFs in PD are stopped, and as a result V_{CTR} should hold on a certain value.

3.3. Transconductor

Figure 8(a) shows the circuit of transconductor. Instead of resistors, two NMOS M1 and M2, which have advantage in size over resistors, are used to extend the linear input range[9]. I_{b1} and I_{b4} are added into the drain of Mp1 and Mp2 to avoid the current being "pump out". I_{CTR1} and I_{CTR2} are the control currents of VCDLs. The relationship between I_{CTR1}, I_{CTR2} and V_{CTR} is roughly illustrated in Fig. 8(b). In this design, I_{b1}, I_{b2}, I_{b3} and I_{b4} are set to be equal, as a result, when $V_{CTR} = V_{DD}/2$, we have $I_{CTR1} = I_{CTR2} = I_{CTR0} = 2I_{b1}$, and as V_{CTR} changes, I_{CTR1} and I_{CTR2} vary from $0.51I_{CTR0}$ to $1.5I_{CTR0}$, equivalently that $\max(|\hat{I}_{CTR1}|) = \max(|\hat{I}_{CTR2}|) = 0.5I_{CTR0}$. The working mode of transconductor can be set by the signal En0. When En0 is '1', the control currents are adjustable; when En0 is '0', V_{CTR} is pulled to 0 V to set the control current of VCDL2 at the minimum value and the control current of VCDL1 at the maximum value. As a result, t_d is fixed at the maximum value.

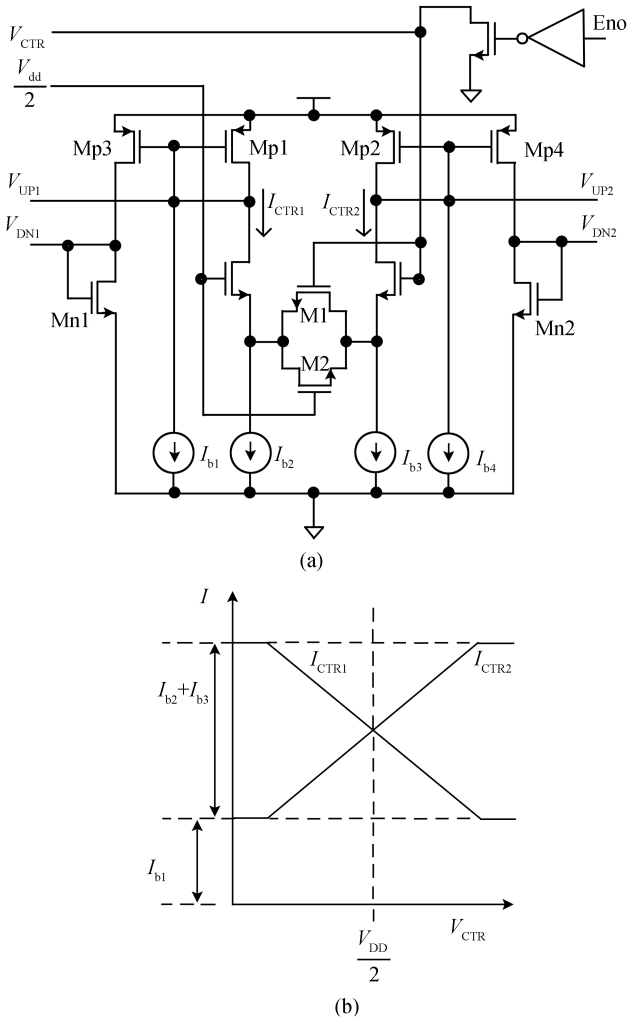

Fig. 8. (a) Circuit of transconductor. (b) Curves of I_{p1}–V_{CTR} and I_{p2}–V_{CTR} when $I_{b1} = I_{b2} = I_{b3} = I_{b4}$.

3.4. VCDL

The DU of VCDL has been shown in Fig. 4(a). The sizes of Mp and Mn should be well designed to keep the over-driven-voltages of M1, M2, M3 and M4 in the range from 0.2 to 0.8 V otherwise the delay of VCDL will change little with I_{CTR}. Both VCDL1 and VCDL2 PCCI chains contain 6 DUs, and the maximum t_d is about 15 ns.

3.5. Buffer

The circuit of the buffer is shown in Fig. 9(a). Since VCDLs vary their delay according to load current but are unable to vary the duty ratio of V_{PWA}, there is a variable interval between the falling edges of V_{PM0} and V_{NM0}. The falling edges of V_{NM0} and V_{PM0} are synchronized in stage 1 as shown in Fig. 9(b). Inverter chains in stage2 provide strong driven capacity and the logics force a minimum dead time about 1.5 ns for protection. Considering switching speed and power consumption, the scaled factors of inverter chains are both set to 8 : 1.

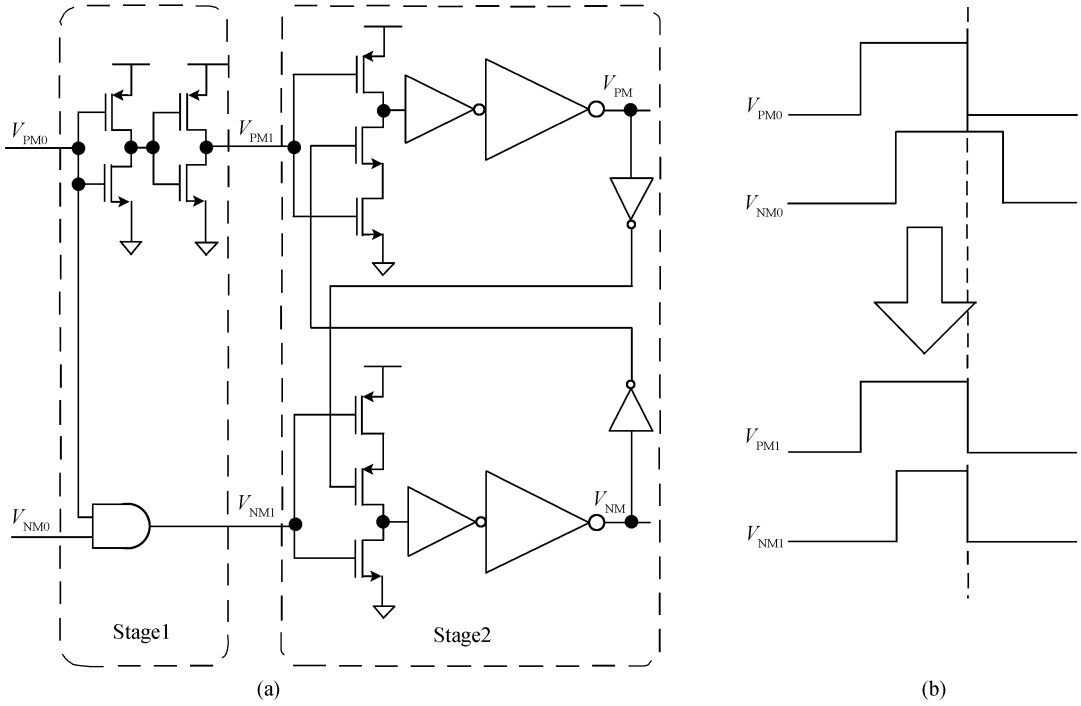

Fig. 9. (a) Circuit of buffer. (b) Waveforms of V_{PM0}, V_{NM0}, V_{PM1} and V_{NM1}.

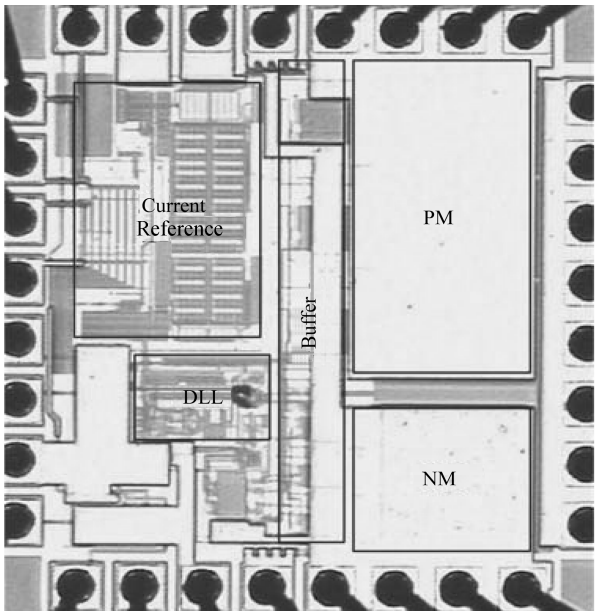

Fig. 10. Chip photo.

4. Experimental result

The design was implemented in the CSM 2P4M 0.35 μm CMOS process. The area is about 1×1 mm^2, and the chip photo is shown in Fig. 10. It consists of the proposed gate driver, PM, NM and an all-CMOS current reference. The sizes of PM and NM are 40 mm/0.5 μm and 15 mm/0.5 μm respectively. The current reference provides 2.3 μA reference current for analog circuits. Some parameters of off-chip components in Fig. 1 are listed in Table 1.

The chip has been tested at a 4 MHz switching frequency, 3.3 V input and 1.3 V output voltage over the load current range from 20 to 600 mA. Waveforms of some important nodes are shown in Fig. 11. Figure 11(a) shows the waveforms of V_{SW} and V_0. Figures 11(b) and 11(c) respectively show the waveform of V_{NM} and V_{SW} in fixed dead time control mode and ZVS control mode. In fixed dead time control mode, there is a 6 ns delay between V_{SW}'s falling edge andV_{NM}'s rising edge, however, in the ZVS control mode this delay is eliminated. The load currents in Figs. 11(b) and 11(c) is 20 mA and V_{SW} changes very slowly. Figure 11(d) shows V_{NM} and V_{SW} at 500 mA load current, and V_{SW} changes much faster. Figures 11(e) and 11(f) show V_{NM} and V_{PM} under ZVS control at load current 20 and 500 mA respectively. The optimal dead time is much longer in light load than in heavy load.

The power consumption of DLL and current reference is about 600 μW at 3.3 V power supply and the compared curves of efficiency versus load current between fixed dead time control and ZVS control are drawn together in Fig. 12. The efficiency can be improved 2%–4% over the load current range from 100 to 600 mA. Table 2 gives a performance comparison of the ZVS gate drivers. Among all of the drivers in Table 2, this work has a high precision and the lowest power consumption while maintains the peak efficiency of DC–DC about 89%.

5. Conclusion

A Dual VCDL DLL based gate driver for a ZVS DC–DC converter is implemented with high precision and low power. When the load current is below 100 mA, the efficiency improvement is limited because the current flow through the parasitic diode of NM D_1 is very small and the power loss on D_1 is very low; but as the load current increases, the power dissipation on D_1 grows up, and the ZVS technique can improve the efficiency by 2%–4% over the load current range from 100

Table 1. Parameters of off-chip components.

Component	C_{i1}	C_{i2}	C	L
Value	10 μF	0.22 μF	10 μF	1 μH
Remark	The first input bypass capacitor of buck converter	The second input bypass capacitor of buck converter	The capacitor of output filter of buck converter	The inductor of output filter of buck converter

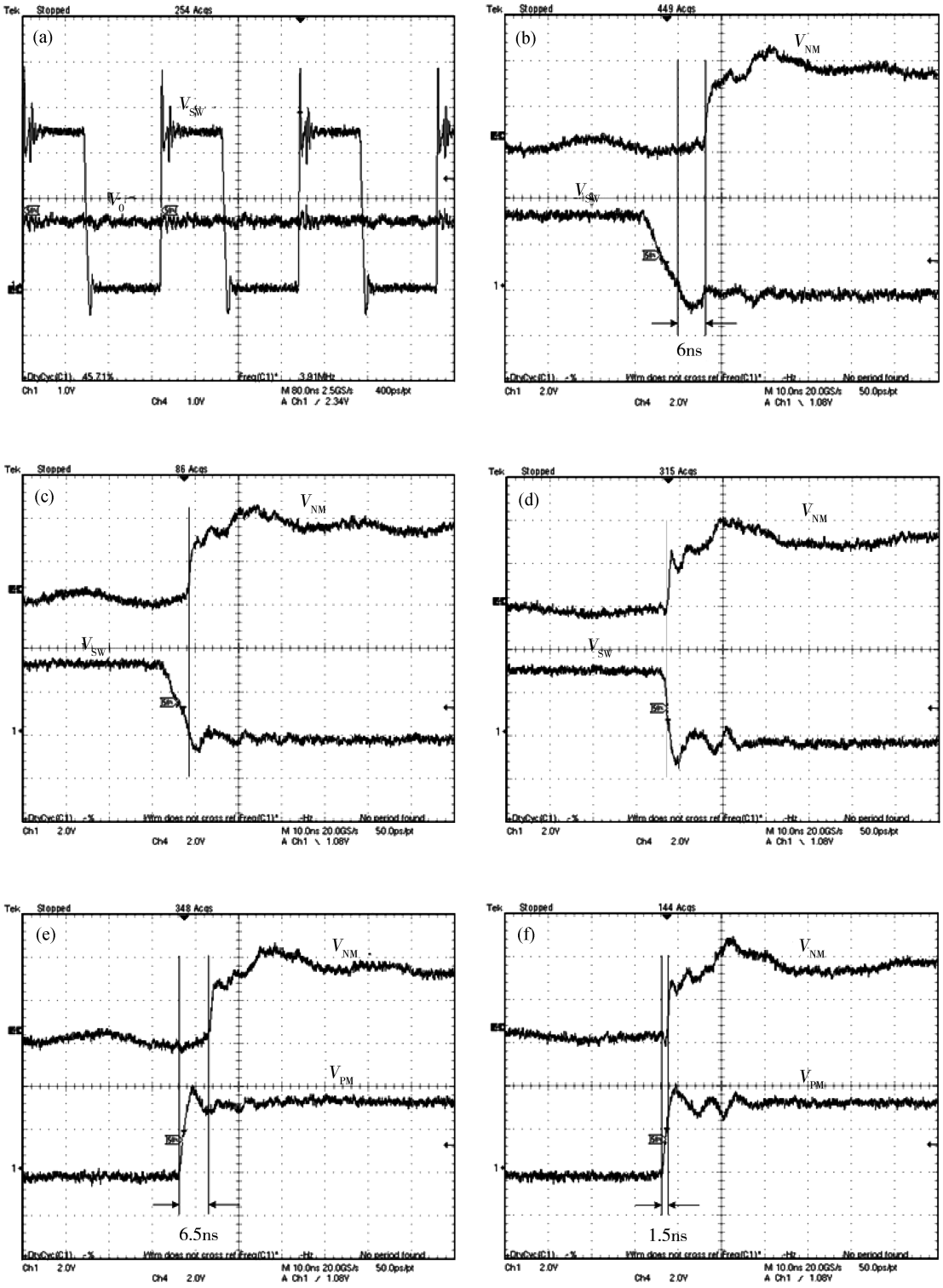

Fig. 11. (a) V_{SW} and V_0 under fixed dead time control mode at 20 mA load current. (b) V_{SW} and V_{NM} under fixed dead time control mode at 20 mA load current. (c) V_{SW} and V_{NM} under ZVS control mode at 20 mA load current. (d) V_{SW} and V_{NM} under ZVS control mode at 500 mA load current. (e) V_{PM} and V_{NM} under ZVS control mode at 20 mA load current. (f) V_{PM} and V_{NM} under ZVS control mode at 500 mA load current.

Table 2. Performance comparison of the ZVS gate drivers.

Parameter	Ref. [3]	Ref. [4]	Ref. [5]	This work
Year	2008	2007	2004	2009
Technology (μm)	0.18	0.35	0.18	0.35
Working voltage (V)	2.2	3.3	2	3.3
Maximum dead time (ns)	n/a	n/a	50	13
Precision	Error equals to signal delay	The same as current sensor	Static locking error of DLL	Static locking error of DLL
Output voltage of converter (V)	1	1.65	1	1.3
Switching frequency of converter (MHz)	660	1	5	4
Improved efficiency (%)	n/a	n/a	2–27	2–4
Peak efficiency (%)	31	95	82	89
Power consumption of ZVS controller (mW)	n/a	n/a	4.5	0.6

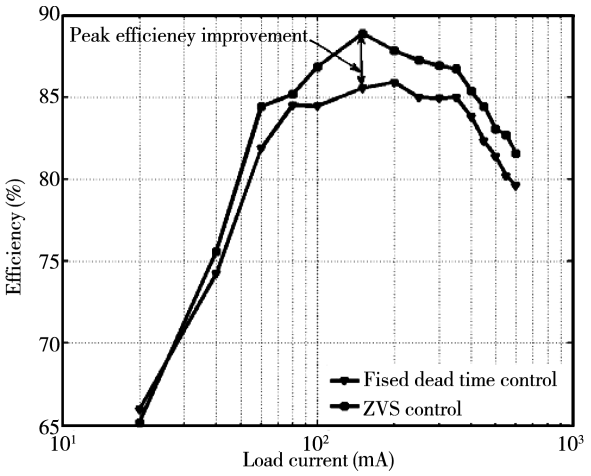

Fig. 12. Efficiency versus load current.

to 600 mA. A peak efficiency improvement occurs at 150 mA, as shown in Fig. 12.

References

[1] Liou W R, Yeh M L, Kuo Y L. A high efficiency dual-mode buck converter IC for portable applications. IEEE Trans Power Electron, 2008, 23(2): 667

[2] Stratakos A J. High-efficiency low-voltage DC–DC conversion for portable applications. Ann Arbor: UMI Company, 1999

[3] Alimadadi M, Sheikhaei S, Lemieux G, et al. A 660 MHz ZVS DC–DC converter using gate-driver charge-recycling in 0.18 μm CMOS with an Integrated Output Filter. IEEE Power Electronics Specialists Conference, 2008: 140

[4] Huang H W, Chen K H, Kuo S Y. Dithering skip modulation width and dead time controllers in highly efficient DC–DC converters for system-on-chip applications. IEEE J Solid-State Circuits, 2007, 42(11): 2451

[5] Trescases O, Ng W T, Chen S. Precision gate drive timing in a zero-voltage-switching DC–DC converter. IEEE International Symposium on Power Semiconductor Devices and ICs, 2004: 55

[6] Cheng Jia. A delay-locked loop for multiple clock phases/delays generation. The United-State of American: Georgia Institute of Technology December, 2005

[7] Johnson M G, Hudson E L. A variable delay line PLL for CPU-coprocessor synchronization. IEEE J Solid-State Circuits, 1988, 23(5): 1218

[8] Razavi B. Design of analog CMOS integrated circuits. New York: The Mcgraw-Hill Companies, 2001

[9] Krummenacher F, Joehl N. A 4-MHz CMOS continuous-time filter with on-chip automatic tuning. IEEE J Solid-State Circuits, 1988, 23(3): 750