Soft error generation analysis in combinational logic circuits*

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Abstract: Reliability is expected to become a big concern in future deep sub-micron integrated circuits design. Soft error rate (SER) of combinational logic is considered to be a great reliability problem. Previous SER analysis and models indicated that glitch width has a great impact on electrical masking and latch window masking effects, but they failed to achieve enough insights. In this paper, an analytical glitch generation model is proposed. This model shows that after an inflexion point the collected charge has an exponential relationship with glitch duration and the model only introduces an estimation error of on average 2.5%.

Key words: soft error; glitch generation; analytical model
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1. Introduction

Along with technology scaling, the smaller node capacitance and lower supply voltage make the amount of charge stored in circuit nodes smaller and so integrated circuits are becoming increasingly vulnerable to soft error. Soft error is generated by alpha particles, fast neutrons, and thermal neutrons which may flip the memory circuit state. In combinational logic circuits, those particles may generate glitches which can be possible propagated and latched in memory circuits. Soft error alters the computation result but the physical device is not damaged[1−3].

A soft error rate (SER) of 3435 FIT for a DRAM based 1 GB memory and a soft error rate of 4000 FIT for a typical processor were reported where FIT means failure in 10^9 h[4, 5]. For three circuit boards which contained 100 Virtex II devices and which were placed at sea-level (3600 m), it was reported by Xilinx that there were 4 soft errors in 262 days (8 in 28 days)[6]. The crash of flagship servers of Sun Microsystems[7] is widely referred to.

It has been reckoned previously that combinational circuits are much less sensitive to soft errors. However, the combinational circuit SER is expected to increase significantly along with the reduced supply voltage and feature sizes[2]. Intensive research has been dedicated to mitigate the combinational circuit soft error rate. Triple modular redundancy[8], time redundancy and partial duplication[9, 10], gate sizing[11], optimal choice of some design parameters[12], flip-flop selection and instruction duplication[13, 14] are proposed.

Analytical models of soft error impact on SRAM are studied in Ref. [15]. The combinational logic soft error is studied in Refs. [16–18]. According to this research, the width of particle strike induced glitch is a very important parameter. It is hard to weaken wide glitches with the electrical masking effect while wider glitches are much more possible to be latched in memory devices than narrow ones. But this research has paid little attention to the distribution of glitch width.

The glitch width distribution problem is important for soft error analysis and mitigation. For example, recently, an output remapping method was proposed to mitigate the soft error of combinational logic[19]. This method comes from a novel observation about glitch width distribution. The glitch width seems to have a maximum value according to HSPICE simulation. Previous analytical models cannot explain this phenomenon. So Reference [19] proposed to enlarge the last stage propagation delay to annihilate all the glitches narrower than the maximum width. But the presented glitch generation model is merely based on simulation techniques which provide limited insights.

In this paper, an analytical glitch generation model is proposed. The model explains that after an inflexion point the collected charge has an exponential relationship with glitch duration. This conclusion is in accordance with the observation in Ref. [19], and the model only introduces an estimation error of about 2.6%. With the help of this model, we achieve some insights about the relation between the glitch generation characteristic of a logic cell and its size as well. This relation can be used to simplify soft error models of logic cells.

2. Background

When particles, like neutrons and alpha particles, pass the p/n junction, deposited electron hole pairs will move under the effect of electrical field. Thus a very short current pulse is generated. This injected current can be approximated with Eq. (1)[20]:

$$\begin{cases} I(t) = I_{\text{peak}}(\mathrm{e}^{-t/\tau_\alpha} - \mathrm{e}^{-t/\tau_\beta}), \\ \int I(t) = Q_{\text{collected}} = I_{\text{peak}}(\tau_\alpha - \tau_\beta), \end{cases} \tag{1}$$

where I_{peak} is the pulse strength, τ_α and τ_β are time constants depending on technology, and $Q_{\text{collected}}$ is the injected charge of this current pulse.

For an SRAM cell or a latch cell, if the collected charge of this current pulse is larger than a minimum value, the logic

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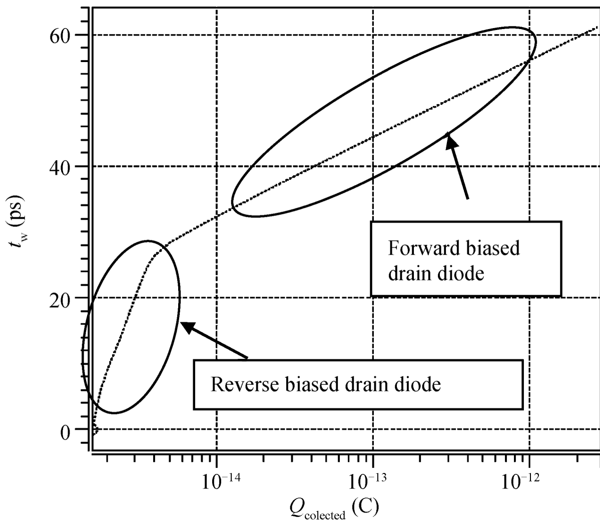

Fig. 1. $Q_{\text{collected}}$–t_{W} characteristic of inverter.

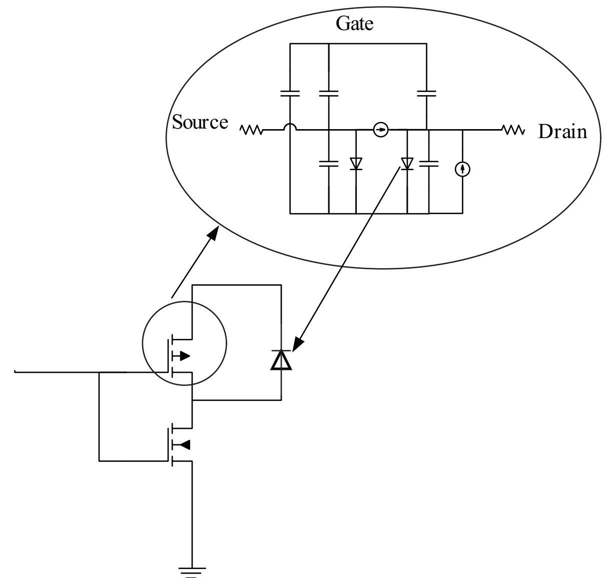

Fig. 2. Drain diode is reverse biased when the peak voltage is smaller than V_{dd}.

state of the cell will be flipped. This minimum value is called critical charge or Q_{critical}. In Ref. [1], an empirical model was proposed to estimate the soft error rate of memory circuits:

$$\text{SER} \propto N_{\text{flux}} \times \text{CS} \times \mathrm{e}^{-Q_{\text{critical}}/Q_{\text{S}}}, \tag{2}$$

where N_{flux} is the neutron flux, CS is the drain area struck by neutron flux, Q_{s} is the charge collection efficiency, and Q_{critical} is the critical charge of the node.

It is obvious from Eq. (2) that SER has an exponential relationship with Q_{critical}. So Q_{critical} is commonly used as the measurement of circuit vulnerability to particle strike.

The soft error rate of combinational logic circuits is vastly lower in comparison with memory circuits due to 3 phenomena: logical masking, electrical masking, and latch-window masking[2]. When a combinational node is hit by a particle, the circuit computation result is not affected if the generated pulse cannot propagate to the output or be latched by the memory circuit. Logical masking occurs when the glitch propagates to an input node of a logic cell whose computation result is controlled by another input node when the glitch arrives. Electrical masking occurs after the glitch is weakened during the propagation. It becomes so powerless that the computation result is not affected. Latch window masking occurs when the glitch arrives at a combinational output node, but is not latched because of the clock.

Q_{critical} of a node of a combinational logic circuit can be defined as the minimum amount of collected charge needed to generate a glitch strong enough to propagate to the output node and be latched.

3. Glitch generation model

In this section, an analytical model of the particle strike induced glitch of a logic cell is proposed. We will first present the phenomena discovered in previous research[19]. These phenomena are fundamentally very important for the soft error mitigation technique proposed in Ref. [19]. We will propose in this section that these phenomena are caused by the forward biased drain diode and then propose an analytical model for them.

There are 2 properties of a combinational logic cell concerning soft error rate: (1) the glitch generation property, which determines the amplitude and width of the generated voltage glitch when the cell is hit by a particle; and (2) the glitch propagation property, which indicates how the glitch propagates from its input node to its output. The transient current injection will cause a voltage pulse whose strength can be described by pulse width t_{w}. If the amplitude of the current pulse (I_{peak}) is more than a minimum value, pulse width t_{w} will be larger than 0. t_{w} will increase when I_{peak} increases. The collected charge of the current $Q_{\text{collected}}$ is proportional to I_{peak}. The $Q_{\text{collected}}$–t_{w} characteristic can be used to describe the glitch generation property. The example of an inverter based on our simulation is illustrated in Fig. 1. Please note that the $Q_{\text{collected}}$ axis has a logarithmic scale. As we can see from the figure, the curve is approximately linear-wise. A great increase of $Q_{\text{collected}}$ leads to a comparatively small increase of t_{w}. We will analyze these phenomena in this section. The drain diode mentioned in the figure is illustrated in Fig. 2.

The HSPICE simulation results of particle-strike-caused voltage pulse are illustrated in Fig. 3. We propose here that these results can be divided into two kinds. The first is that, as long as the particle energy is small enough, the maximum value of the voltage pulse is less than the supply voltage (V_{dd}), and the drain diode remains reverse biased, on which some research already exists. The second is that, as soon as the maximum value grows larger than $V_{\text{dd}} + u$, where u is the threshold voltage of the diode, the increase of the maximum voltage becomes slower, because the drain diode current cannot be ignored any longer. Both will be studied analytically in this section respectively.

3.1. Reverse biased drain diode

The equivalent circuit when the drain diode is reverse biased is illustrated in Fig. 4. In the figure, $I(t)$ is the injected current, r is the node resistance, and c is the node capacitance. This leads to the differential equation (3), which describes the

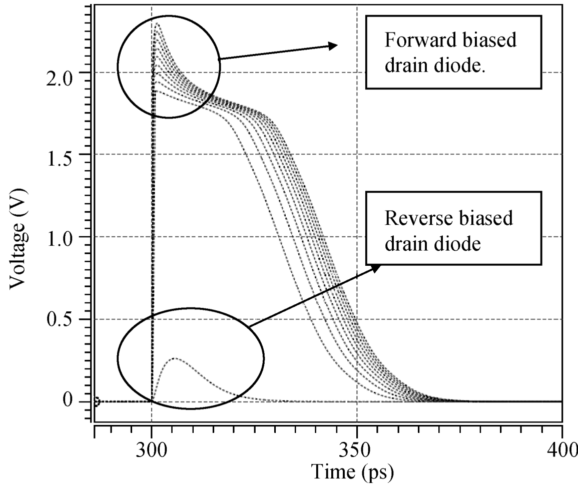

Fig. 3. Voltage pulse caused by particle strike.

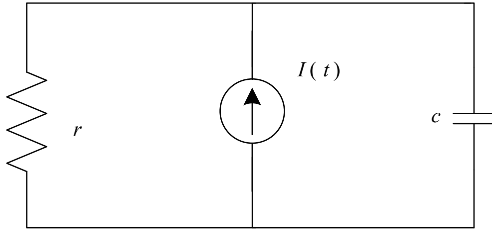

Fig. 4. Equivalent circuit of the current injected node.

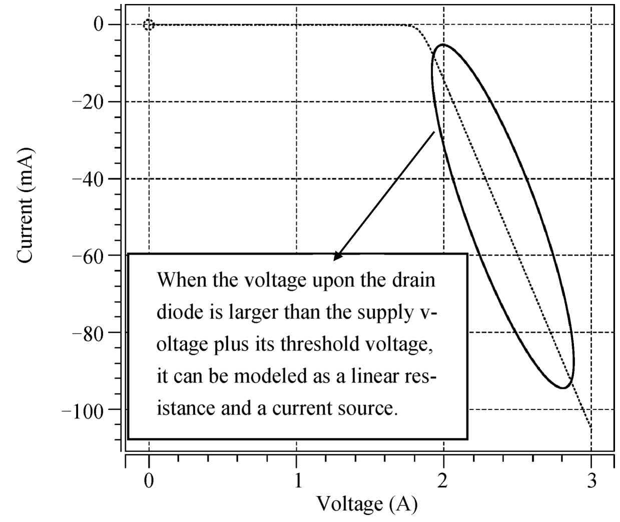

Fig. 5. Drain diode resistance.

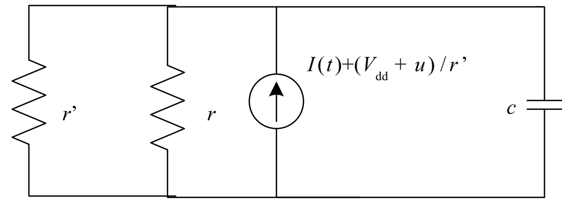

Fig. 6. Equivalent circuit of the current injected node.

relation between node voltage $V(t)$ and current $I(t)$:

$$c\frac{\mathrm{d}V(t)}{\mathrm{d}t}+\frac{V(t)}{r}=I(t). \tag{3}$$

From Eqs. (1) and (3), we have Eq. (4)[19]:

$$\begin{aligned}V(t)=&\frac{I_{\text{peak}}\tau_\alpha r}{\tau_\alpha-rc}\left(\exp\frac{-t}{\tau_\alpha}-\exp\frac{-t}{rc}\right)\\&-\frac{I_{\text{peak}}\tau_\beta r}{\tau_\beta-rc}\left(\exp\frac{-t}{\tau_\beta}-\exp\frac{-t}{rc}\right).\end{aligned} \tag{4}$$

To obtain the equation of glitch duration, we have to find the two roots of Eq. (5), where V_{dd} is the supply voltage:

$$\begin{aligned}\frac{V_{\text{dd}}}{2}=&\frac{I_{\text{peak}}\tau_\alpha r}{\tau_\alpha-rc}\left(\exp\frac{-t}{\tau_\alpha}-\exp\frac{-t}{rc}\right)\\&-\frac{I_{\text{peak}}\tau_\beta r}{\tau_\beta-rc}\left(\exp\frac{-t}{\tau_\beta}-\exp\frac{-t}{rc}\right).\end{aligned} \tag{5}$$

Equation (5) is a transcendental equation in t, so it is impossible to solve it analytically. But we can estimate the minimum collected charge corresponding to glitch width 0. Because τ_α is much larger than τ_β, the τ_β part of Eq. (1) approaches 0 much faster than the τ_α part. So we can use Eq. (6) to determine the time when $V(t)$ reaches its maximum value:

$$V(t)=\frac{I_{\text{peak}}\tau_\alpha r}{\tau_\alpha-rc}\left(\exp\frac{-t}{\tau_\alpha}-\exp\frac{-t}{rc}\right). \tag{6}$$

To find the minimum charge, we first differentiate Eq. (6) and then equate it to 0, which leads to Eq. (7):

$$0=\frac{I_{\text{peak}}\tau_\alpha r}{\tau_\alpha-rc}\left(\frac{1}{rc}\exp\frac{-t}{rc}-\frac{1}{\tau_\alpha}\exp\frac{-t}{\tau_\alpha}\right). \tag{7}$$

Equation (7) leads to Eq. (8)[16]:

$$t_{\max}=\frac{rc\tau_\alpha}{\tau_\alpha-rc}\ln\frac{\tau_\alpha}{rc}. \tag{8}$$

We obtain the minimum charge by substituting $t_{\max}$ for the value of t in Eq. (6), and hence Eq. (9):

$$Q_{\min}=\frac{cV_{\text{dd}}}{2}\frac{(\tau_\alpha-\tau_\beta)\exp\left(\frac{\tau_\alpha}{\tau_\alpha-rc}\ln\frac{\tau_\alpha}{rc}\right)}{\tau_\alpha}. \tag{9}$$

3.2. Forward biased drain diode

The voltage–current characteristic of the drain diode can be illustrated in Fig. 5. When the drain voltage is larger than $V_{\text{dd}}+u$, the diode can be modeled using a linear resistance and a current source approximately. The equivalent circuit is illustrated in Fig. 6, where the equivalent diode resistance r' and the current source are added compared with Fig. 4.

When I_{peak} is large enough, the glitch will become larger than $V_{\text{dd}}+u$. The time that the glitch rises and crosses $V_{\text{dd}}+u$, $t_{V_{\text{dd}}+u}$, can be estimated with Eq. (10), which is obtained by linearly expanding Eq. (5) around the origin:

$$\begin{cases} t_{V_{\rm dd}+u} = \dfrac{V_{\rm dd}+u}{X-Y}, \\ X = \dfrac{I_{\rm peak}\tau_\alpha r}{\tau_\alpha - rc}\left(\dfrac{-1}{\tau_\alpha}+\dfrac{1}{rc}\right), \\ Y = \dfrac{I_{\rm peak}\tau_\beta r}{\tau_\beta - rc}\left(\dfrac{-1}{\tau_\beta}+\dfrac{1}{rc}\right). \end{cases} \tag{10}$$

As $I_{\rm peak}$ approaches $+\infty$, $t_{V_{\rm dd}+u}$ approaches 0. It is in accordance with Fig. 3. We assume here that when the collected charge is large enough the node voltage at time 0 is $V_{\rm dd}+u$. This assumption is reasonable because the injected charge consumed between time 0 and $t_{V_{\rm dd}+u}$ is limited, and it can be estimated with Eq. (11):

$$Q_{t_{V_{\rm dd}+u}} \approx (V_{\rm dd}+u)c. \tag{11}$$

We can safely ignore the consumed charge as $I_{\rm peak}$ approaches $+\infty$, hence Eq. (12) which describes the node voltage:

$$\begin{cases} I(t) = c\dfrac{{\rm d}V(t)}{{\rm d}t} + \dfrac{V(t)}{r} + \dfrac{V(t)-V_{\rm dd}-u}{r'}, \\ V(0) = V_{\rm dd}+u. \end{cases} \tag{12}$$

By solving Eq. (12), we have Eq. (13), where $R_{r//r'}$ is the parallel resistance value of r and r':

$$\begin{aligned} V(t) = {} & \frac{I_{\rm peak}\tau_\alpha R_{r//r'}}{\tau_\alpha - R_{r//r'}c}\left(\exp\frac{-t}{\tau_\alpha} - \exp\frac{-t}{R_{r//r'}c}\right) \\ & - \frac{I_{\rm peak}\tau_\beta R_{r//r'}}{\tau_\beta - R_{r//r'}c}\left(\exp\frac{-t}{\tau_\beta} - \exp\frac{-t}{R_{r//r'}c}\right) \\ & + \frac{(V_{\rm dd}+u)r'}{r+r'}\exp\frac{-t}{R_{r//r'}c} \\ & + \frac{(V_{\rm dd}+u)r}{r+r'}, \quad R_{r//r'} = \frac{rr'}{r+r'}. \end{aligned} \tag{13}$$

We have to solve Eq. (14) in t to obtain the time when the node voltage falls below $V_{\rm dd}+u$.

$$\begin{aligned} V_{\rm dd}+u = {} & \frac{I_{\rm peak}\tau_\alpha R_{r//r'}}{\tau_\alpha - R_{r//r'}c}\left(\exp\frac{-t}{\tau_\alpha} - \exp\frac{-t}{R_{r//r'}c}\right) \\ & - \frac{I_{\rm peak}\tau_\beta R_{r//r'}}{\tau_\beta - R_{r//r'}c}\left(\exp\frac{-t}{\tau_\beta} - \exp\frac{-t}{R_{r//r'}c}\right) \\ & + \frac{(V_{\rm dd}+u)r'}{r+r'}\exp\frac{-t}{R_{r//r'}c} \\ & + \frac{(V_{\rm dd}+u)r}{r+r'}, \quad t \neq 0. \end{aligned} \tag{14}$$

Because $R_{r//r'}c$ and τ_β are much smaller than τ_α, we can use Eq. (15) to approximate Eq. (14):

$$V_{\rm dd}+u = \frac{I_{\rm peak}\tau_\alpha R_{r//r'}}{\tau_\alpha - R_{r//r'}c}\exp\frac{-t}{\tau_\alpha} + \frac{(V_{\rm dd}+u)r}{r+r'}. \tag{15}$$

Hence we have Eq. (16), in which t_1 denotes the time when the node voltage crosses $V_{\rm dd}+u$:

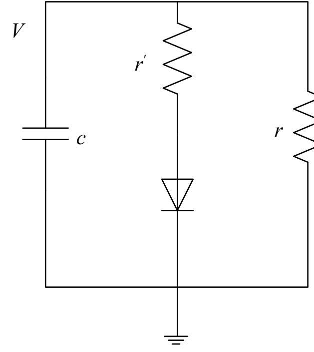

Fig. 7. Equivalent circuit of the current injected node.

$$Q = \frac{\exp\dfrac{t_1}{\tau_\alpha}(V_{\rm dd}+u)(\tau_\alpha-\tau_\beta)(\tau_\alpha - R_{r//r'}c)}{r\tau_\alpha}. \tag{16}$$

After this point, the resistance of the drain diode is nonlinear and the equivalent circuit is illustrated in Fig. 7. We can ignore the injected current safely because it decreases very quickly to 0. So the node voltage falls with a determined shape (please refer to Fig. 3 for the shape), and the amount of time it takes to fall from $V_{\rm dd}+u$ to $V_{\rm dd}/2$ is constant and is determined by the diode and the node capacitance and resistance. We use t_2 to denote the amount of time; please note that $t_1+t_2=t_{\rm w}$. Equation (17) follows, where t_2 is a constant:

$$\begin{aligned} Q &= \frac{\exp\dfrac{t_1+t_2}{\tau_\alpha}\exp\dfrac{-t_2}{\tau_\alpha}(V_{\rm dd}+u)(\tau_\alpha-\tau_\beta)(\tau_\alpha - R_{r//r'}c)}{r\tau_\alpha} \\ &= k\exp\frac{t_W}{\tau_\alpha}. \end{aligned} \tag{17}$$

Our model predicts that the time constant of the $Q_{\rm collected}$–$t_{\rm W}$ characteristic of different cells is τ_α, and cell type has no influence. This conclusion will be verified later.

4. Model verification

Our analytical model is verified in this section. Logic cells implemented with the PTM library in various sizes and loads are used in the experiments during which the $Q_{\rm collected}$–$t_{\rm W}$ characteristic of each cell is extracted[21]. Equation (17) is used to fit the experiments and the result is shown in Table 1.

For example, the first row of Table 1 is the result of an inverter with size 1 (the smallest inverter), whose load is two inverters of the same size. In the same row, τ_α comes from Eq. (17); τ_α error is the estimation error of τ_α; and the last column is the overall estimation error of the $Q_{\rm collected}$–$t_{\rm w}$ characteristic of this inverter. τ_α used in our experimentation is 5 ps, so the τ_α error column is obtained with $(\tau_{\alpha,\rm estimated} - 5\ {\rm ps})/5$ ps, where the $\tau_{\alpha,\rm estimated}$ comes from curve fitting.

From Table 1, it is observed that no size or load impact on the model precision is observed. It is also obvious that stack-

Table 1. Verification of Eq. (17).

Cell	Size	Fan out	τ_α (ps)	τ_α error	Error
inv	1	2	5.13	2.6%	2.4%
inv	1	4	5.14	2.8%	2.4%
inv	1	8	5.16	3.2%	2.5%
inv	2	2	5.15	3%	2.5%
inv	3	2	5.16	3.2%	2.5%
nand	1	2	5.16	3.2%	2.5%
nor	1	2	5.19	4.8%	2.6%

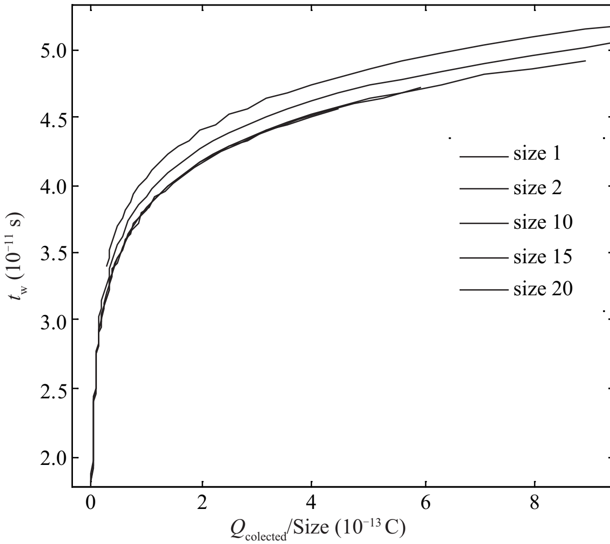

Fig. 8. Q in Eq. (18) is roughly proportional to gate size.

ing does not affect our model precision, including both NMOS stacking (nand) and PMOS stacking (nor).

Because $R_{r//r'}c$ is much smaller than τ_α, we can use Eq. (18) to approximate the charge Q in Eq. (17).

$$Q = (\tau_\alpha - \tau_\beta)(V_{dd} + u)\exp\left(\frac{-t_2}{\tau_\alpha}\right)\frac{1}{r}\exp\left(\frac{t_w}{\tau_\alpha}\right). \quad (18)$$

First, in the equation, τ_α and τ_β are technology dependent, and u depends on the technology as well. r (Fig. 7) is inversely proportional to the transistor size (or gate size).

Second, according to the HSPICE diode model, r' is inversely proportional to the diode size and the saturation current of the junction diode is proportional to the size. So we can approximately infer that the effective resistance in Fig. 7 is inversely proportional to the gate size. Obviously the intrinsic node capacitance which is a part of c in Fig. 7 is proportional to the transistor size. So t_2 remains about the same when load capacitance increases proportionally with gate size (so the gate delay stays approximately the same).

In summary, the first part of Eq. (18) $(\tau_\alpha - \tau_\beta)$ and the second part $(V_{dd} + u)$ are technology dependent; the third part remains approximately the same when the load capacitance increases proportionally with gate size. So the charge Q in Eq. (18) is roughly proportional to gate size when gate delay and pulse width stay the same. This relationship is shown in Fig. 8. In the figure, simulation results for inverters of various sizes are illustrated. All the curves are close to each other and the curves from ‘size 10’ to ‘size 20’ are too close to be distinguished from each other.

This relation can be used to simplify soft error models of logic cells. For example, there are inverters with different drive strengths in a logic cell library. With the help of this model, we can use the model of the smallest inverter to represent the others.

5. Conclusion

In this paper, an analytical glitch generation model is proposed. The model shows that after an inflexion point the collected charge has an exponential relationship with glitch duration and the model only introduces an estimation error of about 2.6%. A recently proposed combinational circuit soft error mitigation method[19] is based on the observation that the relation between propagation delay and glitch duration has a great impact on soft error rate. This paper provides more insights into the relation between glitch duration and soft error rate. With the help of this model, we achieve some insights into the relation between the glitch generation characteristic of a logic cell and its size as well. This relation can be used to simplify soft error models of logic cells. For future work, we will validate our model using real chips and analyze the key parameters in the proposed model.

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