A CMOS variable gain low-noise amplifier with ESD protection for 5 GHz applications*

Zhang Hao(张浩), Li Zhiqun(李智群)†, Wang Zhigong(王志功), Zhang Li(章丽), and Li Wei(李伟)

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: This paper presents a variable gain low-noise amplifier (VG-LNA) for 5 GHz applications. The effect of the input parasitic capacitance on the inductively degenerated common source LNA's input impedance is analyzed in detail. A new ESD and LNA co-design method was proposed to achieve good performance. In addition, by using a simple feedback loop at the second stage of the LNA, continuous gain control is realized. The measurement results of the proposed VG-LNA exhibit 25 dB (−3.3 dB to 21.7 dB) variable gain range, 2.8 dB noise figure at the maximum gain and 1 dBm IIP3 at the minimum gain, while the DC power consumption is 9.9 mW under a 1.8 V supply voltage.

Key words: continuous variable gain; low-noise amplifier; electrostatic discharge; co-design; CMOS
DOI: 10.1088/1674-4926/31/5/055005 **EEACC:** 2520

1. Introduction

The LNA is one of the key components in any communication system, because it is the first active block after the antenna and it determines the dynamic range of the receiver. The conventional inductively degenerated common source LNA is very often used for narrow band applications, because it can achieve low noise figure, high power gain, good reverse isolation and moderate linearity. For this topology, there are many optimization methods proposed in published studies[1, 2], but for simplicity, they ignore the effect of the input parasitic capacitance which come from the pad and the electrostatic discharge (ESD) protection circuits. Considering the reliability of products, ESD protection of the chips is very important and necessary. At RF frequencies, the parasitic capacitances of the input port have a significant effect on the performance of LNA[3], so, they must be taken into account in the circuit design carefully. Sivonen[4] proposed an ESD and LNA co-design method, but the biggest drawback of this method is that it needs two off-chip lumped components to realize the input power matching, which will increase the design complexity and the system cost.

In this paper, a two-stage cascade topology is adopted for the VG-LNA design. Through a detailed analysis of the parasitic effect, a new co-design method is proposed in the first stage. In addition, in order to avoid the saturation of the next block when the input power is large, the LNA must be able to change the gain. So, the second stage uses a simple feedback loop to realize the gain control. Therefore, the whole LNA can achieve a low noise figure and a broad gain control range simultaneously.

2. Input impedance analysis

2.1. Input impedance of the conventional LNA

A schematic of the conventional common source LNA with source inductive degeneration is shown in Fig. 1(a). C_p is the parasitic capacitor of the input pad and the ESD protection circuit. At several GHz, the influence of C_p is obvious.

Figure 1(b) shows the input stage small-signal circuit. The input impedance looking into the gate of M1 can be expressed by:

$$Z'_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} = \frac{1}{sC_1} + R_{eq}, \quad (1)$$

where

$$\frac{1}{C_1} = \frac{1}{C_{gs}} - \omega^2 L_s, \quad R_{eq} = \frac{g_m L_s}{C_{gs}}. \quad (2)$$

Through a series of parallel-series and series-parallel conversions in Fig. 2, we have:

$$R_{in} \approx \frac{1}{R_2 (\omega C_2)^2}, \quad (3)$$

$$C_{eq} \approx C_2 \approx C_1 + C_p, \quad (4)$$

where

$$R_2 \approx \frac{1}{R_{eq} (\omega C_1)^2}, \quad (5)$$

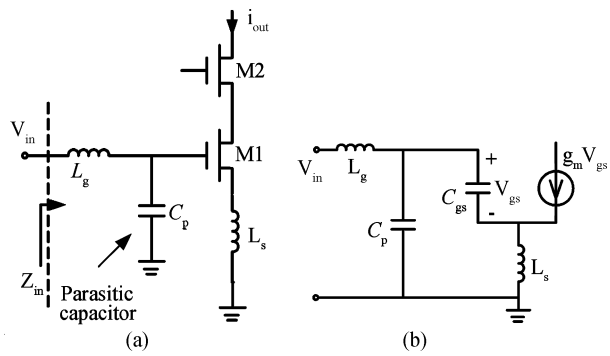

Fig. 1. Input stage of the conventional LNA. (a) Equivalent circuit. (b) Small-signal model.

* Project supported by the SEU-Winbond United Research Center and the National High Technology Research and Development Program of China (No. 2007AA01Z2A7).
† Corresponding author. Email: zhiqunli@seu.edu.cn
Received 21 October 2009, revised manuscript received 5 January 2010

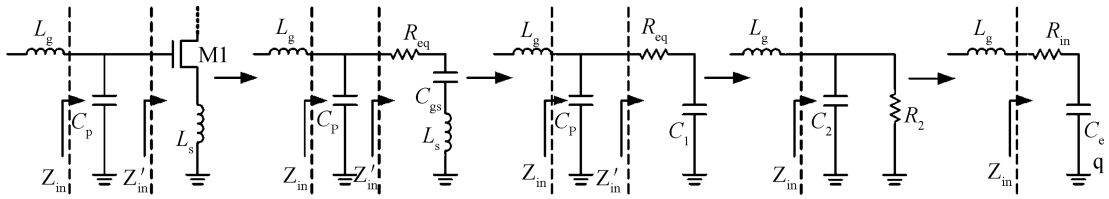

Fig. 2. Input impedance conversion.

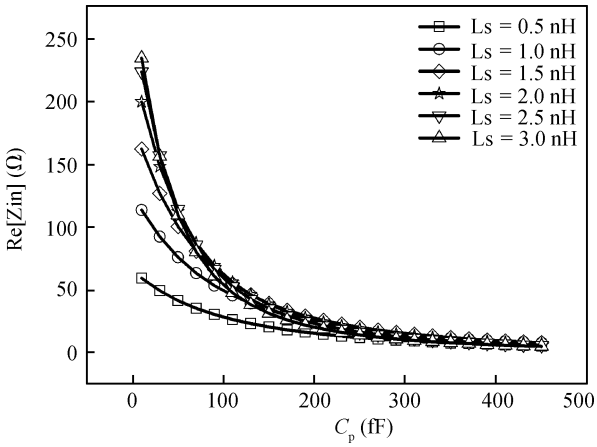

Fig. 3. Effect of C_p on the real part of the input impedance ($W/L = 90$ μm /0.18 μm, $V_{GS} = 0.65$ V, Freq = 5.25 GHz).

$$C_2 \approx C_1 + C_p. \tag{6}$$

The real part of the input impedance Z_{in} is then given as:

$$\mathrm{Re}\,(Z_{in}) = R_{in} = \left(\frac{C_1}{C_1 + C_p}\right)^2 R_{eq}. \tag{7}$$

From Eq. (7), it can be seen that the parallel parasitic capacitance C_p transforms downwards the real part of the input impedance. Figure 3 shows the real part of the input impedance Z_{in} versus the parasitic capacitance C_p at different L_s values. When C_p increases, the real part of Z_{in} reduces greatly. When $C_p > 200$ fF (usually C_p is greater than 200 fF), the real part of Z_{in} is below 30 Ω. A single inductor L_g cannot match the input impedance to 50 Ω. In order to achieve the input power match, Sivonen[4] gives a new ESD and LNA co-design method using an LC matching network, which can match the input impedance to 50 Ω easily. But this method needs two off-chip lumped components, increasing the system cost. In addition, this method cannot achieve input power matching and noise matching simultaneously. So, in the next section, a new ESD and LNA co-design method is proposed.

2.2. Input impedance of the proposed LNA

Figure 4 shows the schematic of the proposed LNA's input stage and its small-signal model. Compared with Fig. 2, the capacitance C_{ex} was added between the gate and the source of M1. By adding the capacitance C_{ex}, the real part of the input impedance has been increased.

From Eq. (7), the real part of the impedance Z_{in} can be re-expressed as follows:

$$\mathrm{Re}\,(Z_{in}) = \left(\frac{C_1}{C_1 + C_p}\right)^2 \frac{g_m L_s}{C_t}, \tag{8}$$

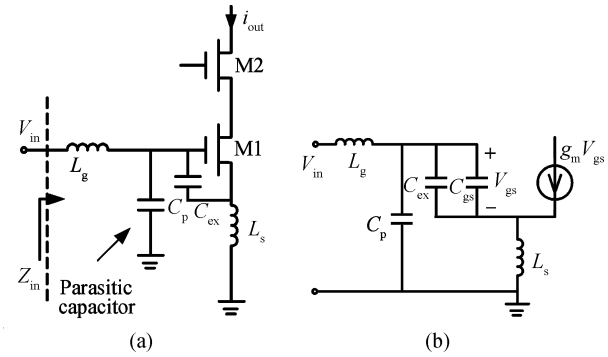

Fig. 4. Input stage of the proposed LNA. (a) Equivalent circuit. (b) Small-signal model.

where

$$\frac{1}{C_1} = \frac{1}{C_t} - \omega^2 L_s, C_t = C_{gs} + C_{ex}. \tag{9}$$

According to Eqs. (8) and (9), the real part of the impedance Z_{in} can be derived as follows:

$$\mathrm{Re}\,(Z_{in}) = \frac{g_m L_s}{\dfrac{a^2}{C_t} + b^2 C_t + 2ab}, \tag{10}$$

where

$$a = C_p,\ b = 1 - \omega^2 L_s C_p. \tag{11}$$

From Eq. (10), it can be seen that: when $C_t < a/b$, Re(Z_{in}) increases as C_{ex} increases; when $C_t = a/b$, Re(Z_{in}) achieves maximum; when $C_t > a/b$, Re(Z_{in}) decreases as C_{ex} increases. Figure 5 shows the simulation results of Re(Z_{in}) versus C_{ex} at different L_s. From Fig. 5, it can be seen that the real part of the input impedance can reach 50 Ω by using appropriate C_{ex} and L_s.

From Eqs. (3) and (4), the input impedance can be expressed by:

$$Z_{in} = R_{in} + sL_g + \frac{1}{sC_{eq}} = \left(\frac{C_1}{C_1 + C_p}\right)^2 \frac{g_m L_s}{C_t} + \frac{\dfrac{1}{sC_t} + sL_s}{1 + sC_p\left(\dfrac{1}{sC_t} + L_s\right)} + sL_g. \tag{12}$$

So, 50-Ω impedance matching could be achieved easily by choosing appropriate g_m, L_s, and C_{ex}. The inductor L_g must be selected as:

$$L_g = \frac{1}{C_3\omega^2} = \left[\omega^2\left(\frac{C_t}{1 - \omega^2 C_t L_s} + C_p\right)\right]^{-1}. \tag{13}$$

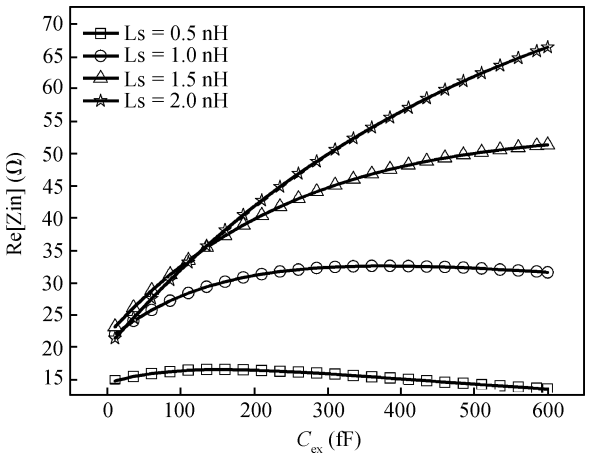

Fig. 5. Effect of C_{ex} on Re(Z_{in}).

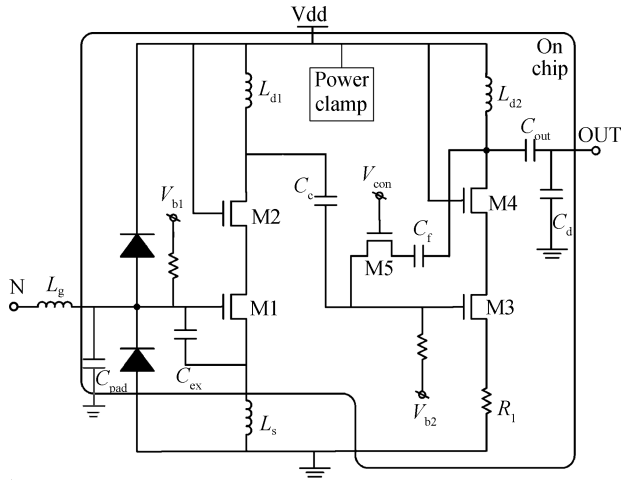

Fig. 6. Schematic of the VG-LNA.

In this method, a single inductor L_g can achieve input port matching to 50 Ω. At the same time, C_{ex} can achieve input power matching and noise matching simultaneously[2].

3. Circuit design

3.1. Circuit topology

Based on the theoretical results in section 2, a CMOS variable gain ESD-protected LNA for 5 GHz applications was designed. Figure 6 shows the schematic of the proposed VG-LNA, which is composed of two cascode stages with source degeneration. The total noise factor and linearity of the whole LNA can be expressed as[5]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} \tag{14}$$

$$\frac{1}{IIP3_{tot}^2} = \frac{1}{IIP3_1^2} + \frac{G_1^2}{IIP3_2^2}, \tag{15}$$

where G_1 is the first stage available power gain; F_{tot}, F_1 and F_2 are the noise factors of the total circuit, first stage and second stage, respectively; $IIP3_{tot}$, $IIP3_1$ and $IIP3_2$ are the third intercept points of the total circuit, first stage and second stage, respectively. From Eq. (14), it can be seen that the noise factor of the first stage is directly added to the noise factor of the total circuit, and a high gain of the first stage can suppress the noise contribution of the second stage. So, the first stage must have a low noise figure and a high enough gain. From Eq. (15), it can be seen that the linearity of the second stage is significant to the total LNA's linearity. Thus, the resistor R_1 was added to improve the second stage's linearity.

The input port and VDD were added to the ESD protection circuits. The load of the two stages uses the LC resonant network to acquire high power gain.

3.2. ESD and LNA co-design

The noise figure and the gain are mainly considered for the design of the first stage of the LNA. In the first stage, the inductor L_g, L_s, capacitance C_{ex} and parasitic capacitance C_p are used to achieve impedance matching at the input port. In order to acquire 2 kV HBM ESD protection, the value of ESD parasitic capacitance is about 200 fF[6]. In order to reduce the effect of C_p, the input pad only uses the top metal (M6) to reduce the pad's parasitic capacitance. The parasitic capacitance of the octagonal pad is about 35 fF. So, in this study, the value of C_p is about 235 fF.

Large f_T (which means a large overdrive voltage) can acquire low NF; large device size W can acquire high gain, but large W and overdrive voltage may increase the power consumption. So, the design of the LNA can be started by selecting the appropriate value of the overdrive voltage and device size. Figure 7 illustrates the simulated NF_{min} and f_T as a function of overdrive voltage under different device sizes. In Fig. 7, it can be seen that in the different device size W, the minimum NF_{min} occurs nearly at the same V_{gs}. So, we can select the V_{gs} first. Then, choose the device size W according to the power constraint, and obviously select the minimum gate length. Next, from Fig. 5, select the appropriate L_s and C_{ex}. A small value of L_s can imply a small value of Re(Z_{in}), even though C_{ex} is added. On the other hand, a large value of L_s may result in a low power gain and large noise figure. Usually, the value of L_s is about 1–3 nH, so, L_s = 1.5 nH is a reasonable compromise. Finally, the value of L_g is chosen according to Eq. (15). In this design, the inductor L_g was adopted for the bond wire inductor. Compared with the on-chip inductor, the Q factor of the bond wire is very high which can reduce the LNA's noise figure greatly.

3.3. Gain control mechanism

The gain control and linearity are mainly considered for the design of the second stage of the LNA. The continuous gain control is realized by adding a feedback loop in the second stage. The loop is controlled by an NMOS FET M5 in Fig. 6. When $V_{con} - V_{b2} < V_{th}$, M5 cuts off the feedback loop, the circuit is a classical cascode structure and the maximum gain is acquired; when $V_{con} - V_{b2} > V_{th}$, M5 works in the triode region with an equivalent resistance expressed by:

$$R_{on} = \frac{1 + \theta(V_{con} - V_{b2} - V_{th})}{K_n \dfrac{W}{L}(V_{con} - V_{b2} - V_{th})}, \tag{16}$$

where K_n is depends on the technology, V_{th} is the threshold voltage of the MOSFET, parameter θ models to a first order

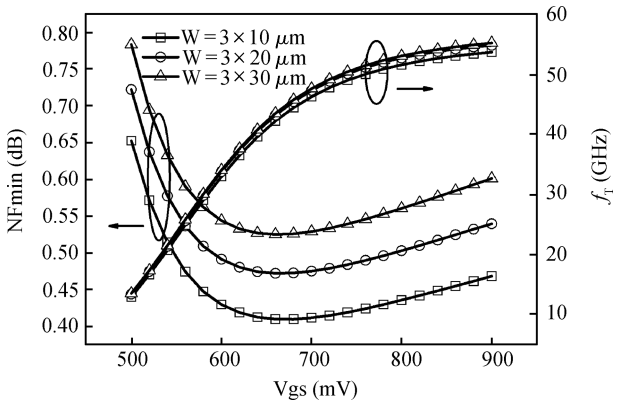

Fig. 7. f_T and NF_{min} versus V_{GS} at different $W(W/L = 90\ \mu m / 0.18\ \mu m$ @ $V_{DS} = 1$ V).

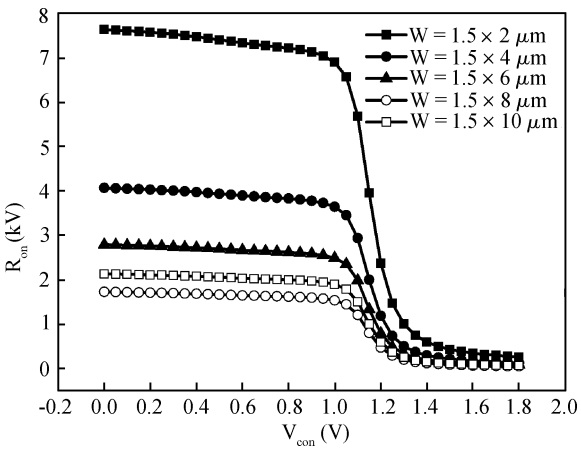

Fig. 8. R_{on} versus V_{con} under different transistor widths at $V_{b2} = 0.65$ V.

of the source series resistance, mobility degradation due to the vertical field, and velocity saturation due to the lateral field in short channel devices. By such a controlling scheme, the gain can be changed in a broad range. Figure 8 shows the equivalent resistance versus V_{con} under different transistor widths. From Fig. 8, it can be seen that a large device width will reduce the variable range of R_{on}. That is to say, a small device size can achieve a large gain variable range.

Ignoring the Miller effect and assuming that C_f is a short circuit, the voltage gain of the second stage can be expressed by:

$$V_{gain} = \frac{V_o}{V_i} = \frac{1 - \dfrac{g_{m3}}{1 + g_{m3}R_1}R_{on}}{1 + \dfrac{R_{on}}{Z_L}}, \tag{17}$$

where g_{m3} is the transconductance of M3, Z_L is the impedance of the load, and R_1 is the source degeneration resistor. From Eq. (17), it can be seen that the gain of the second stage is a function of R_{on}, so the gain is a function of V_{con}. When the control voltage V_{con} increases, the R_{on} and voltage gain are reduced.

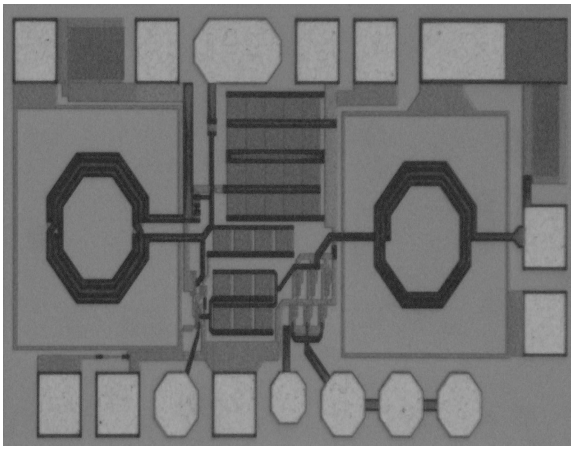

Fig. 9. Microphotograph of the VG-LNA.

4. Layout design and measurement results

The VG-LNA was fabricated in the SMIC 0.18-μm RF CMOS process. A micrograph of the VG-LNA is shown in Fig. 9. The chip area including all bonding pads is 485×950 μm^2. The chip was measured in the test laboratory of the Institute of RF- & OE-ICs, Southeast University. The major test equipment includes an Agilent network analyzer E5071B, a spectrum analyzer E4440A, an RF signal generator E4438C and a noise figure analyzer N8975A.

4.1. Layout design

In order to minimize the contribution of the substrate resistance on the input noise, M1 was divided into three parts, each part surrounded by substrate contacts[7]. In addition, each MOSFET was surrounded by a deep n-well (DNW) to reduce the noise and avoid the body effect. In order to avoid degradation of the output matching due to the output bonding wire inductor, the output adopts 150 μm wide gold strip bonding to the PCB board. In addition, this circuit uses two on-chip spiral inductors. Each inductor has a guard ring (composed of N^+ contacts and P^+ contacts) to isolate the noise. Large on-chip capacitors between V_{dd} and ground and between V_{con} and ground were used for bypass of the AC signals.

4.2. Measurement results

Figure 10 shows the measurement results of the S-parameter at the maximum gain (V_{con} = 1 V) and minimum gain (V_{con} = 1.8 V) states. From Fig. 10, it can be observed that the VG-LNA has a measured maximum gain of 21.7 dB and a minimum gain of –3.3 dB at 5.25 GHz.

Figure 11 shows the measured result of the noise figure at the maximum gain mode. The minimum noise figure is about 2.7 dB at 5 GHz. Figure 12 shows the relationship between the gain and the noise figure versus V_{con} at a center frequency of 5.25 GHz. It presents a large gain control range of 25 dB. At the low gain mode, the noise figure degradation is not serious. Figure 13 shows the measured linearity performance of the VG-LNA at a frequency of 5.25 GHz. The input 1-dB compression point at the maximum gain and minimum gain modes is −21 dBm and −9 dBm, respectively.

Table 1 gives the measured results of the VG-LNA compared to recently published works at the 5 GHz band. To eval-

Table 1. Performance comparisons between recently published LNAs.

Reference	Gain (dB)	NF (dB)	P_{dc} (mW)	P_{1dB} (dBm)	IIP3 (dBm)	Process (nm)	ESD	VGR (dB)	FOM_1 (dB/mW)	FOM_2 (mW^{-1})	FOM_3 (GHz)
Ref. [8]	14.8	2.6	6.6	Na	−9	130	yes	no	2.24	1.02	0.67
Ref. [9]	13.3	2.9	9.72	−11.5	−3	90	yes	no	1.37	0.50	1.32
Ref. [10]	18	2.6	10.3	Na	Na	130	yes	no	1.75	0.94	Na
	16	2	10.3	Na	Na	130	no	no	1.55	1.05	Na
Ref. [11]	20	3.5	15	Na	−9	180	yes	no	1.33	0.54	0.36
Ref. [12]	12.5	3.7	7.2	−11	−0.45	180	no	8.9	1.74	0.44	2.06
Ref. [13]	21.4	4.4	16.2	Na	−18.5/−6.5*	180	no	10.2	1.32	0.41	0.03
Ref. [14]	13.6	2.94	4.2	−20/−17.5*	−11/−6*	180	no	5.2	3.24	1.18	0.49
This work	21.7	2.8	9.9	−21/−9*	−11/1*	180	yes	25	2.19	1.36	0.57

VGR: variable gain range.
∗Correspond to the maximum gain mode and the minimum gain mode, respectively.

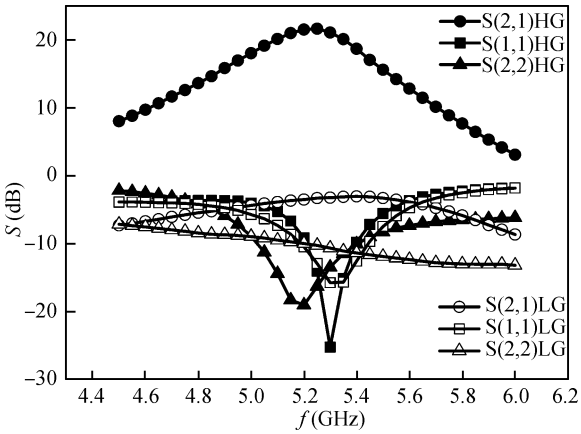

Fig. 10. Measured S-parameter at the maximum gain (HG) and minimum gain (LG) modes.

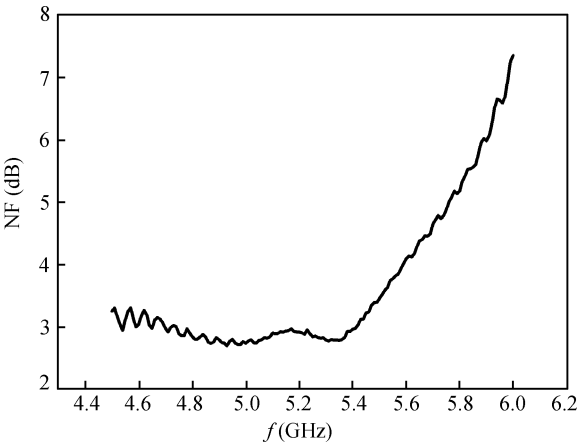

Fig. 11. Measured noise figure at the maximum gain mode.

uate the performance of the LNA, different figures of merit (FOM) are commonly used in the literature. One figure of merit of the LNA (FOM_1) is the ratio of the gain in dB to the dc power consumption in mW. Furthermore, it can be extended to include the NF, IIP3, and operating frequency as follows[8]:

$$\mathrm{FOM_2[mW^{-1}]} = \frac{\mathrm{Gain[abs]}}{(\mathrm{NF}-1)[\mathrm{abs}]\cdot \mathrm{Pdc[mW]}}, \quad (18)$$

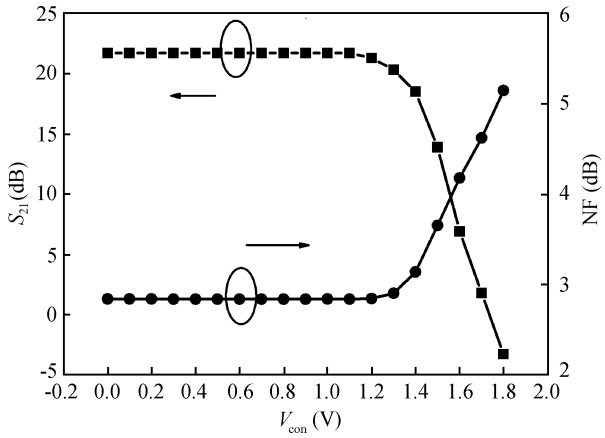

Fig. 12. Gain and noise figure versus V_{con} @ 5.25 GHz.

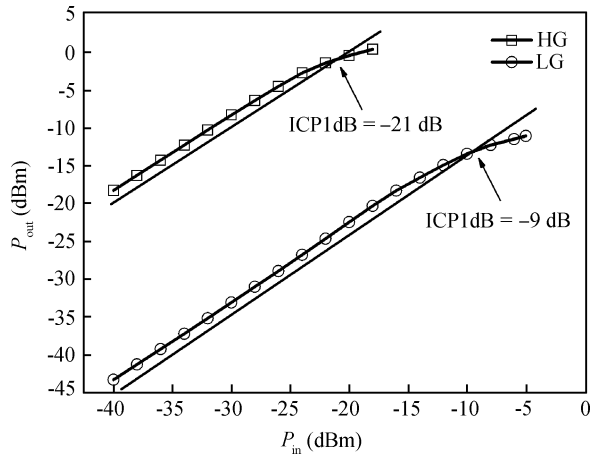

Fig. 13. Measured input 1-dB compression point.

$$\mathrm{FOM_3[GHz]} = \frac{\mathrm{Gain[abs]}\cdot \mathrm{IIP3[mW]}\cdot \mathrm{Freq[GHz]}}{(\mathrm{NF}-1)[\mathrm{abs}]\cdot \mathrm{Pdc[mW]}}. \quad (19)$$

5. Conclusions

In this paper, the effect of the input parasitic capacity on the input impedance of an LNA is analyzed in detail. Then, a new ESD and LNA co-design method was proposed. Based on this method, a continuous variable gain LNA for 5 GHz applications is presented. The measured results show that the

VG-LNA achieves good FOMs at high gain mode. In Table 1, some papers have a higher FOM than this work due to a lack of ESD protection or gain variable. In addition, by using a simple feedback loop on the second stage, the VG-LNA exhibits a large variable gain range of 25 dB. So this gain control mechanism can be used for many large dynamic range systems.

References

[1] Shaeffer D K, Lee T H. A 1.5 V, 1.5 GHz CMOS low noise amplifier. IEEE J Solid-State Circuits, 1997, 32(4): 745

[2] Nguyen T K, Kim C H, Ihm G J, et al. CMOS low-noise amplifier design optimization techniques. IEEE Trans Microw Theory Tech, 2004, 52(5): 1433

[3] Chandrasekhar V, Mayaram K. Analysis of CMOS RF LNAs with ESD protection. IEEE International Symposium on Circuits and Systems, 2002: 779

[4] Sivonen P, Parssinen A. Analysis and optimization of packaged inductively degenerated common-source low-noise amplifiers with ESD protection. IEEE Trans Microw Theory Tech, 2005, 53(4): 1304

[5] Razavi B. RF microelectronics. New Jersey: Prentice-Hall, 1998

[6] Richier C, Salome P, Mabboux G, et al. Investigation on different ESD protection strategies devoted to 3.3 V RF applications (2 GHz) in a 0.18 μm CMOS process. Proceeding of EOS/ESD Symposium, 2000: 251

[7] Colvin J T, Bhatia S S, Kenneth K O. Effect of substrate resistances on LNA performance and a bondpad structure for reducing the effects in a silicon bipolar technology. IEEE J Solid-State Circuits, 1999, 34(9): 1339

[8] Borremans J, Thijs S, Wambacq P, et al. A fully integrated 7.3 kV HBM ESD-protected transformer-based 4.5–6 GHz CMOS LNA. IEEE J Solid-State Circuits, 2009, 44(2): 344

[9] Linten D, Thijs S, Natarajan M I, et al. A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS. IEEE J Solid-State Circuits, 2005, 40(7): 1434

[10] Hsiao Y W, Ker M D. An ESD-protected 5-GHz differential low-noise amplifier in a 130-nm CMOS process. IEEE Custom Integrated Circuits Conference (CICC), 2008: 233

[11] Leroux P, Steyaert M. A 5 GHz CMOS low-noise amplifier with inductive ESD protection exceeding 3 kV HBM. European Solid-State Circuits Conference, 2004: 295

[12] Liao C H, Chuang H R. A 5.7-GHz 0.18-μm CMOS gain-controlled differential LNA with current reuse for WLAN receiver. IEEE Microw Wireless Compon Lett, 2003, 13(11): 526

[13] Raja M K, Boon T T C, Kumar K N, et al. A fully integrated variable gain 5.75-GHz LNA with on chip active Balun for WLAN. IEEE Radio Frequency Integrated Circuits Symposium, 2003: 439

[14] Sun P T, Liao S S, Lin H L, et al. The design of low noise amplifier with gain-controlled and low power consumption for WLAN applications. Progress in Electromagnetics Research Symposium, 2009: 906