A fast automatic power control circuit for a small form-factor pluggable laser diode drive*

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Abstract: A fast automatic power control (APC) circuit for a laser diode driver (LDD) has been implemented in a 0.6-μm BiCMOS process. The APC circuit adopts double-loops and variable-bandwidth techniques to achieve a turn-on time of < 400 μs for most kinds of TOSAs. Thus, it meets the small form-factor pluggable (SFP) agreement. Such techniques make a good tradeoff between stability, accuracy, turn-on time, noise and convenience. The measured results indicate that the APC circuit is suitable for SFP LDD.

Key words: APC; LDD; turn-on time; SFP
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1. Introduction

An LDD (laser diode driver) converts a current to optical power together with an LD (laser diode) in optical communication systems. To guarantee the signal quality, the average optical power must be stable. Unfortunately, the threshold current and the slope efficiency of an LD are related to the temperature and the aging. It is well known that the output optical power decreases while the temperature rises if the current remains constant. An APC (automatic power control) circuit is usually used to compensate the various threshold currents according to the temperature[1−3]. As is well known, an APC circuit is generally a closed loop although an open APC circuit has been reported elsewhere[4]. The optimization of the APC always focuses on the stability and the accuracy[5]. But for SFP applications, the turn-on time of the LDD is restricted under 1 ms as the system is enabled. So, the setting time of the APC must be less than 1 ms. As a closed loop, the setting time depends on its bandwidth. A wider bandwidth results in a faster setting, but poorer stability and more noise. Consequently, the conflict between stability, setting time, and noise should be resolved during the design of an APC circuit for SFP LDD.

This paper relearns the principle of the APC and illustrates the relationship between bandwidth, gain, setting time and noise. In order to achieve an optimized balance of these parameters, a novel fast APC circuit is proposed based on double loops together with a variable-bandwidth technique. Finally, such an APC is adapted to implement an SFP LDD and the measured results are presented.

2. Circuit design

2.1. APC principle

A traditional APC circuit is shown in Fig. 1(a). It is composed of input sampling resistor $R_{\rm in}$, an operating amplifier, a capacitor $C_{\rm APC}$, a tuning transistor Q1 and a transmitter optical subassembly (TOSA). When increasing the temperature results in decreased optical power and photodiode (PD) current, the output voltage of the differential amplifier as well as the collector current of transistor Q1 will rise. Consequently, the feedback loop tunes $i_{\rm BIAS}$ automatically to compensate the threshold current of the LD. So, the emitted optical power of the LD can remain constant regardless of changes in temperature, aging, etc. The average optical power is given by

$$P_{\rm avg} = \frac{V_{\rm ref}}{\rho R_{\rm in}}, \tag{1}$$

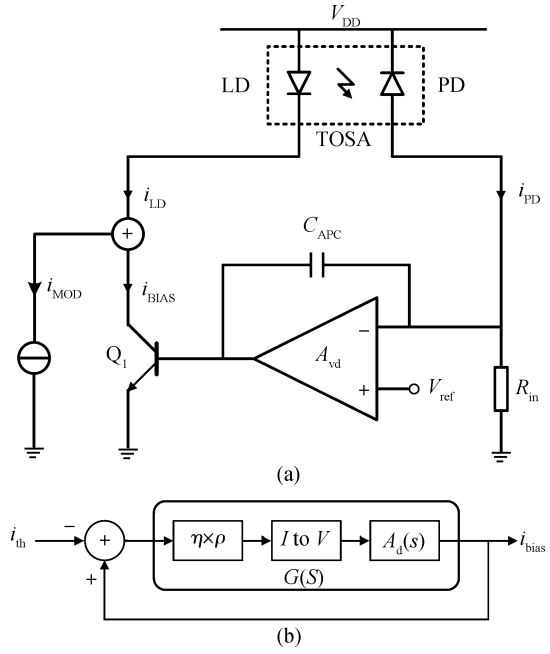

Fig. 1. (a) Block diagram of a traditional APC circuit. (b) Model of (a).

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where ρ is the efficiency of the PD and is approximately independent of the temperature. For convenient analysis, the threshold current of the LD and the collector current of transistor Q1 are regarded as the loop's input and output, respectively. The modulation current, marked with i_{MOD} in Fig. 1(a), is supposed to remain constant. The loop's small signal model is shown in Fig. 1(b) and the transfer function of the closed loop can be expressed as

$$H(s) = \frac{i_{\mathrm{bias}}(s)}{i_{\mathrm{th}}(s)} = \frac{-G(s)}{1-G(s)} \approx \frac{g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}A_{\mathrm{vd}}}{1+g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}A_{\mathrm{vd}}+sA_{\mathrm{vd}}R_{\mathrm{in}}C_{\mathrm{APC}}}, \quad (2)$$

with $G(s)$ the opened loop gain, g_{m} the transconductance of Q_1, η the slope efficiency of the LD, and A_{vd} the differential voltage gain of the amplifier.

For traditional applications, the opened loop gain G is designed to be high enough for reducing deviation between i_{bias} and i_{th}, and the pole frequency is sufficiently low to guarantee stability and noise attenuation. But for SFP applications, the loop's setting time must be considered. With step input of $I_{\mathrm{th}}\varepsilon(t)$, the output response in the time domain can be derived from Eq. (2) to be:

$$i_{\mathrm{bias}}(t) = I_{\mathrm{TH}}\frac{g_{\mathrm{m}}\eta\rho A_{\mathrm{vd}}R_{\mathrm{in}}}{g_{\mathrm{m}}\eta\rho A_{\mathrm{vd}}R_{\mathrm{in}}+1} \times\left[1-\exp\left(-\frac{g_{\mathrm{m}}\eta\rho A_{\mathrm{vd}}R_{\mathrm{in}}+1}{A_{\mathrm{vd}}R_{\mathrm{in}}C_{\mathrm{APC}}}t\right)\right] \approx I_{\mathrm{TH}}\left[1-\exp\left(-\frac{g_{\mathrm{m}}\eta\rho}{C_{\mathrm{APC}}}t\right)\right]. \quad (3)$$

This expression shows that the response time can be reduced with an increase in g_{m} or a decrease in C_{APC}. But the choice of C_{APC} is simultaneously limited by the noise from data especially with long consecutive "0" or "1". Such a conflict becomes too serious to implement a practical system in a low speed data link, such as 125-Mb/s Ethernet.

In addition, if the output resistance of the amplifier shown in Fig. 1(a) is not zero, the loop's transfer function should be revised to be:

$$H(s) = \frac{(A_{\mathrm{vd}}-sR_{\mathrm{o}}C_{\mathrm{APC}})g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}}{1+g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}A_{\mathrm{vd}}+s(A_{\mathrm{vd}}-g_{\mathrm{m}}\eta\rho R_{\mathrm{o}})R_{\mathrm{in}}C_{\mathrm{APC}}}, \quad (4)$$

where R_{o} is the output resistance of the amplifier. Equation (4) indicates a zero in the right plane, which will worsen the noise performance and the loop stability. Thus, an additional pole is added to attenuate the high-frequency noise and an appropriate loop bandwidth is chosen for stability in practical products[6]. Moreover, various values of C_{APC} should be chosen for TOSAs with different $\eta\times\rho$ to meet the turn-on time specification[7]. It is more difficult to do this with consideration of the temperature factor.

2.2. Fast APC

As is well known, the APC loop must be working at a fixed DC point to make the analysis in Section 2.1 right. But the setting process of such a DC point will consume a long time after the loop is enabled. To reduce the initial time of the loop,

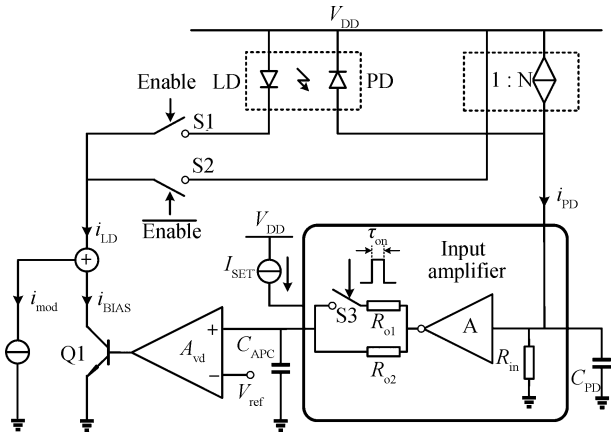


Fig. 2. Block diagram of the proposed fast APC circuit.

a novel fast APC circuit as shown in Fig. 2 is proposed. It is composed of double loops. When the loop is disabled, switch S1 is off whereas switch S2 is on. Consequently, a current mirror is connected into the loop instead of the TOSA to establish another loop. Every node of the loop, especially the main pole node with capacitor C_{APC}, will still work at a certain DC point even though the loop is disabled. The value of mirror ratio N should be optimized to avoid overcurrent once the loop is enabled. An efficient method is to choice appropriate values of N and I_{SET} in the disabled APC loop to hold the voltage on C_{APC} at the lowest value of the variable range.

The above technique based on double loops only reduces the loop's initial time. As mentioned in Section 2.1, the loop's response time is related to bandwidth, which conflicts with other performance parameters. To achieve a tradeoff between accuracy, stability, setting time and noise, a variable bandwidth technique is proposed in the fast APC circuit, shown in Fig. 2. The bandwidth variation occurs once the loop is enabled and the duration is always less than 1 ms. With the same analysis method of the traditional APC circuit, the transfer function of the enabled loop shown in Fig. 2 can be given by

$$H(s) = g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}/\left[R_{\mathrm{o}}R_{\mathrm{in}}C_{\mathrm{APC}}C_{\mathrm{PD}}s^2 +(R_{\mathrm{o}}C_{\mathrm{APC}}+R_{\mathrm{in}}C_{\mathrm{PD}})s+sR_{\mathrm{in}}C_{\mathrm{PD}}+g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}+1\right], \quad (5)$$

where R_{o} is the output resistance of the input amplifier. This expression shows that there is no zero in the loop and two poles are listed as follows.

$$\omega_{\mathrm{p}} = \omega_{\mathrm{H}} \approx \frac{1+g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}}{R_{\mathrm{o}}C_{\mathrm{APC}}+R_{\mathrm{in}}C_{\mathrm{PD}}} \approx \frac{g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}}{R_{\mathrm{o}}C_{\mathrm{APC}}}, \quad (6)$$

$$\omega_{\mathrm{p2}} \approx \frac{R_{\mathrm{o}}C_{\mathrm{APC}}+R_{\mathrm{in}}C_{\mathrm{PD}}}{R_{\mathrm{o}}R_{\mathrm{in}}C_{\mathrm{APC}}C_{\mathrm{PD}}} \approx \frac{1}{R_{\mathrm{in}}C_{\mathrm{PD}}}. \quad (7)$$

So, the high frequency noise from data can be attenuated at a ratio of -40 dB/dec, and the output bias current can be low noise regardless of data patterns. Treated as a single pole system with neglect of ω_{p2}, the loop's transfer function can be simplified to be

$$H(s) \approx \frac{g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}/(1+g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}})}{1+\dfrac{s}{\omega_{\mathrm{H}}}}$$

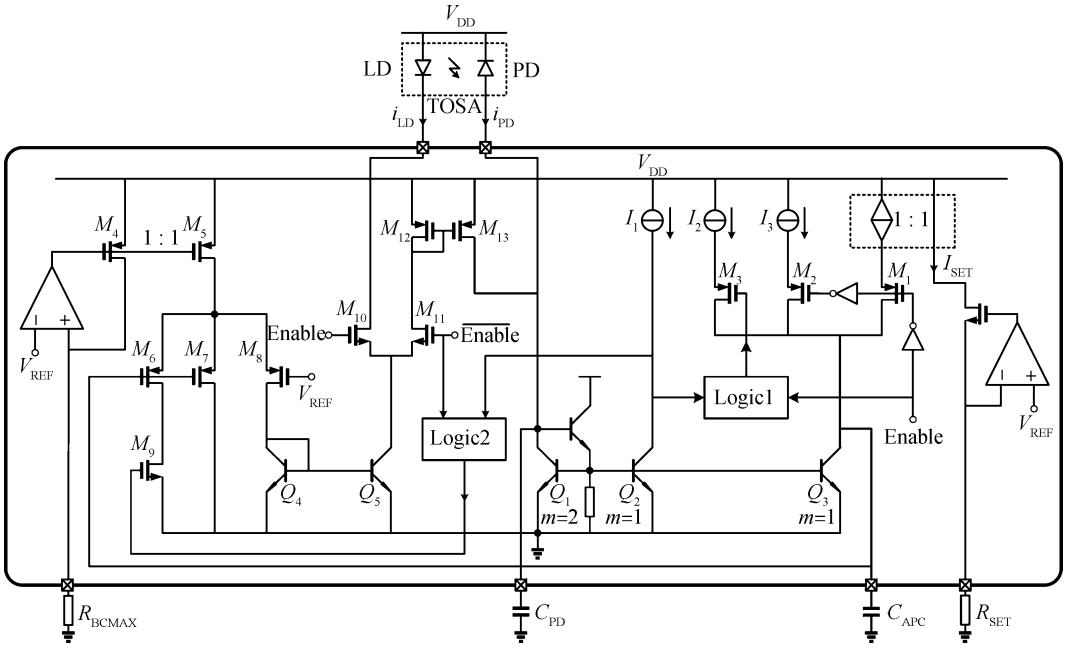


Fig. 3. Simplified schematic of the fast APC circuit.

$$\approx \frac{1}{1+s\Big/\dfrac{g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}}{R_{\mathrm{o}}C_{\mathrm{APC}}}}, \tag{8}$$

with a step input of $I_{\mathrm{th}}\varepsilon(t)$, and the transient response of i_{bias} can be expressed as

$$i_{\mathrm{bias}}(t) = I_{\mathrm{TH}}\Big[1-\exp\Big(-\frac{g_{\mathrm{m}}\eta\rho R_{\mathrm{in}}AA_{\mathrm{vd}}}{R_{\mathrm{o}}C_{\mathrm{APC}}}t\Big)\Big]. \tag{9}$$

Compared with Eq. (3), the above expression indicates that smaller R_{o} results in a faster response if the others remain constant. But Equations (5) and (6) show that R_{o} influences the loop's pole frequency, stability and noise attenuation simultaneously. So, an appropriate tradeoff is to decrease R_{o} only during the loop's turn-on time required by SFP agreement. As shown in Fig. 2, switch S3 turns on after the loop is enabled and R_{o} is decreased from R_{o2} to be $R_{\mathrm{o1}}//R_{\mathrm{o2}}$. Once the loop finishes all the steps to turn on, switch S3 returns to being off. Such a variable output resistance means variable bandwidth of the loop and provides an approach to the balance of accuracy, stability, response time and noise attenuation. Therefore, the open loop gain can be designed to be large with a fixed capacitor C_{APC} regardless of the TOSA's performance or the data pattern, which is very convenient for application.

Equation (9) indicates that the response time of i_{bias} is independent of I_{th}, which is contrary to the facts. Such a conflict comes from ignorance of the amplifier's driving ability, or slew rate. Actually, on the other hand, the means of variable output resistance changes the slew rate of the amplifier.

2.3. Circuit design

The fast APC circuit according to Fig. 2 is implemented in 0.6-μm BiCMOS technology and its simplified schematic is shown in Fig. 3. The transistors Q1–Q3, the current sources of I_1–I_3, I_{SET} and the digital cell marked as logic1 comprise the input amplifier. The components in the differential amplifier include transistors of M4–M9, Q4 and a digital cell, named logic 2. The current mirror composed of transistors M12–M13 is connected into the loop while the TOSA off-chip is disconnected when the loop is disabled. In the input amplifier, the current sources I_{SET} and I_3 are switched on alternately, controlled by the enable signal. As the value of I_3 is smallest in the range of I_{SET}, the voltage on C_{APC} maintains the lowest value near to V_{REF} when the loop is disabled. Once the loop is enabled, i_{PD} is compared with current source I_1 to generate a pulse together with the enable signal to control current source I_2, which can change the output resistance of transistor Q3. Since the initial voltage on C_{APC} is near to V_{REF} and the current in transistor Q3 is boosted by I_2, the voltage on C_{APC} can reach the normal value rapidly. Ultimately, the PD current which is proportional to optical power is stabilized to $2I_{\mathrm{SET}}$, as illustrated in Section 2.

Table 1. Parameters for simulation.

Parameter	Value
C_{APC}	100 nF
C_{PD}	1 nF
$\eta\times\rho$	0.03
Threshold of LD	20 mA
i_{MOD}	0 mA
R_{SET}	1.2, 12, 120 kΩ

For convenience in application, the circuit shown in Fig. 2 has been optimized carefully to meet most kinds of TOSAs with fixed off-chip capacitors. With typical parameters listed in Table 1, the frequency response of the open loop and the transient response of the closed loop are presented in Figs. 4(a) and 4(b), respectively. In Fig. 4(a), the open loop response achieves a phase margin of $> 80°$ and noise attenuation of -80 dB/dec over 1 MHz. Figure 4(b) shows the setting process of $V(C_{\mathrm{APC}})$ and i_{LD} after the loop is enabled at 100 μs. The worst case of setting time is less than 170 μs with $R_{\mathrm{SET}} = 120$ kΩ and $I_{\mathrm{SET}} = 10$ μA.

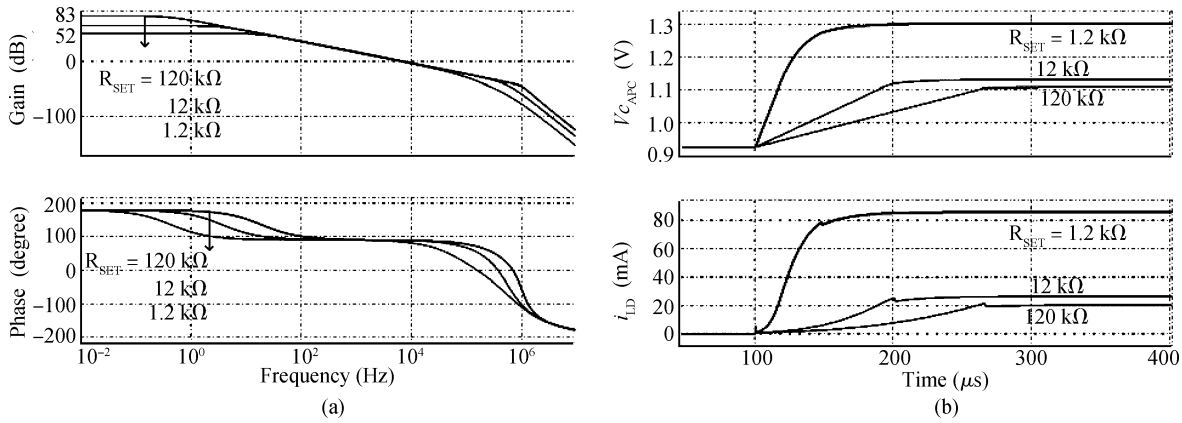


Fig. 4. (a) Frequency response of the open loop. (b) Transient response of the closed loop.

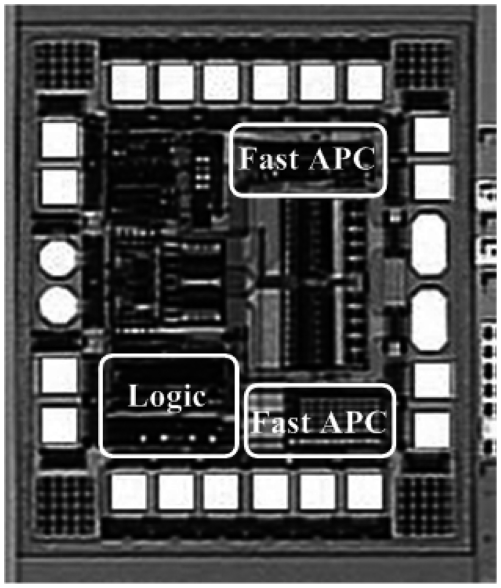


Fig. 5. Die photograph of the LDD with a fast APC.

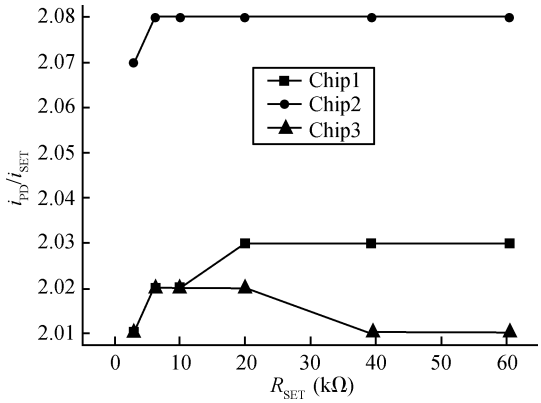


Fig. 6. Setting ratio of i_{PD}/i_{SET}.

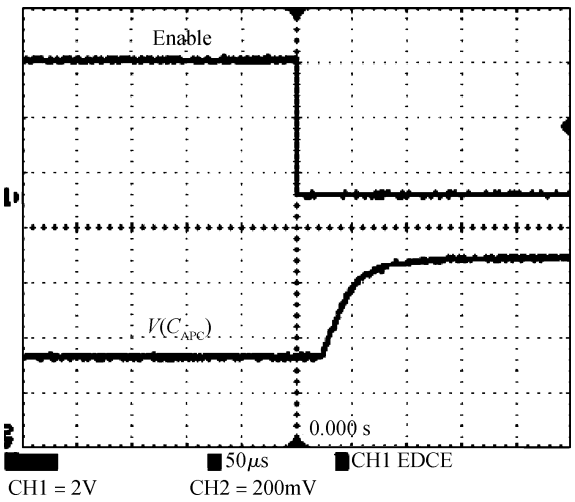


Fig. 7. Transient response of $V(C_{APC})$.

3. Measured results

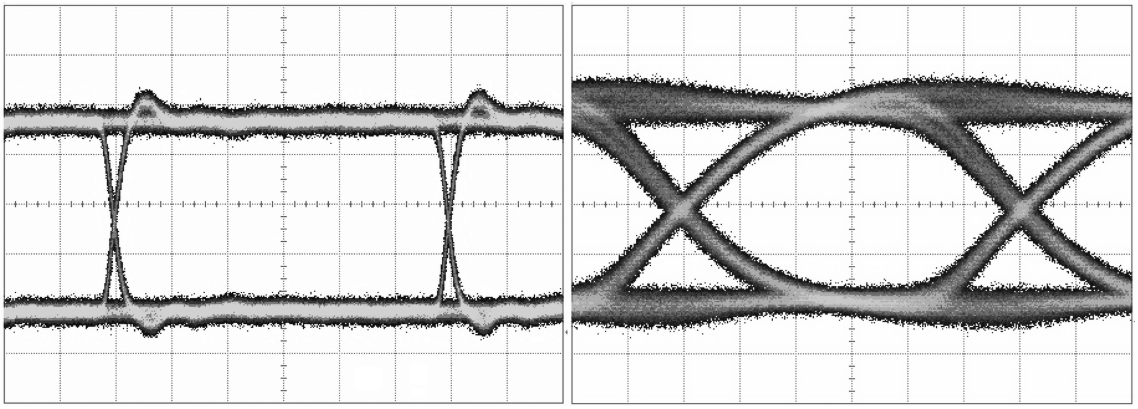
The fast APC circuit proposed in this paper has been implemented in a 0.6-μm BiCMOS process for 1.25-Gb/s SFP LDD. The die photograph is shown in Fig. 5. Such an LDD has been measured together with a TOSA and other off-chip components. The TOSA has a typical current gain of 0.03, expressed as i_{PD}/i_{LD}. With 3.3 V or 5 V supply, the current consumption is 2–10 mA according to different conditions, which excludes output i_{BIAS}.

Figure 6 is the measured setting ratio of the APC loop. It is sampled from different chips and indicates the setting error of $< \pm 5\%$. Figure 7 shows the transient process of $V(C_{APC})$, main pole of the loop, before and after the loop is enabled.

According to the measured results, a rapid response requiring less than 80 μs to turn on 100 mA bias current is achieved. The values of C_{APC} and C_{PD} are 100 nF and 1 nF, respectively. These capacitors do not need to be changed even though the LDD works with other TOSAs or works at a different data rate. The ultimate optical eye diagrams at 155 Mb/s and 1.25 Gb/s, shown in Figs. 8(a) and 8(b), prove the loop's stability and show a satisfactory noise attenuation. The detailed performance is summarized in Table 2.

4. Conclusion

A fast APC circuit has been implemented in a 0.6-μm BiCMOS process. The APC circuit adopts double-loops and the variable-bandwidth technique to accelerate the transient re-



(a) (b)

Fig. 8. (a) Optical eye diagrams at 155 Mb/s, 100 μW/div, 1.12 ns/div. (b) Optical eye diagrams at 1.25 Gb/s, 100 μW/div, 132 ps/div.

Table 2. Summarized performance of the fast APC circuit.

Parameter	Value	Condition
Supply range	3–5.5 V	
Current consumption	2–10 mA	$R_{\rm SET}$ = 1.2–120 kΩ
Output current range	2–100 mA	$R_{\rm BCMAX} \leqslant$ 3 kΩ
$I_{\rm SET}$ range	20–2000 μA	$R_{\rm SET}$ = 1.2–120 kΩ
Setting error of $i_{\rm PD}$	$< \pm$5%	($i_{\rm PD}/i_{\rm SET}-2$)/2
Turn-on time	$<$ 400 μs	$C_{\rm APC}$ = 100 nF, $C_{\rm PD}$ = 1 nF
Noise attenuation	$>$ 60 dB	@ 2 MHz

sponse. With fixed off-chip capacitors, the turn-on time of the APC loop is measured to be $<$ 80 μs, which is guaranteed to be $<$ 400 μs by design for most kinds of TOSAs. Simultaneously, other performance parameters such as stability, accuracy, noise attenuation etc, are also satisfied. These measured results indicate that the proposed fast APC circuit is suitable for SFP LDD.

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