A current-mode voltage regulator with an embedded sub-threshold reference for a passive UHF RFID transponder

Liu Zhongqi(刘忠奇)[1,†], Zhang Chun(张春)[2], Li Yongming(李永明)[2], and Wang Zhihua(王志华)[2]

(1 Department of Electronic Engineering, Tsinghua University, Beijing 100084, China)
(2 Institute of Microelectronics, Tsinghua University, Beijing 100084, China)

Abstract: This paper presents a current-mode voltage regulator for a passive UHF RFID transponder. The passive tag power is extracted from RF energy through the RF-to-DC rectifier. Due to huge variations of the incoming RF power, the rectifier output voltage should be regulated to achieve a stable power supply. By accurately controlling the current flowing into the load with an embedded sub-threshold reference, the regulated voltage varies in a range of 1–1.3 V from –20 to 80 ℃, and a bandwidth of about 100 kHz is achieved for a fast power recovery. The circuit is fabricated in UMC 0.18 μm mixed-mode CMOS technology, and the current consumption is only 1 μA.

Key words: RFID; tag; regulator
DOI: 10.1088/1674-4926/31/6/065006 **EEACC:** 2570

1. Introduction

RFID technology firstly appeared in World War II for flight fighter recognition. Nowadays this technology has been widely implemented in many areas such as supply chain management, access control and environment monitoring. RFID transponders fall into two categories: active and passive. The passive transponder uses the RF energy transmitted by the reader as its power source. Figure 1 shows the conversion of RF power into a DC voltage supply. The RF energy is induced on the tag antenna and converted into the voltage supply by the RF-to-DC rectifier, which is realized by stacked voltage doublers known as a Dickson charge pump[1]. Since the transponder is located at various distances from the reader, the receiving radio power varies aggressively and causes huge rectifier output voltage fluctuations. As a result, a voltage regulator is necessary to be placed at the rectifier output to generate a stable power supply. There are two cases when there is instant absence of RF power available for tag. One is that for the forward link (reader to tag communication), a bit “0” is denoted by the absence of RF energy. The other one is for the reverse link (tag to reader communication), when the reader transmits full RF power, a bit “1” is sent to the reader by connecting the tag antenna to ground to reflect most of the receiving energy back to the reader, known as backscatter modulation. As a result, an on chip capacitor should be connected with the regulator output to provide power for the transponder during the absence of RF power and to store energy when RF power appears.

Figure 2(a) shows a simple voltage regulator using a crude voltage clamp. When $V_{\rm DD}$ exceeds $3V_{\rm D} + V_{\rm thn}$, where $V_{\rm D}$ and $V_{\rm thn}$ are the threshold voltages of the diode and NMOS transistor respectively, the bypass device turns on and provides an alternate path for the excess current. Hence, $V_{\rm DD}$ is crudely clamped to $3V_{\rm D} + V_{\rm thn}$. This circuit suffers from two problems. Firstly, $V_{\rm thn}$ and $V_{\rm D}$ change with the process and temperature variations. On the other hand, due to its small voltage-to-current gain, a fine regulated voltage cannot be achieved. To resolve these two problems, a regulator with a voltage reference, shown in Fig. 2(b), is produced. A simple different amplifier compares the scaled voltage of $V_{\rm DD}$ with the reference to control the bypass device current. However, a pole is added due to the amplifier, leading to limited bandwidth and instability problems[2]. Huge variations of input and load currents also make frequency compensation very difficult. The two regulators described above are parallel regulators with a bypass device to conduct the excess current. The other method, called series regulation, is to insert a pass device between the rectifier output and power supply as shown in Fig. 2(c)[3]. The voltage across the pass device increases with the rectified voltage to keep the supply voltage below a fixed value. Nevertheless, the input power is very limited without the device for huge power dissipation. Furthermore, all devices of the amplifier operate under an unregulated high voltage and the circuit lifetime is affected. A combination of both the parallel and series regulations is presented in Ref. [2]. A dynamic bias method is also introduced in the regulator to ensure enough bandwidth and phase margin. However, two diodes in the current path cause large voltage loss and low power efficiency at far field leading to limitation of the communication range. A maximum bandwidth of 90 kHz is achieved with large receiving power.

So a current-mode regulator is proposed to clamp the supply voltage by precisely controlling the rectified current to the load with a series current source of 35 μA and two parallel current bypass paths. The regulated voltage is set at 1.2 V for low power circuit operation and a bandwidth of 100 kHz is achieved.

2. Current-mode voltage regulator

A new architecture for the regulator is developed as shown in Fig. 3. The output of the rectifier is modeled as a current source $I_{\rm in}$. Firstly, a bypass current path I_1 is connected between V_1 and ground and it will be conducted when V_1 exceeds

† Corresponding author. Email: liu-zq04@mails.tsinghua.edu.cn
Received 8 November 2009, revised manuscript received 8 January 2010

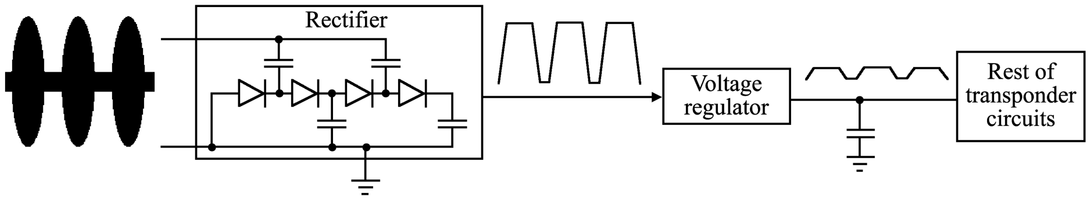


Fig. 1. Conversion of RF power into DC supply.

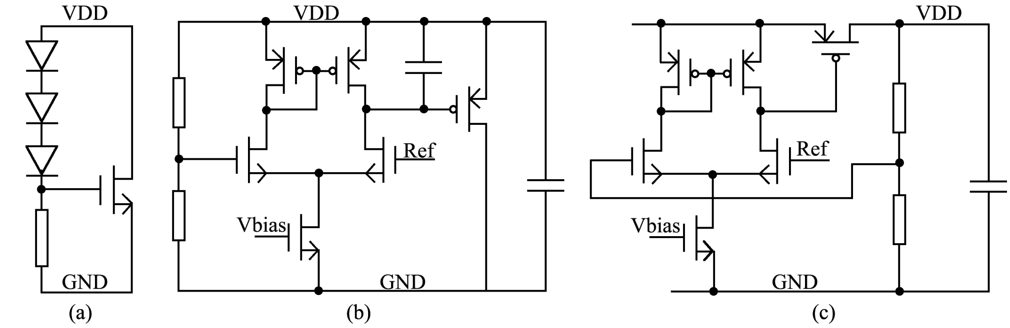


Fig. 2. Conventional voltage regulators.

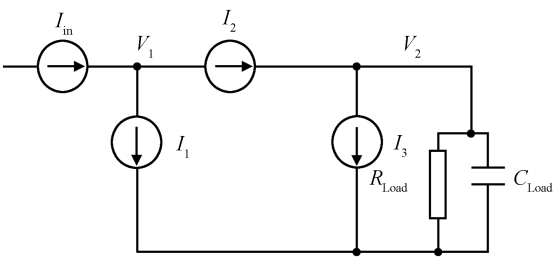


Fig. 3. Current mode voltage regulation.

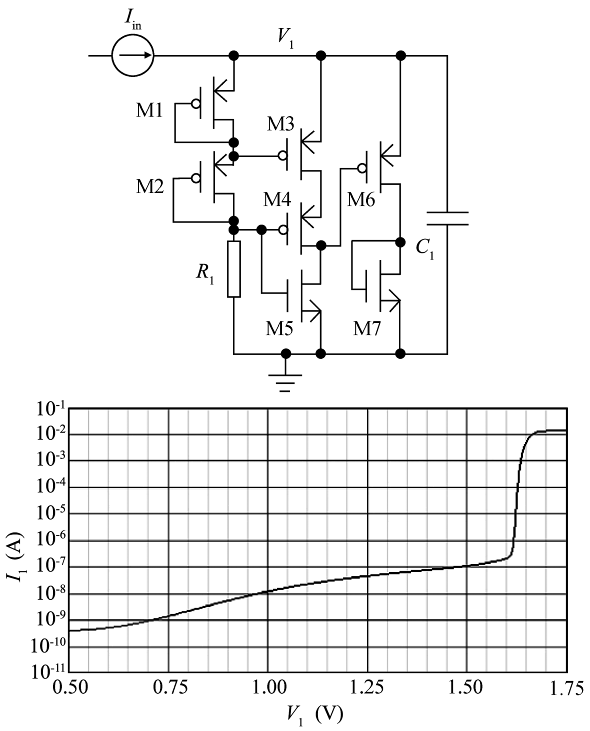


Fig. 4. Coarse bypass current I_1 circuit.

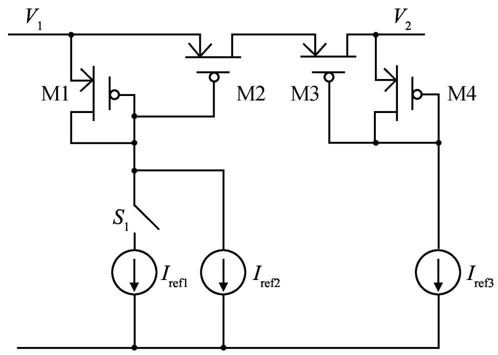


Fig. 5. Constant current I_2 circuit.

1.6 V. The value of I_2 is set at 35 μA. I_3 is another current bypass path to conduct the excess current. Hence V_2 is given by

$$V_2 = (I_2 - I_3)R_{\rm Load}. \tag{1}$$

I_3 as a function of V_2 is given by

$$I_3 = g_{\rm m}(V_2 - V_{\rm Ref}), \tag{2}$$

where $V_{\rm ref}$ is 1.2 V. By comparing Eqs. (1) and (2) we can get

$$V_2 = \frac{I_2 R_{\rm Load} + g_{\rm m} R_{\rm Load} V_{\rm Ref}}{1 + g_{\rm m} R_{\rm Load}} \approx V_{\rm Ref}. \tag{3}$$

If $g_{\rm m} R_{\rm Load}$ is large, V_2 is almost equal to $V_{\rm Ref}$.

2.1. Coarse parallel regulator I_1

Figure 4 illustrates the detailed circuit of I_1. I_1 is a coarse voltage clamp to dissipate excess current. R_1 is about 2 MΩ. When V_1 exceeds about $2V_{\rm thp} + V_{\rm thn}$, the current in M6 increases sharply. The standby current is several hundreds of nA. The voltage-to-current gain is highly increased by adding the inverter formed by M4 and M5.

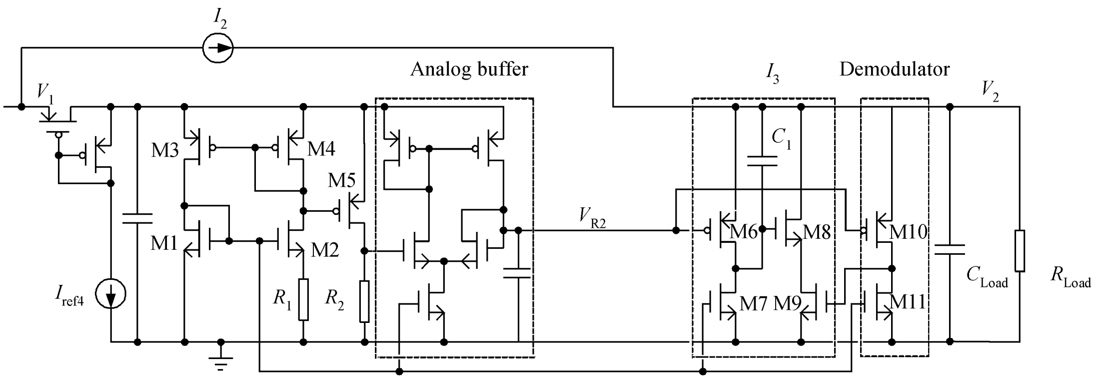


Fig. 6. Bypass current I_3 circuit.

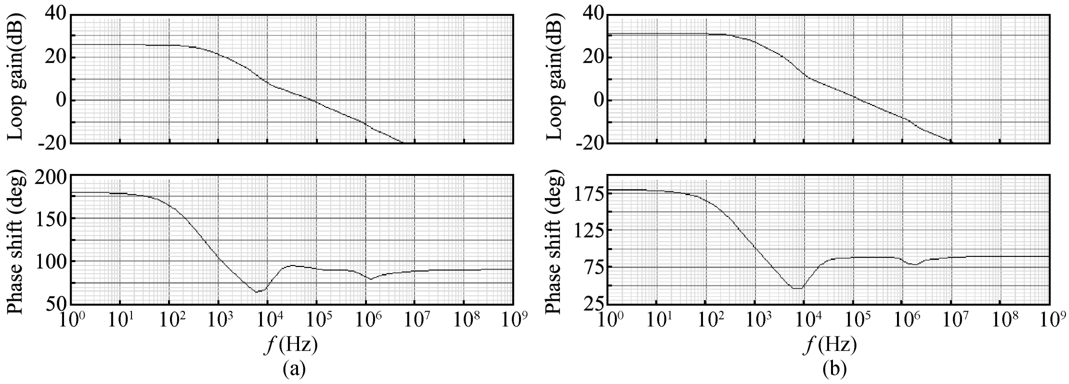


Fig. 7. Simulation results of circuit loop gain and phase shift. (a) $R_{\rm Load}$ = 60 kΩ. (b) $R_{\rm Load}$ = 600 kΩ.

2.2. Constant current source I_2

The circuit of I_2 is shown in Fig. 5. There are two current sources $I_{\rm ref1}$ and $I_{\rm ref2}$ connected with the diode-connected PMOS transistors to control the passing current. When there is no RF energy or the tag sends data by connecting the antenna to the ground, V_1 will drop below V_2 due to bypass current I_1. Hence, a low voltage loss switch formed by M3 and M4 is inserted between V_1 and V_2 to prevent the current flowing back to I_1. As V_1 rises above V_2, the equivalent resistor of M3 is reduced by decreasing the M3 gate voltage. The voltage drop across M3 is much smaller than the diode or diode-connected MOS transistor. $I_{\rm ref1}$ is generated by power supply V_1 and $I_{\rm ref2}$ is generated by V_2. At the initial state when the tag firstly enters the reader interrogation area and begins receiving RF power, $I_{\rm ref2}$ may be zero. As a result $I_{\rm ref1}$ gives I_2 an initial value to provide energy for the storage capacitor. After V_2 is stabilized and $I_{\rm ref2}$ is started up, the switch S_1 is open to block $I_{\rm ref1}$ variations induced from unregulated V_1. $I_{\rm ref1}$ and $I_{\rm ref2}$ are several dozen nA to reduce the power. The current I_2 is enlarged by the W/L ratio of PMOS transistors M1 and M2.

2.3. Fine parallel regulator I_3

Figure 6 shows the fine parallel regulator I_3. M6–M9 form a main bypass current path. M10 and M11 constitute a demodulator to accelerate the closure of the current path in M8 when there is no power available for the tag. When V_2 exceeds $V_{\rm Ref} = V_{\rm R2} - V_{\rm GS6}$, M8 is turned on and draws huge current to keep V_2 equal to $V_{\rm Ref}$. $V_{\rm R2}$ is generated from another power supply and it is given by

$$V_{\rm R2} = \frac{\alpha\zeta R_2 V_{\rm T}}{R_1}\ln\frac{(W/L)_2}{(W/L)_1}, \tag{4}$$

where $\zeta > 1$, $\alpha = (W/L)_5/(W/L)_4$ and $V_{\rm T} = KT/q$. As a result, $V_{\rm R2}$ is a positive-temperature coefficient voltage. Because M6 works in the sub-threshold region $V_{\rm GS6}$ can be approximated by[4]

$$V_{\rm GS6}(T) \approx V_{\rm GS6}(T_0) + K_{\rm G}\left(\frac{T}{T_0} - 1\right), \tag{5}$$

where $K_{\rm G}$ is positive. Therefore, the following condition is satisfied to obtain a zero-temperature coefficient $V_{\rm Ref}$:

$$\frac{K_{\rm G}}{T_0} = \frac{\alpha\zeta R_2 K}{R_1 q}\ln\frac{(W/L)_2}{(W/L)_1}. \tag{6}$$

By breaking the loop at M8 gate, the loop gain can be calculated as

$$\mathrm{LG} \approx g_{\rm m8}g_{\rm m6}r_{\rm ds7}R_{\rm Load}\frac{1 + C_1 s/g_{\rm m6}}{(1 + r_{\rm ds7}C_1 s)(1 + R_{\rm Load}C_{\rm Load}s)}. \tag{7}$$

There are two poles:

$$p_1 = -1/R_{\rm Load}C_{\rm Load}, \tag{8}$$

$$p_2 = -1/r_{\rm ds7}C_1. \tag{9}$$

Table 1. Comparison of performances between the proposed and referenced regulators.

Parameter	Technology (μm)	Efficiency	Bandwidth (kHz)	Current consumption (nA)	Regulated voltage (V)
Ref. [2]	0.15	N/A	20–90	110	1.15–1.35
Proposed	0.18	86%	100	1000	1–1.3

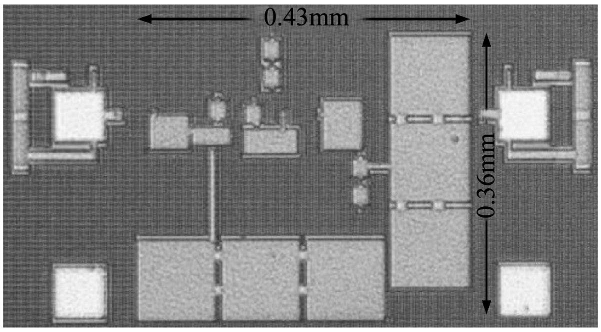


Fig. 8. Die photograph (die size 0.43 × 0.36 mm^2).

C_1 is added to move p_2 to the low frequency region. Clearly p_2 can be compensated by a left-plane zero near p_2 expressed as

$$z_1 = -g_{m6}/C_1. \tag{10}$$

So the system is stable with only one pole. Figure 7 shows the simulation results of loop gain and phase shift with constant current I_2 of 35 μA and C_{Load} of 300 pF. The system stability is enhanced when R_{Load} reduces because of the further p_2 and p_1 separation. A bandwidth of 100 kHz is achieved for fast supply voltage recovery.

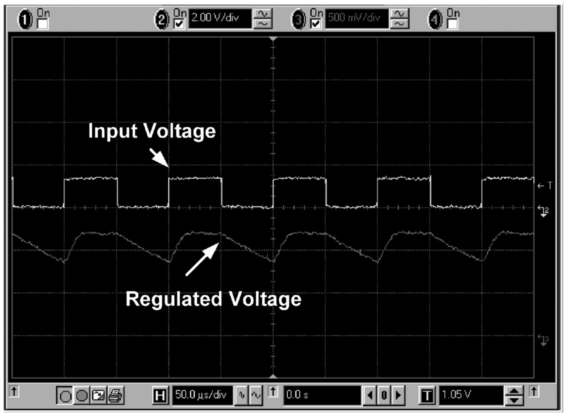
3. Measurement results

The whole circuit is fabricated in UMC 0.18 μm mixed-mode CMOS technology. The die photo is shown in Fig. 8 and the chip area is 0.43 × 0.36 mm^2.

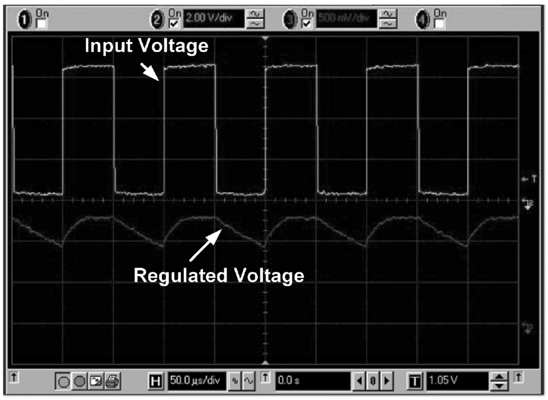
Figure 9 shows the transient response of the regulator to the input current from 0 to 3 μA and 0 to 6 mA at 10 kHz with R_{Load} of 600 kΩ and C_{Load} of 300 pF. Clearly the voltage drops slowly for little leakage current consumption. The measurement results show the regulated voltage variation is around 1.15 V of ± 0.15 V across a temperature range of –20 to 80 ℃ with 2 μA to 2 mA input current. The current consumption of the regulator is only 1 μA. Table 1 compares the performances between the proposed and referenced regulators.

4. Conclusions

A current-mode voltage regulator is developed to converting the rectified LF power into a stable voltage supply. The output of the proposed regulator is clamped at 1.2 V by an accurate control of the rectified current flowing through the load with an embedded sub-threshold reference, and a bandwidth of about 100 kHz is achieved. The regulator is fabricated in UMC



(a)



(b)

Fig. 9. Measurement voltage waveforms of input and regulated voltages. (a) Input current 0–3 μA. (b) Input current 0–6 mA.

0.18 μm mixed-mode CMOS technology with 1 μA current consumption.

References

[1] Karthaus U, Fischer M. Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power. IEEE J Solid-State Circuits, 2003, 38(9): 1602

[2] Balachandran G K, Barnett R E. A 110 nA voltage regulator system with dynamic bandwidth boosting for RFID systems. IEEE J Solid-State Circuits, 2006, 41(8): 2019

[3] De Vita G, Iannaccone G. Ultra-low-power series voltage regulator for passive RFID transponders with subthreshold logic. Electron Lett, 2006, 42(23): 1350

[4] Huang P H, Lin H, Lin Y T. A simple subthreshold CMOS voltage reference circuit with channel-length modulation compensation. IEEE Trans Circuits Syst II: Express Briefs, 2006, 53(8): 882