A 5-GHz programmable frequency divider in 0.18-μm CMOS technology*

Shu Haiyong(舒海涌)[1,2] and Li Zhiqun(李智群)[1,2,†]

(1 Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)
(2 Engineering Research Center of RF-ICs & RF-Systems, Ministry of Education, Southeast University, Nanjing 210096, China)

Abstract: A 5-GHz CMOS programmable frequency divider whose modulus can be varied from 2403 to 2480 for 2.4-GHz ZigBee applications is presented. The divider based on a dual-modulus prescaler (DMP) and pulse-swallow counter is designed to reduce power consumption and chip area. Implemented in the 0.18-μm mixed-signal CMOS process, the divider operates over a wide range of 1–7.4 GHz with an input signal of 7.5 dBm; the programmable divider output phase noise is –125.3 dBc/Hz at an offset of 100 kHz. The core circuit without test buffer consumes 4.3 mA current from a 1.8 V power supply and occupies a chip area of approximately 0.015 mm^2. The experimental results indicate that the programmable divider works well for its application in frequency synthesizers.

Key words: frequency divider; dual-modulus prescaler; pulse-swallow; frequency synthesizer
DOI: 10.1088/1674-4926/30/5/055004 **EEACC:** 1265B; 1280; 2570D

1. Introduction

ZigBee (IEEE 802.15.4) is an industry standard for short range, low cost, low power and low bit rate wireless applications. It covers sixteen channels within the 2.4 GHz unlicensed ISM band with a channel spacing of 5 MHz[1]. Frequency synthesizers (FS) based on a phase-locked loop (PLL) are widely used to generate local oscillation (LO) signals in modern communication systems. Wherever frequencies are translated, an FS is crucial to provide a clean, stable, and programmable LO signal.

The most difficult challenge for increasing the operating frequency of an FS at a given technology node is the realization of a programmable frequency divider (especially DMP) with a sufficient maximum operating frequency. Meanwhile, the input sensitivity of the divider must be about 300 mV or less, since that is what can be reasonably expected from an on-chip oscillator operating from a low supply voltage of 1.8 V. In order to cover the required-carries and operate from an input frequency of approximately 5 GHz, the modulus of the divider has to be programmed from 2403 to 2480 while the reference frequency is set to be 2 MHz. In-phase and quadrature (IQ) 2.4 GHz signals are generated by a frequency divider (/2) at the output of VCO.

Current high-speed frequency dividers fall into three categories: (1) flip-flop-based frequency dividers, (2) injection-locked frequency dividers (ILFDs), and (3) regenerative frequency dividers.

ILFDs employ an oscillator whose center frequency is locked to a harmonic of the incoming signal frequency[2,3]. Usually they can reach millimeter wave frequency, anywhere from GHz up to tens of GHz while dissipating low power. However, the operating bandwidth is fairly narrow due to the nature of this architecture.

Regenerative frequency dividers are realized by placing a mixer and a low-pass filter in a closed-loop feedback[4,5]. They can operate in a wider lock range at very high frequencies compared to an injection-locked counterpart, but utilize many passive components in the process which is a disadvantage from overall chip-area and circuit matching considerations.

Flip-flop-based frequency dividers are the most popular structure when the operating frequency is below 20 GHz. In recent years, many kinds of high-speed flip-flops have been reported, and they can be generally categorized into three groups: true-single-phase-clocked (TSPC) dynamic flip-flops[6], current-mode-logic (CML) master-slave (MS) flip-flops[7] and pseudo-differential MS flip-flops[8].

This paper focuses on the design of a DMP and a pulse-swallow counter to reach the required divider modulus and make the divider work well for its application in the frequency synthesizer of a ZigBee RF transceiver. First, the chosen architecture of the programmable divider is introduced. Then, the design, realization and some key circuit techniques of the programmable divider are discussed. The next section deals with the layout and implementation of the circuit.

2. Architecture and design

Figure 1 shows the proposed divider architecture based on pulse-swallow topology. The prescaler initially divides the high frequency input signal by N+1 with the modulus control (MC) set to LOW. After the swallow-counter counts S output pulses from the DMP, it changes the MC to HIGH, and the DMP starts to divide by N. The output of the DMP is also counted by the pulse counter simultaneously. Therefore, the total division ratio (M) is given by

$$M = (N+1)S + N(P-S) = NP + S, \qquad (1)$$

where P is the number of the pulse counter, and S is the number of the swallow counter.

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z2A7) and the Science and Technology Program of Zhejiang Province, China (No. 2008C16017).
† Corresponding author. Email: zhiqunli@seu.edu.cn
Received 9 November 2009, revised manuscript received 23 December 2009

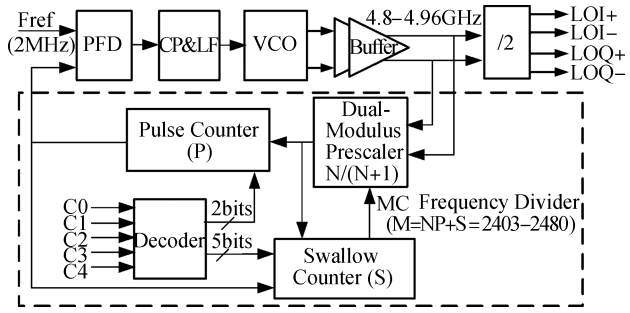

Fig. 1. Block diagram of the frequency synthesizer and the proposed programmable divider.

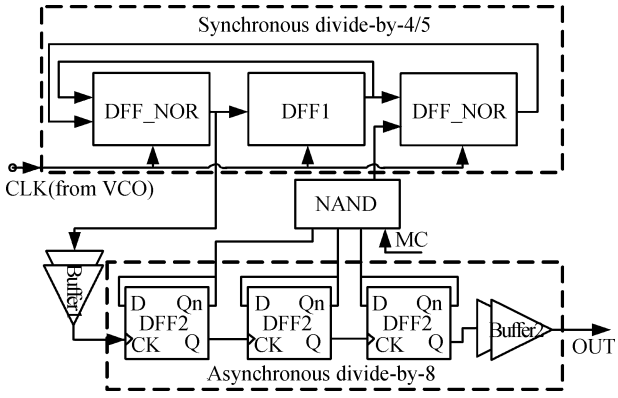

Fig. 2. Block diagram of the 32/33 DMP.

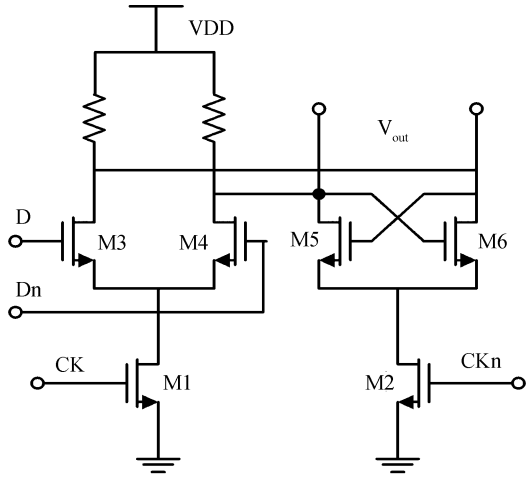

Fig. 3. Pseudo-differential latch..

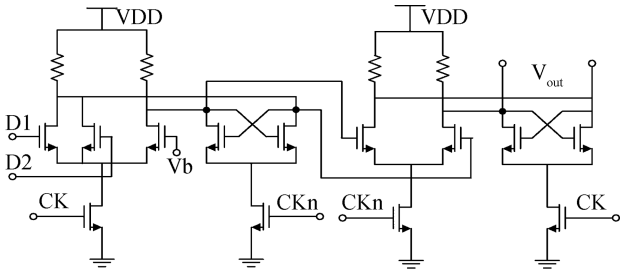

Fig. 4. Merged DFF and NOR gate (DFF_NOR).

IEEE 802.15.4 specifies 16 channels within the 2.4 GHz band, in 5 MHz steps, numbered 11 through 26. The RF frequency of channel k is given by[1]

$$\mathrm{FC} = 2405 + 5(k-11)\,\mathrm{MHz}, \quad k = 11, 12, ..., 26. \quad (2)$$

In receive mode the actual LO frequency is FC – 2 MHz, since a 2 MHz IF is used. Direct conversion is used for transmission, so here the LO frequency equals FC. The total division ratio should cover the following frequency division:

$$M = 2405\,(\mathrm{or}\,2403) + 5(k-11), \quad k = 11, 12, ..., 26. \quad (3)$$

According to Eqs. (1) and (3), P is set to be from 75 to 77, S is set to be from 0 to 31, while N is set to be 32, so the total division ratio is from 2400 to 2495 with a step of 1. Noting that only 32 values of frequency division ratio are required, the operating frequency is set by programming the 5 bit frequency word. A decoder is utilized to convert the 5 bit frequency word to the corresponding P and S.

2.1. Dual-modulus prescaler (DMP)

The proposed DMP divided-by-32/33 is constructed with two parts: a synchronous divide-by-4/5 and a cascaded asynchronous divide-by-8 as shown in Fig. 2. In such a topology, the synchronous divider is the only part of the circuit operating at the maximum frequency. The rest of the circuit runs at maximum one-fourth of the input frequency. The overall prescaler ratio is 32 or 33, depending on the level of the modulus control (MC) signal.

Synchronous divide-by-4/5: This consists of three DFFs and two NOR gates working at the highest frequency and therefore consumes significant power. To improve the operating speed of the synchronous divide-by-4/5, we used four techniques.

First, pseudo-differential MS flip-flops are used for DFF to enable high-speed operation while providing large output swing. The pseudo-differential MS flip-flops are different from the conventional SCL frequency divider in that the tail current source is removed. This improves the performance of the circuit when operating at a low supply voltage. The pseudo-differential MS flip-flops are cascaded by two pseudo-differential latches as shown in Fig. 3. The two bottom NMOS transistors (M1, M2) are utilized as the current switch. The transistors M3–M6 in the latches data path are of the same size and 1/2 the width of M1–M2 (clock transistors). These larger clock devices are used to increase the input sensitivity.

Second, the DFF and the NOR gates are merged (called DFF_NOR in Fig. 2) to reduce additional gate delays[8]. This leads to a higher operating speed compared to the conventional topology, and at the same time the power consumption is reduced. This principle is shown in Fig. 4. The voltage V_b is biased at the midway between the high and low levels of inputs D1 and D2.

Third, the voltage V_b uses filtering technology. The circuit that sets up V_b ($V_{\mathrm{b}1}$, $V_{\mathrm{b}2}$) on-chip is shown in Fig. 5. The MOS capacitances are used for filtering spurs on V_b, which could keep the voltage V_b more stable. The simulated waveform of the voltage V_b is shown in Fig. 6. As can be seen, the peak

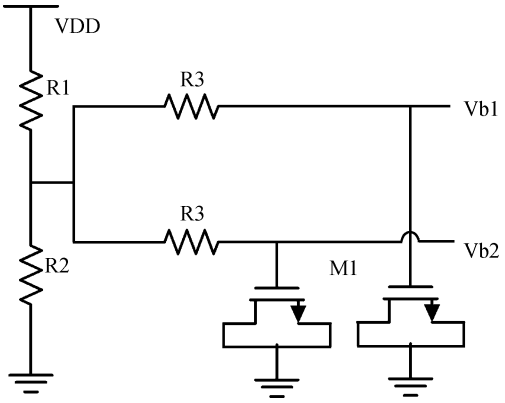

Fig. 5. Bias circuit of V_b.

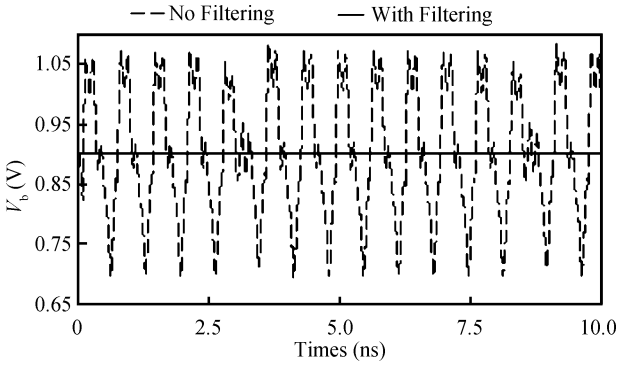

Fig. 6. Waveform of the voltage V_b.

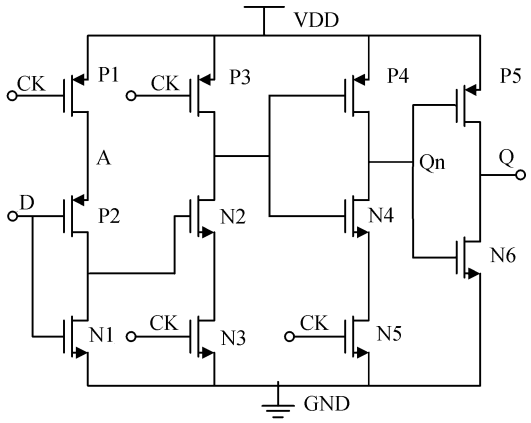

Fig. 7. Circuit diagram of TSPC DFF.

to peak ripple voltage decreases from 0.35 V to no more than 1 mV when the filtering capacitances are adopted. In addition, the simulation results indicate that the maximum operating frequency of the circuit is improved from 9.4 to 10.8 GHz with the input signal of –4 dBm.

Fourth, the symmetrical layout is used to ensure correct differential operation. Because the two clock current switch transistors are independent, fully complementary clock signals are needed. The dummy devices are used to eliminate the possible mismatch. Moreover, to reduce the parasitic capacitance, a high sheet resistance poly silicon resistor without a silicide layer is used.

Asynchronous divide-by-8: The divide-by-8 circuit is cascaded with three divide-by-2 circuits which operate at different frequencies, each divide-by-2 circuit must be designed and optimized carefully. Since the asynchronous divide-by-8 works at a lower frequency and high speed is not required, the optimization of DFF in this stage is focused on the reduction of power consumption.

Compared with static DFF, dynamic TSPC topology leads to lower power, far fewer transistors and less sensitivity to layout and process variations, so in the divide-by-8 circuit, a kind of TSPC DF[14] shown in Fig. 7 (called DFF2 in Fig. 2) is used. In order to meet the large input voltage required by TSPC, an inverter amplifier is inserted as an input buffer (Buffer1 shown in Fig. 2) in front of the asynchronous divide-by-8.

CMOS inverters are used to buffer the 32/33 DMP output (Buffer2 as shown in Fig. 2). The buffer can provide about 0.3 Vpp across a 50-Ω load. Broad-band matching for the clock inputs is realized with 225 Ω and 180 Ω on-chip resistors, which also act as a DC level shifter and ESD protection. This input DC level shifter was optimized for fast switching.

When no signal is applied at the input, the DMP behaves like a ring oscillator with an output self-oscillation frequency of 173.75 MHz (MC is set to HIGH). Referred to the input the self-oscillation frequency is 5.56 GHz, and this frequency corresponds to the minimum point of the sensitivity curve.

2.2. Pulse-swallow counter

In this paper, the DMP is used to reduce the input operation frequency of the sequential pulse-swallow counter (PS_counter), while the aim of the pulse-swallow counter is to acquire a series of continuous division radios by working together with DMP. The pulse-swallow counter is designed based on the Artisan 0.18-μm standard cell library. The use of a standard cell library offers shorter design time, induces fewer errors in the design process, and is easier to maintain. First, the function is realized in Verilog HDL. Then we use a synthesis tool Synopsys Design Compiler® (DC) to synthesize the design. The next steps are auto place and routing (P&R), which are back-end design and can be completed in Astro™. By importing the layout information from Astro™ into Cadence Virtuoso, we use Cadence Assura and Mentor Calibre to perform the design rule check (DRC) and layout-vs-schematic (LVS) and to verify the correctness of the design. After combining with the DMP circuits, we use Assura RCX to extract RC parameters to do the transient analysis in Cadence Spectre. The transient analysis results are shown in Fig. 8. Here, M is set to be 2448 before 1 μs and to be 2443 from 1 to 2 μs while the frequency of the input clock is 6.5 GHz. According to the figure, we can see that the period of the output is 376.6 ns and 376 ns respectively.

3. Layout and implementation

Layout plays an important role in increasing the operating frequency of the circuit. Every effort was made to compact the layout and keep the parasitic capacitances and resistances as small as possible. Because of differential structure of the pseudo-differential DFF, the symmetrical layout is necessary. 45° metal lines can be adopted to shorten the lines, and hence minimize their parasitic effect. On-chip bypassing is provided

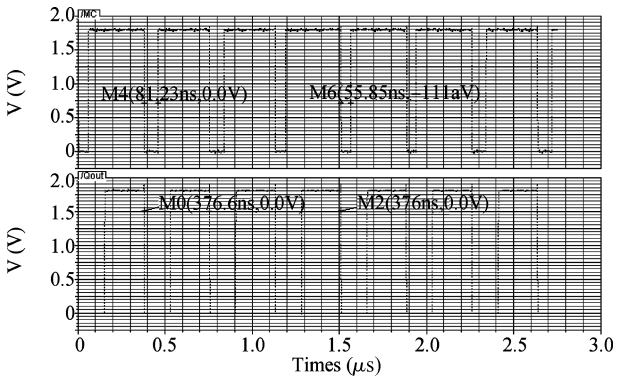

Fig. 8. Transient simulation waveforms of the programmable divider.

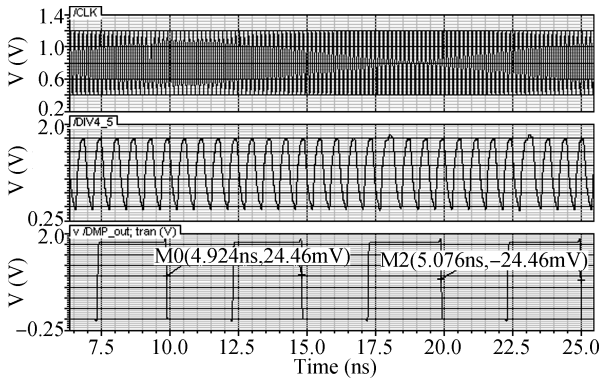

Fig. 10. Transient simulation waveforms of the 32/33 DMP.

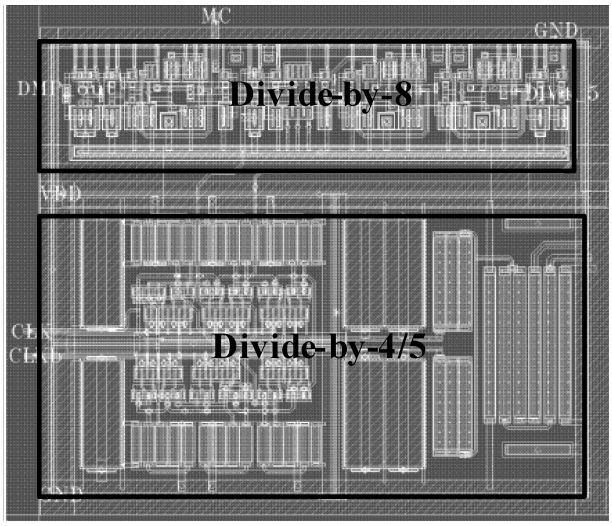

Fig. 9. Chip layout of the 32/33 DMP.

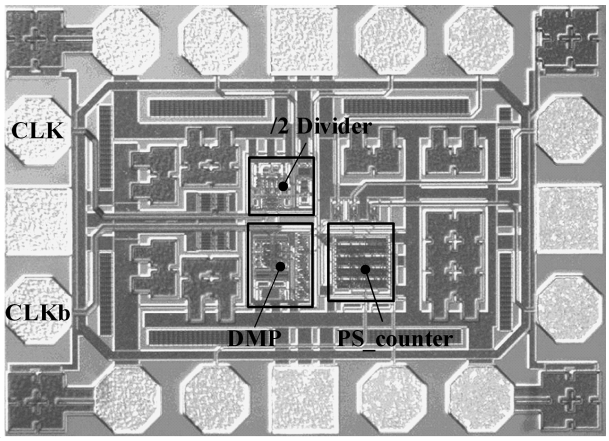

Fig. 11. Die microphotograph of the frequency divider.

using MOS or MIM capacitors. The chip layout of the 32/33 DMP is shown in Fig. 9.

In the post-layout simulations, for PVT conditions, the proposed 32/33 DMP achieves a maximum operating frequency of 7 GHz and consumes about 3.8 mA. Figure 10 shows the transient simulation waveforms of the 32/33 DMP. Before the time of 15 ns, MC = 1, the DMP operates in divide-by-32 mode, After that, the DMP operates in divide-by-33 mode, while the frequency of the input signal is 6.5 GHz and the process corner is set to be SS (slow/slow corner). According the figure, we can see the period of the output is 4.923 ns and 5.076 ns respectively.

The proposed programmable frequency divider was manufactured by 0.18-μm CMOS 1P6M technology. The die microphotograph is shown in Fig. 11. The chip size including the pad is 0.475 × 0.675 mm^2 (including another divide-by-2 frequency divider of the FS), while the core size of the programmable divider circuit is only approximately 0.015 mm^2.

4. Measurement results

The performance of the fabricated programmable divider was evaluated on wafer by employing a Cascade Microtech probe station. The differential inputs were provided using a hybrid. The output was monitored on an oscilloscope and a spectrum analyzer.

Figure 12 shows the measured transient output signal of 2 MHz with an input signal of 4.96 GHz while the total division ratio is set to be 2480. The measured output voltage swing on an external 50 Ω load is about 550 mV$_{pp}$, and the spur on the transient waveform is caused by coupling between the DMP output buffer and the adjacent programmable divider output buffer. The measured phase noise is –125.3 dBc/Hz at 100 kHz offset as shown in Fig. 13. Figure 14 shows the divider input sensitivity as a function of the input divider frequency measured with a Rohde-Schwarz SMP04 signal generator and an Agilent E4440A frequency analyzer at 1.8 V VDD. The measured results demonstrate the proposed frequency divider with a wide operating range from 1 to 7.4 GHz. The lack of sensitivity below 1 GHz is caused by the limited slew rate of the sinusoidal input signal. At low frequencies a square wave signal should be applied. The sensitivity curve has a minimum corresponding to the self-oscillation of the DMP. The core part of the divider only draws 4.3 mA from the 1.8 V power supply.

The performance of the proposed divider is summarized in Table 1 with several recently published programmable dividers for comparison. All the designs are implemented in CMOS technology.

5. Conclusion

The design and performance of a low-power high-speed CMOS programmable frequency divider have been presented.

Table 1. Performance comparison with other published programmable frequency dividers.

Ref.	Tech. (μm)	$f_{min}-f_{max}$ (GHz)	Area (mm^2)	VDD (V)	Power (mA)	Division range
Ref. [10], 2000	0.25	N/A–5.3	0.09	1.8	17.4	220–224
Ref. [11], 2006	0.09	N/A–4.7	0.083	1.2	2.3	64–127
Ref. [12], 2007	0.18	5.15–5.825	0.285	1.8	2.0	257–294
Ref. [13], 2007	0.18	N/A–3.5	0.10	1.8	8.7	8–510
Ref. [14], 2008	0.35	N/A–2.6	0.195	3.3	17	128–255
Ref. [15], 2008	0.09	N/A–3.5	0.02	1.0	4.5	24–27
Ref. [16], 2008	0.18	1.4–7.55	0.007	1.8	6.1	8–255
This work	0.18	1.0–7.4	0.015	1.8	4.3	2403–2480

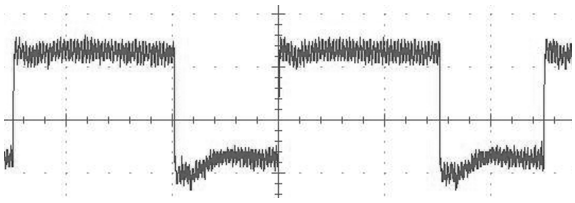

Fig. 12. Output waveform of the programmable frequency divider.

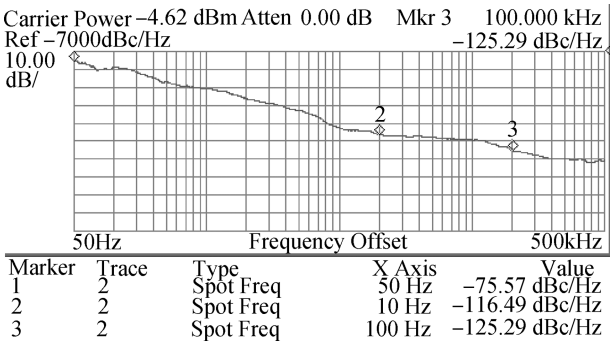

Fig. 13. Measured phase noise of the programmable frequency divider.

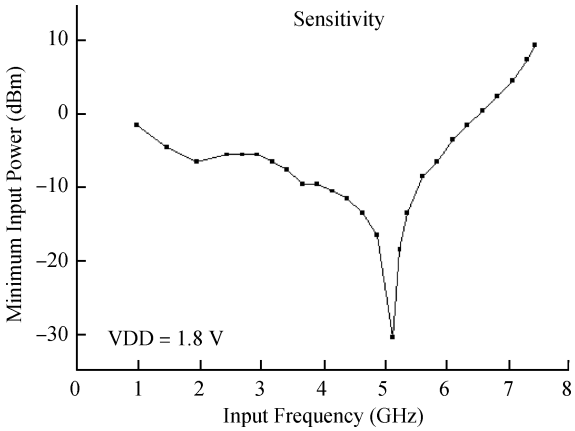

Fig. 14. Measured input sensitivity characteristic of the frequency divider.

The measurement results show that the frequency divider can operate reliably over a wide range of 1–7.4 GHz with a power consumption of less than 4.3 mA, while taking up an area of 90×170 μm^2 and being suitable for application in RF receiver systems.

References

[1] IEEE std. 802.15.4-2003: wireless medium access control (MAC) and physical layer (PHY) specifications for low rate wireless personal area networks (LR-WPANs), 2003

[2] Lin B Y, Tsai K H, Liu S I. A 128.24–137.00 GHz injection-locked frequency divider in 65 nm CMOS. International Solid-State Circuits Conference, USA, 2009: 282

[3] Yin Jiangwei, Li Ning, Zheng Renliang, et al. Low-power wide-locking-range injection-locked frequency divider for OFDM UWB systems. Journal of Semiconductors, 2009, 30(5): 055003

[4] Wallin T, Hellen J, Berg H, et al. Regenerative frequency divider SiGe-RFIC with octave bandwidth and low phase noise. Microwave Integrated Circuit Conference, 2008: 322

[5] Momeni O, Sengupta K, Hashemi H. Regenerative frequency divider with synchronous fractional outputs. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2007: 717

[6] Arguello A M G, Navarro J, van Noije W. A 3.5 mW programmable high speed frequency divider for a 2.4 GHz CMOS frequency synthesizer. IEEE 18th Symposium Integrated Circuits and Systems Design, 2005: 144

[7] Wohlmuth H D, Kehrer D. A 24 GHz dual-modulus prescaler in 90 nm CMOS. IEEE International Symposium on Circuits and Systems, 2005: 3227

[8] Tang Lu, Wang Zhigong, He Xiaohu, et al. Low jitter, dual-modulus prescalers for RF receivers. Chinese Journal of Semiconductors, 2007, 28(12): 1930 (in Chinese)

[9] Oguey H, Vittoz E. CODYMOS frequency dividers achieve low power consumption and high frequency. IEEE Electron Lett, 1973, 9: 386

[10] Krishnapura N, Kinget P. A 5.3-GHz programmable divider for HiPerLAN in 0.25 μm CMOS. IEEE J Solid-State Circuits, 2000, 35(7): 1019

[11] Ali M, Hegazi E. A multigigahertz multimodulus frequency divider in 90-nm CMOS. IEEE Trans Circuits Syst II, Express Briefs, 2006, 53(12): 1333

[12] Kuo Y F, Weng R M. A dynamic-logic frequency divider for 5-GHz WLAN frequency synthesizer. 17th International Conference Radioelektronika, 2007, 1: 403

[13] Zhang M, Islam S K, Haider M R. Efficient driving-capability programmable frequency divider with a wide division ratio range. IET Circuits, Devices & Systems, 2007, 1(6): 485

[14] Li Zhiqiang, Chen Liqiang, Zhang Jian, et al. A programmable 2.4 GHz CMOS multi-modulus frequency divider. Journal of Semiconductors, 2008, 29(2): 224 (in Chinese)

[15] Barale F, Sen P, Sarkar S, et al. Programmable frequency-divider for millimeter-wave PLL frequency synthesizers. 38th European Microwave Conference EuMC, 2008: 460

[16] Sleiman S B, Atallah J G, Rodriguez S. Wide-division-range high-speed fully programmable frequency divider. Circuits and Systems and TAISA Conference, 2008: 17