A novel embedded soft-start circuit for SOC power supply

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Abstract: To improve the power sequencing performance of the system-on-a-chip (SOC), a novel embedded soft-start circuit is presented. A seamless soft-start reference voltage is obtained with 7 bits DAC, which can not only restrain the turning point overshoot, but also improve the output accuracy and the poor loading capability, reduce the pin number and save PCB area. The whole DC–DC converter has been fabricated in a 0.35 μm CMOS process. The measurement results show that the chip starts up successfully with 250 μs soft-start time under conditions of 400 kHz switching frequency, 2.5 V DC–DC output and 1.8 V LDO output. Stable operation after soft-start is also shown.

Key words: SOC; current mode converter; soft-start; loading capability
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1. Introduction

In recent years, System-on-a-chip has been in great demand for electric devices, such as wireless communications, industrial controls, video controls and some other fields. I/O driver power, dynamic power management and power circuits, which need both digital and analog power supplies, have played a more important role in SOC. Power management is a timely and essential research area, enabling the advancement of SOC technology. The development of high-performance integrated voltage regulators, in terms of power sequencing, output accuracy, silicon area, response time, and an off-chip component free feature, is undoubtedly vital to the success of SOC. Preventing initial inrush current and voltage spikes from causing damage to systems is an important issue for DC–DC converters. Conventionally, we use one capacitor to generate a gently ramping signal for a DC–DC converter to implement soft-start during start-up. In LDOs, the requirements for soft-start are usually determined by the application. In portable universal serial bus (USB) applications, there are stringent requirements imposed by the USB standard on the maximum current that the USB power bus can source. When the USB is simultaneously powering numerous LDOs, an overcurrent condition could occur on the USB power bus, ultimately resulting in system faults (e.g., resets) due to inrush currents during the power-up transient. Therefore, each LDO on the USB power bus should be soft-started upon enabling to avoid the overcurrent condition.

Though the conventional soft-start reduces the damage resulting from inrush current, an over-voltage or drop-voltage situation may still occur[1, 2]. For example, voltage spikes will occur when the domination of the converter is changing between the start-up mode and normal operation. In addition, we will consume one external pin for the soft-start capacitor because this capacitor is too large to be on chip. Also, there has some other research, such as Refs. [4, 5], which added the soft-start slope voltage to the pulse width modulator comparator and error amplifier. But there are also three problems: First, the turning point from the soft-start signal to the error amplifier output signal is not smooth in some applications, which can induce an inrush inductor current. Second, if the soft-start time is becoming longer, the loading capability of the converter will be affected obviously, which is mainly because the converter cannot achieve the nominal load during the long soft-start. Third, the compound amplifier or comparator will reduce the output voltage accuracy. The aim of our project is to find a solution to the above problems.

In this paper, the proposed soft-start circuit does not need an extra pin-out, a compound structure, and it improves the output voltage accuracy and loading capability of the converter. The design of the power supply with excellent embedded soft-start was fabricated in a 0.35 μm CMOS process. The measurement results show that the soft-start circuit has good performance and can be used for SOC blocks such as processor, memory, DSP, RF, SRAM and ADDA.

2. Power supply system design

A diagram of the power supply system with the peak current mode DC-DC converter and LDO is shown in Fig. 1. Through sinking the current controlled by 7 bits DAC from the band-gap reference voltage, the reference voltage of the system starts up softly, and then the output voltage soft-start is obtained. Current and voltage loop stability is achieved by linear slope compensation and the cancellation of pole-zero at the output of the error amplifier respectively. Also, there are the current sense and the zero current detect circuit, to realize current mode controlling and high conversion efficiency. In the low dropout regulator, the soft-start reference voltage is obtained through a buffer to reject the noise from the switching converter. The output of the regulator will start softly depending on the soft-start reference voltage. At the same time, the output mode can be selected by the $V_{\rm LFB}$ voltage in order to save the PCB board. When the $V_{\rm LFB}$ voltage is below 100 mV or is grounded, the regulator selects the fixed mode, and the output voltage is determined only by the internal fixed resistor divider. Meanwhile, we can get different voltages by the trimming solution. Certainly, the output can also be adjusted

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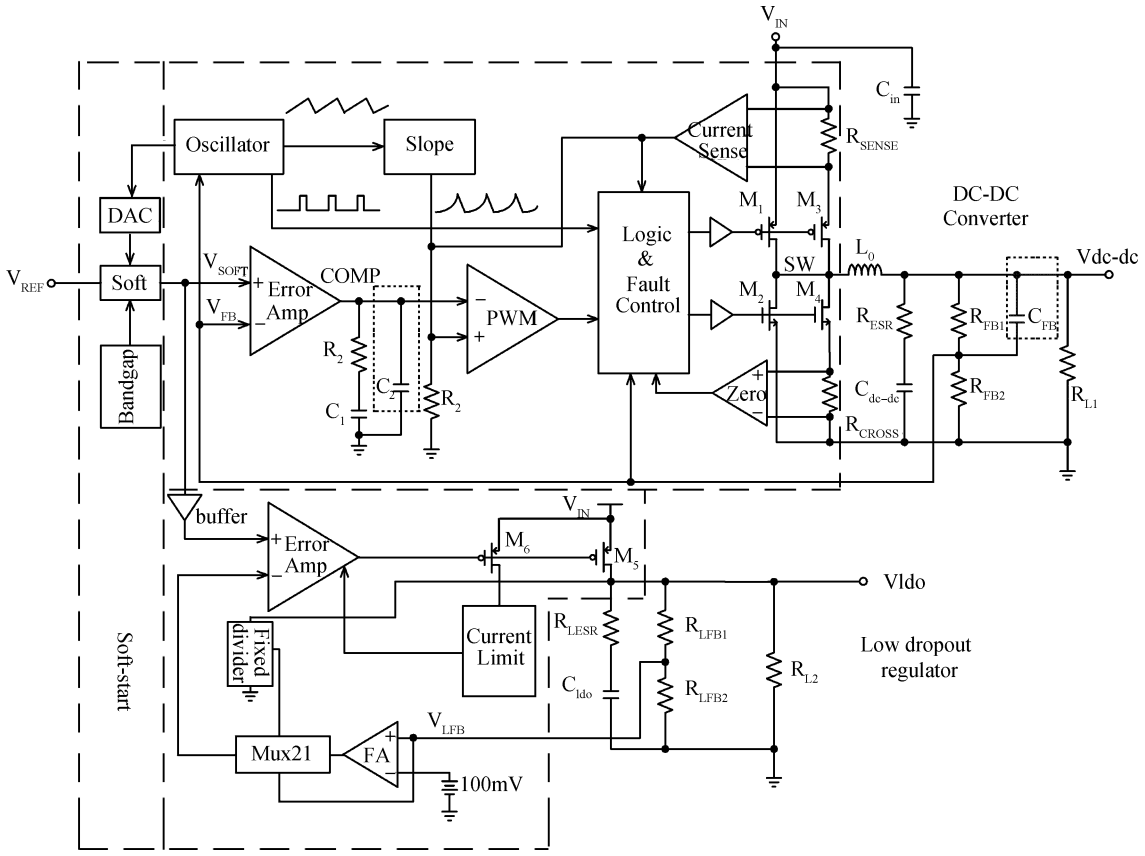


Fig. 1. Diagram of the power supply.

by the divider easily when the $V_{\rm LFB}$ pin connects to the external resistor divider. These functions are achieved through the FA comparator. Finally, the current limit block is to limit the current through the pass transistor[6–8]. The fault control unit, including over-temperature protection, over-voltage protection, under-voltage protection and so on, protects the system beyond the recommended operating conditions.

3. Traditional soft-start circuit

Some soft-start circuits have been reported in Refs. [1, 2–5, 9–13] as summarized in Figs. 2(a), 2(b) and 2(c). Figure 2(a)[1–3] shows the most common and simplest soft-start circuit, where the soft-start function is realized by charging the off-chip capacitor with the on-chip constant current. The soft-start time is calculated from the system starting to work to the $V_{\rm SOFT1}$ equal to $V_{\rm REF}$, where $V_{\rm SOFT1}$ is the voltage across the off-chip capacitor, and $V_{\rm REF}$ is the internal reference voltage. So the soft-start time can be calculated by:

$$t_{\rm soft1} = \frac{C_{\rm SOFT1} V_{\rm REF}}{I_{\rm C}}, \tag{1}$$

where $I_{\rm C}$ is the charging current referred to above. From Eq. (1), we can see that the soft-start time can be accurately controlled because $V_{\rm REF}$ and $I_{\rm C}$ are designed with high precision. The disadvantage of this method is the off-chip capacitor. If a long soft-start time is needed, this will increase the PCB board area. Therefore, in order to reduce the PCB board space, improved methods are shown in Figs. 2(b) and 2(c). In Fig. 2(b)[4], $V_{\rm SOFT2}$ is obtained by charging the capacitor $C_{\rm SOFT2}$ with the DAC controlled current during the soft-start time. The compound error amplifier amplifies the differential voltage between $V_{\rm FB}$ and the smaller one of $V_{\rm REF}$ and the $V_{\rm SOFT2}$ voltage. Once $V_{\rm SOFT2}$ is greater than $V_{\rm REF}$, there is a detecting comparator to switch the comparison point from $V_{\rm SOFT2}$ to $V_{\rm REF}$, then the turning point spur is induced by the detecting circuit[4]. The output accuracy and the turning point spur from $V_{\rm SOFT2}$ to $V_{\rm REF}$ induced by the compound structure is an important problem in this method. In the third method[5], the soft-start voltage is added to the input of the pulse width modulator comparator directly while the operation principle is similar to the second method, but it also has the same problems. In addition, the third method has a fatal disadvantage that the loading capability during a long soft-start time is poor. During the start-up process, the duty cycle increases depending on the output of the converter, so if the output cannot start up in time due to the maximum load, this will mislead the loop to operate in a certain load less than the maximum load; the worse case is when the inductor current inversely increases rapidly, as a result, the inductor is saturated and devices are damaged by large current. The proposed soft-start in section 4 aims to give a solution to these problems.

4. Proposed soft-start circuit

In previous works[1–3], extra pin-out and discrete capacitors were needed to reach longer soft-start time. For example, if $V_{\rm REF}$ equals 0.8 V and 1 ms soft-start time is needed with 1 μA charging current, a 1.25 nF capacitor is needed. In other works[4, 5, 9–13], one is the clock-based soft-start circuit which

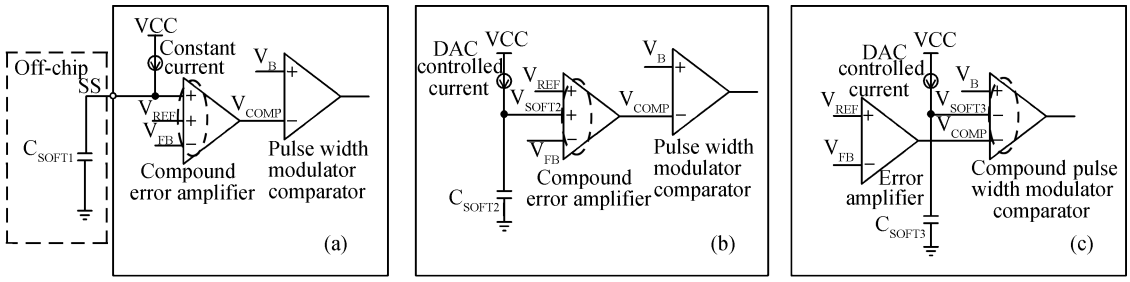


Fig. 2. Traditional soft-start circuit.

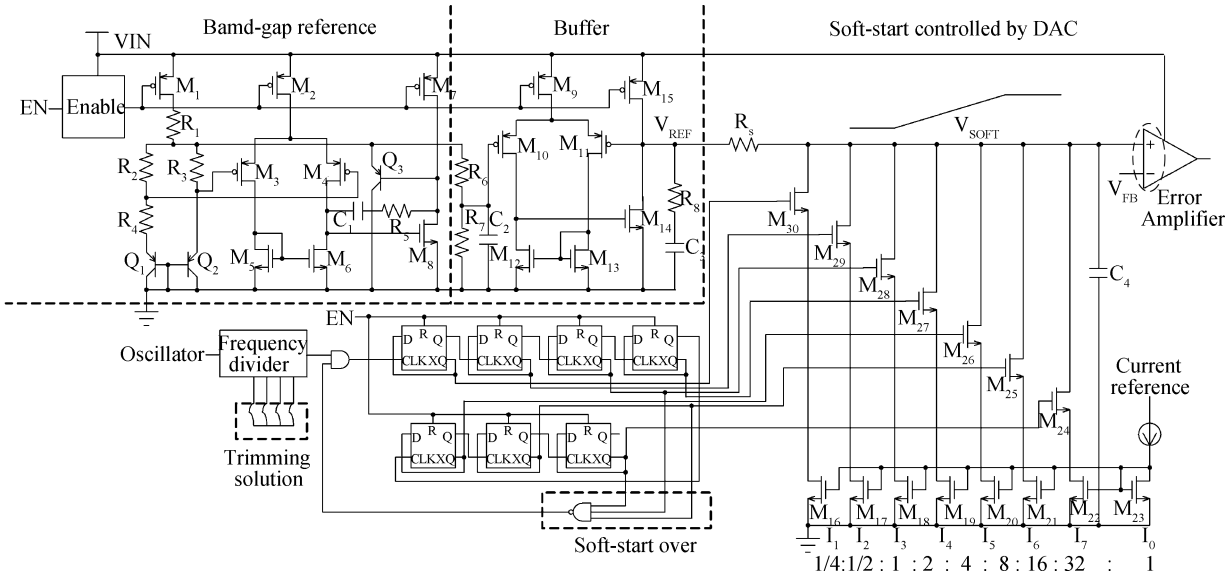


Fig. 3. Schematic of the proposed soft-start circuit.

raises the reference voltage, maximum output current or duty cycle slowly. In this method, the way to achieve the longer soft-start time is to reduce the clock frequency or increase the bit-length of the counter. The latter one fails to reach the goal of raising the switching frequency to minimize the energy storage elements (such as inductors and capacitors), enhance the response speed in switching regulator design, and improve the system accuracy and smooth transition.

As discussed above, for an excellent soft-start, it should have the following features: (1) without the extra pin; (2) without compound structure, such as a compound comparator and amplifier, only with a simple two input-port amplifier and comparator; (3) without the detecting circuit to switch the comparison point; (4) the switching frequency should not be reduced when we reduce the soft-start clock frequency. So, our proposed soft-start circuit with these features is shown in Fig. 3. We will discuss the advantages over other circuits after the description of the principle. First, a 1.2 V band-gap voltage having no relationship with the power supply and temperature is generated by the typical band-gap circuit. The resulting band-gap voltage is:

$$V_{\text{band-gap}} = \frac{R_3 + 2R_1}{R_4} \frac{k \ln\left(S_{Q1}/S_{Q2}\right)}{q} T + V_{\text{beQ2}}, \quad (2)$$

where k and q are constants, and S_{Q1} and S_{Q2} are the emitter areas of transistors Q1 and Q2 respectively.

Second, to widen the range of the output voltage, 0.8 V reference voltage is obtained by the resistor divider R_6 and R_7. A buffer circuit is used to improve the loading capability. Then:

$$V_{\text{REF}} = \frac{R_7}{R_6 + 2R_7} V_{\text{band-gap}}. \quad (3)$$

Third, by using a high precision current sink from the V_{REF} through the resistor R_S cycle by cycle, the soft-start can be simply controlled by DAC with the clock cycle and steps. It is realized by the oscillator control and 7 bits DAC. The soft-start over-circuit is to shut the sinking current when detecting the end of the soft-start, which is effective for low power dissipation and low noise. Otherwise, our detecting circuit is different from the above because this detecting is a certain transition, and it does not need the detecting comparator to switch the comparison point. In this work, 250 μs soft-start time is designed. Because the clock frequency is fixed at 400 kHz, and the clock cycle is 2.5 μs, it is obvious that the steps must be 100. Based on this point, 7 bits DAC is designed for counting from 0000000 to 1100100. To generalize the soft-start process, the soft-start signal V_{SOFT} added to the error amplifier can be calculated by:

$$V_{\text{SOFT}} = V_{\text{REF}} - R_S(b_0 I_0 + b_1 I_1 + b_2 I_2 + b_3 I_3 + b_4 I_4 + b_5 I_5 + \cdots + b_n I_n)$$

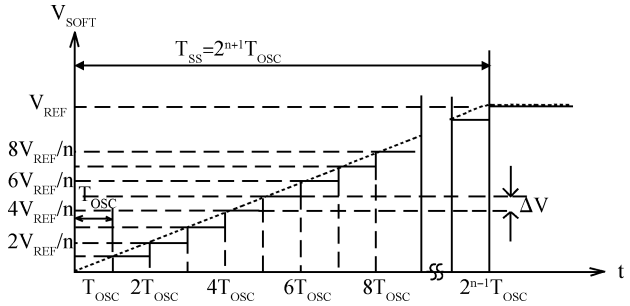


Fig. 4. Curve of the soft-start.

$$= V_{\mathrm{REF}} - R_{\mathrm{S}}(b_0 I_0 + b_1 2I_0 + b_2 4I_0 + b_3 8I_0 + b_4 16I_0 + b_5 32I_0 + \cdots + b_n 2^n I_0)$$

$$= V_{\mathrm{REF}} - R_{\mathrm{S}} I_0 \sum_{i=0}^{n} 2^i b_i, \tag{4}$$

$$V_{\mathrm{SOFT}} = \begin{cases} 0, & \text{Disenable,} \\ V_{\mathrm{REF}} - R_{\mathrm{S}} I_0 \sum\limits_{i=0}^{n} 2^i b_i, & \text{During soft-start,} \\ V_{\mathrm{REF}}, & \text{After soft-start,} \end{cases} \tag{5}$$

where $I_0 = I_{\mathrm{REF}}/4$ in order to reduce the layout area. From Eq. (5), the whole soft-start time can be adjusted from 0 to 2^{n+1} clock cycles by the DAC. The soft-start time can be programmed by the value of R_{S}, I_0 and the clock cycle. So the soft start-up is very smooth and linear due to the accurate control. Also, the soft-start time can be adjusted from microseconds to milliseconds simply by setting R_{S}, I_0 and the clock cycle without the external component. The start-up principle can be illustrated by Fig. 4. If we assume ΔV is the voltage step of the V_{SOFT} during the soft-start, ΔI is the changed value of inductor current induced by ΔV, as shown in Fig. 4, then:

$$\Delta I = \Delta V \times A_{\mathrm{EA}(\omega)} \times \mathrm{GM}_{\mathrm{MOD}(\omega)}, \tag{6}$$

where $A_{\mathrm{EA}(\omega)}$ is the gain of the error amplifier and $\mathrm{GM}_{\mathrm{MOD}(\omega)}$ is the transconductance of the modulator under a certain frequency. The inductor current will become worse if the voltage interval ΔV is too large. A solution is to reduce the clock cycle and voltage steps during the soft-start.

There are several advantages compared to other solutions shown in Fig. 2: (1) The key point, which the maximum soft-start voltage will equal the reference voltage, is obvious, so there is no turning point overshoot when changing the soft-start voltage to the reference voltage, then the soft-start process can be smooth as shown in Fig. 4, which can be understood through the start-up of output in Fig. 6. (2) The soft-start time can be programmed to several milliseconds by the frequency divider with the trimming solution, which can not result in the problem of poor loading capability and the size of the energy storage elements (such as inductors and capacitors). In other words, if a long soft-start time is needed, we can change the frequency divider to get a low frequency before the 7 bits DAC. (3) The output accuracy is improved due to the absence of the compound amplifier and comparator.

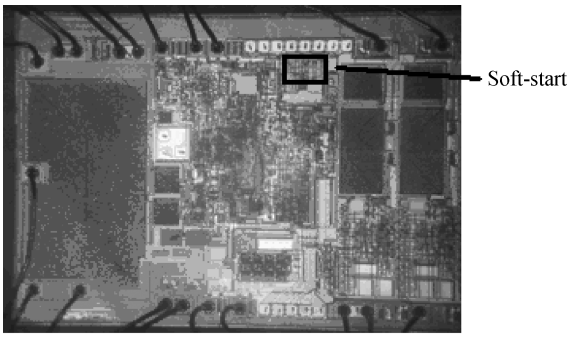
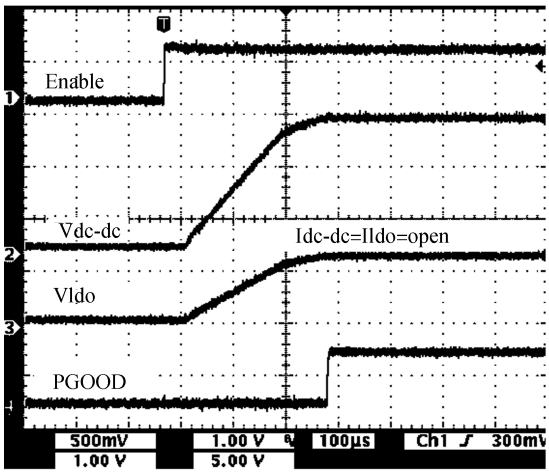
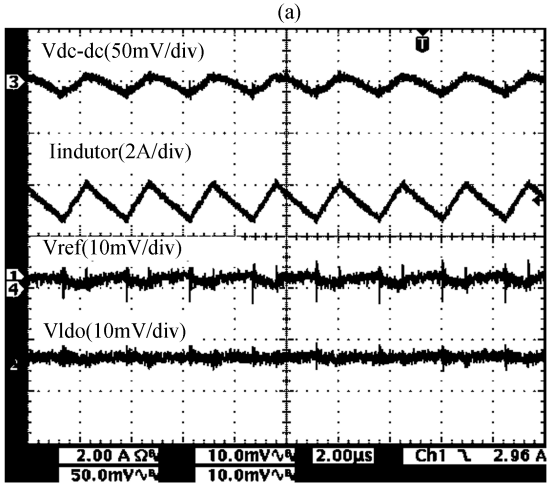


Fig. 5. Micrograph of the proposed power system.



(a)



(b)

Fig. 6. Measurement waveform of (a) soft-start and (b) nominal operation. Conditions: $V_{\mathrm{dc-dc}} = 2.5$ V, $V_{\mathrm{ldo}} = 1.8$ V, $C_{\mathrm{in}} = 10$ μF, $C_{\mathrm{dc-dc}} = 4.7$ μF, $C_{\mathrm{ldo}} = 1$ μF, $L = 1$ μH. The test circuit is shown in Fig. 1, and the off-chip component is outside the dashed frame.

5. Experimental results and discussions

The power supply chip with excellent embedded soft-start was fabricated in a 0.35 μm CMOS process. The total layout area is only 1.05 mm^2. A micrograph is shown in Fig. 5. The operation waveforms of the system are shown in Fig. 6. It can be seen from Fig. 6(a) that the soft-start is smooth and the output voltage has no overshoot. Once the system is enabled, V_{ref}

Table 1. Performance summary and comparison.

Parameter	Ref. [3]	Ref. [4]	Ref. [13]	Ref. [14]	This work
Process	–	0.6 μm BCD	–	0.6 μm CMOS	0.35 μm CMOS
Input voltage (V)	4.75–23	5	2.5–5.5	2.2–6	2.5–5.5
Input capacitor (off-chip) (μF)	10×2	–	10	–	10
Output capacitor (off-chip) (μF)	22×2	300	2200×2	10	$C_{dc-dc} = 4.7$, $C_{ldo} = 1$
Inductor (off-chip) (μH)	10	–	1.5	4.7	1
Supply current (μA)	1300	–	420	48.6 (No switching)	350, 28 (No switching)
Frequency (MHz)	0.34	–	2.25	1.1	0.40
Soft-start time (μs)	15 000 @ $C_{SS} = 0.1$ μF (with an extra pin and a compound amplifier)	1200 (with a reference switch circuit)	950 (with a compound amplifier)	> 1500 (with imprecise soft-start)	250 (without an extra pin, compound amplifier or comparator)
Maximum output current (A)	3	6.5	0.8	1	4
Output voltage accuracy (%)	–	–	± 2	–	± 1.3

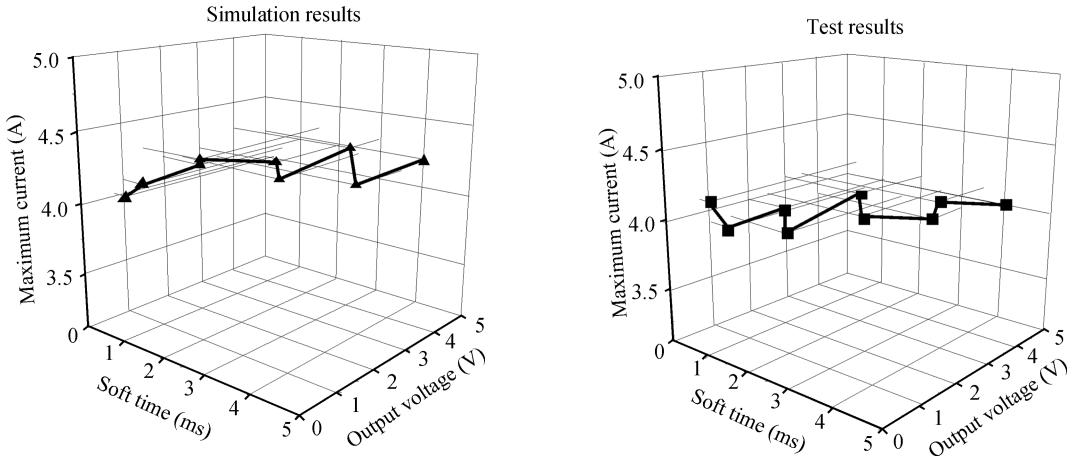


Fig. 7. Comparison of simulation and test maximum load current during the soft-start with different output voltages (conditions is similar to Fig.6).

starts up linearly, and the output of the converter V_{dc-dc} and V_{ldo} begins to start up simultaneously. A PGOOD pin is used for showing the nominal state when the output of the DC–DC and LDO achieves 80% of the target value. Figure 6(b) shows the nominal operation. Since we choose the common filter capacitor, the equivalent series resistor is relatively large, so the output ripple is about 15 mV, which is suitable for conventional applications. But if a small ripple is needed, it can be simply realized by a low equivalent series resistor. Also, Figure 7 shows the maximum load current versus the soft-start time and the output of the DC–DC converter. We can see the maximum load current, which has no relationship with soft-start time. From 100 μs to 4 ms soft-start time, the maximum load current always stays in 4 A. With different output voltages and soft-start time, the fact that the maximum current shows a slight difference is normal because of the shift of some characteristics, such as power transistors, parasitical capacitors and resistors, and practical noise, but the average value is a constant. Finally, we give a performance and comparison summary in Table 1. It can be seen that Reference [3] adopts the most common and simplest soft-start circuit, and realizes 15 ms soft, but needs an extra pin C_{SS}. Reference [4] uses the detecting circuit to switch the comparison point from the soft voltage to the reference voltage, and realizes 1.2 ms soft, but there exists a complicated compensation circuit to cancel out the turning point spur. In particular, once the switch comparator switching the comparison point has a little offset, the inrush inductor current must be induced, rather than the offset of the switch comparator being changed with the corner of the supply voltage, the temperature, and so on. Reference [5] uses a compound pulse width modulation comparator and adds two comparators, which will reduce the output accuracy and increase the layout area. Reference [13] uses a similar technique to Ref. [4]. In addition, it also has a compound error amplifier. Reference [14] uses a smaller charging current (1 nA) to the on-chip capacitor, but the soft-start accuracy is reduced. In our work, we avoid the above problems and adopt a simple amplifier, without an extra pin and switch comparator, to realize 250 μs soft independent of load current. Furthermore, the conditions of soft-start in the converter and some results from soft-start are given in the table.

6. Conclusion

A novel embedded soft-start circuit for a power supply for

SOC is presented in this paper. The operation principle has been introduced, and the proposed circuit has been applied to a power supply with a current mode buck converter and low dropout regulator. Excellent performance is shown and verified by simulation and experimental results. The whole chip has been fabricated in a 0.35 μm CMOS process. The measurement results show that the chip starts up successfully with 250 μs soft-start time in 400 kHz switching frequency, 2.5 V DC–DC output, 1.8 V LDO output conditions. Stable operation after soft-start is also shown. A performance and comparison summary is given in Table 1. So, the proposed circuit can be applied to SOC applications that require good performance characteristics: power sequencing, output accuracy, silicon area, response time, and off-chip component.

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