A 6–9 GHz 5-band CMOS synthesizer for MB-OFDM UWB*

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Abstract: An ultra-wideband frequency synthesizer is designed to generate carrier frequencies for 5 bands distributed from 6 to 9 GHz with less than 3 ns switching time. It incorporates two phase-locked loops and one single-sideband (SSB) mixer. A 2-to-1 multiplexer with high linearity is proposed. A modified wideband SSB mixer, quadrature VCO, and layout techniques are also employed. The synthesizer is fabricated in a 0.18 μm CMOS process and operates at 1.5–1.8 V while consuming 40 mA current. The measured phase noise is −128 dBc/Hz at 10 MHz offset, and the sideband rejection is −22 dBc at 7.656 GHz.

Key words: 6–9-GHz; frequency synthesizer; PLL; MB-OFDM; UWB; CMOS
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1. Introduction

Ultra-wideband (UWB) technologies are mainly used to achieve short-range, high-data-rate wireless communications with less than 10 meters of transmission distance and higher than 480 Mb/s of transmission rate for wireless personal area networks (WPANs).

Since 2002, the American Federal Communications Commission (FCC) approved the use of a 7.5 GHz band spectrum (3.1–10.6 GHz) with the power spectral density of up to −41.3 dBm/MHz, the worldwide major countries have announced their own ultra-wideband frequency regulatory[1].

Multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB standard proposed by WiMedia Alliance partitions the 3.1−10.6 GHz band into 14 sub-bands of 528 MHz width and adopts frequency hopping methods for signal transmission. These frequencies are further grouped into 6 groups, each with two or three adjacent frequency bands[2].

From the comparison of the worldwide UWB frequency regulatory, and combining with the characteristics of China's own spectrum plan, we found that to choose the 6−9 GHz UWB frequency band, covering the MB-OFDM UWB band group (BG) 3 and BG6, will be a better compromise between versatility and cost.

To meet the stringent frequency hopping time requirements (< 9.47 ns), several frequency synthesizers based on SSB frequency mixing were proposed recently[3−9]. Nevertheless, these architectures achieve either 14 frequencies for full-band 3.1−10.6 GHz[3, 9], or three frequencies for 3.1–4.5 GHz BG1[4] and nine frequencies for 3.1–8.5 GHz BG1/2/3[5, 6, 8]. In the 6−9 GHz frequency band, the above mentioned frequency synthesizers have the shortcomings of insufficient specificity, or excessive coverage of frequency band leading to waste area and power, or low coverage of frequency band leading to be unable to take full advantage of 6–9 GHz five frequencies thus affecting the channel capacity.

To resolve the above difficulties, this paper proposes a 5-band CMOS I/Q frequency synthesizer based on a single SSB mixer architecture, which has the highest versatility and spectral purity with the realization of low complexity, low cost and low power consumption. The synthesizer uses two PLLs and generates 6600 MHz, 7128 MHz, 7656 MHz, 8184 MHz, 8712 MHz carriers with sufficient sideband rejection, and its switching time is less than 3 ns. With proper frequency planning, only divide-by-2 dividers are needed in the feedback path of the PLL. Thus, more precise in-phase and quadrature phase sub-harmonics can be derived from the divider chain for SSB frequency mixing.

2. Architecture

A band-switching time of synthesizers for MB-OFDM UWB transceivers is required on the order of nanoseconds, which poses difficult challenges with respect to noise, sidebands, and power consumption. Due to their long settling time, conventional PLL-based synthesizers fail to provide such a fast hopping. The fast hopping characteristic can be achieved using dual-loop architecture with SSB mixing in this paper.

The proposed synthesizer architecture is illustrated in Fig. 1. This synthesizer can generate five bands of BG3 and BG6 distributed from 6 to 9 GHz with only one SSB mixer, one MUX and two PLLs with less than 3 ns switching time. The principle of operation is as follows: PLL_1 generates the fixed I/Q frequency of 7656 MHz, whereas PLL_2 produces the fixed frequency of 4224 MHz. A frequency selection switch (that is MUX) in front of the tri-mode divider[6] selects the 2112 MHz and 1056 MHz signals for frequency additions and subtractions, which are produced by two stages of static divide-by-2 frequency divider in the feedback path of 4224 MHz PLL. The subsequent programmable tri-mode divider, placed in front of one of the inputs of the SSB mixer, provides DC or quadrature signals with different I/Q phase sequences of 528 MHz and 1056 MHz, allowing the SSB mixer to create up five synthesized frequencies. By quadrature mixing the 7656 MHz signal

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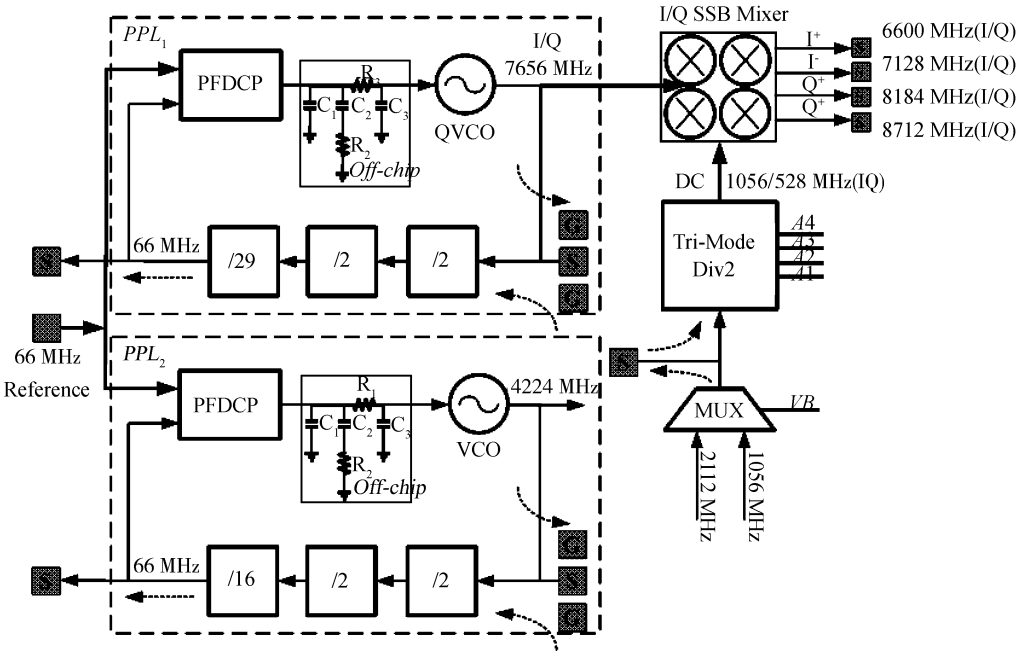

Fig. 1. Block diagram of our proposed frequency synthesizer.

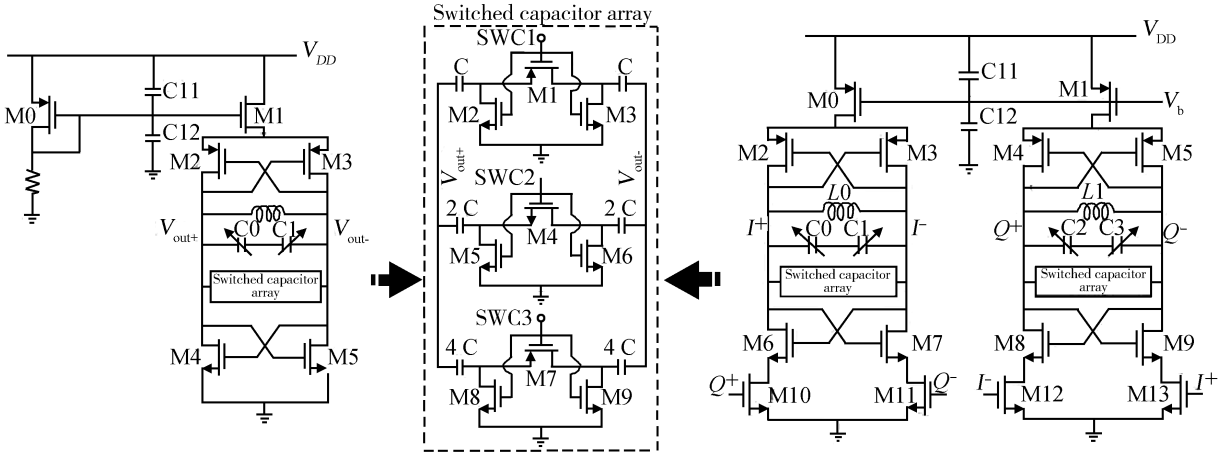

Fig. 2. Schematic of 4 GHz VCO (left) and 7 GHz QVCO (right).

with either ±1056 MHz or ±528 MHz or DC using a quadrature SSB mixer, the I/Q frequencies of Bands 7 to 11 are generated respectively.

The carrier generation can be simply formulated as follows:

$$f = 7656\,\text{MHz} \pm (0, 528\,\text{MHz}, 1056\,\text{MHz}). \quad (1)$$

The PLL_1 is operating at 7656 MHz, providing I/Q phases from an LC-QVCO. The PPL_2 has an oscillator at 4224 MHz, whose output signal is fed to two stages of static divide-by-2 frequency divider, generating the 2112 MHz and 1056 MHz I and Q signals. Both PLLs use a common 66 MHz external reference signal.

In order to achieve broadband operations while relaxing the complexity of signal routings, the five bands are directly produced from the quadrature SSB mixer with the input of 7656 MHz I/Q carrier and DC/528 MHz/1056 MHz I/Q carrier.

One major technical issue in this architecture is unwanted spur tones generated by non-linear components, such as dividers and SSB mixers. The sideband suppression requirement is very strict due to its wideband characteristics. Since only one SSB mixer is utilized, the effect of nonidealities due to mismatches in the signal path and the mixer itself can be considerably reduced. In addition, this scheme can achieve good in-band spur suppression with lower DC power consumption than other previous works because it adopts fewer nonlinear components, such as dividers and mixers in accordance with the proposed frequency plan.

3. Circuit implementation

3.1. VCO and QVCO

The synthesizer includes two oscillators utilized for two PLLs respectively. As shown in Fig. 2, the 4 GHz VCO employs a popular topology of a LC-type oscillator, while

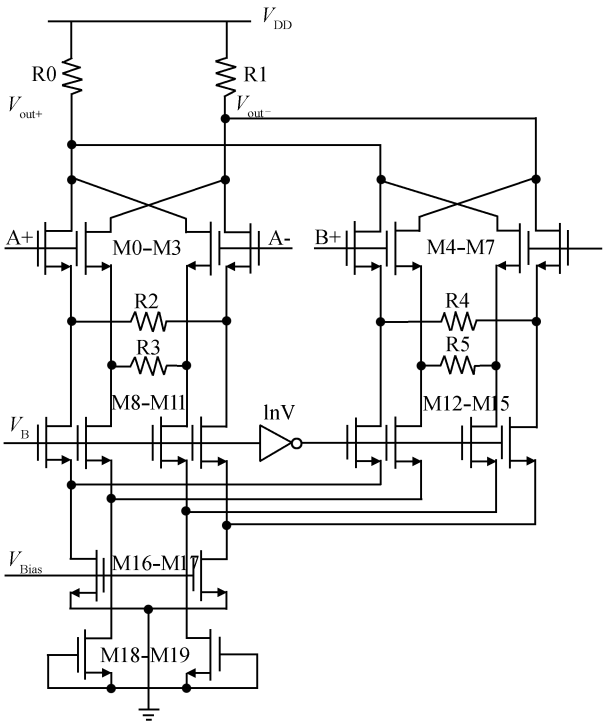

Fig. 3. Schematic of the proposed MUX.

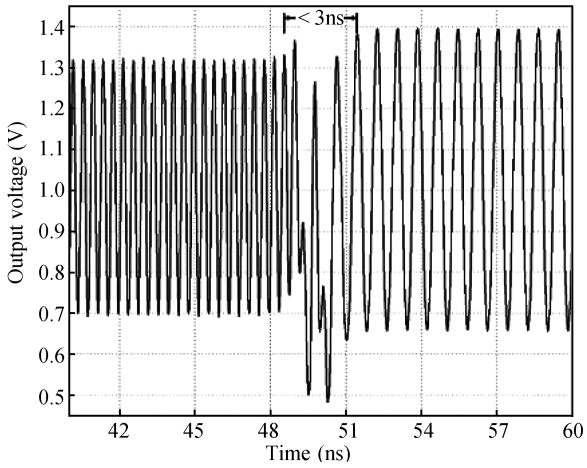

Fig. 4. Switching time of the proposed MUX.

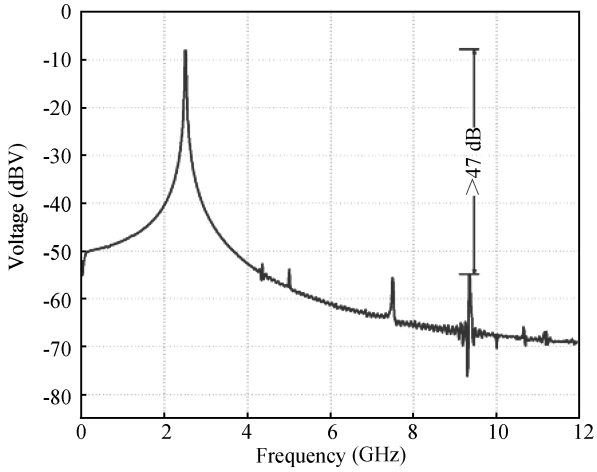

Fig. 5. Simulated spectrum of the proposed MUX.

the 7 GHz quadrature VCO employs modified bottom-series structure with two symmetric coupled LC oscillators[10, 11]. The LC-type VCOs include a complemented cross-coupled NMOS/PMOS pair for the generation of negative conductance and LC resonators consisting of a differential coil, accumulation-mode nMOS varactors and coarse tuning capacitor array. To cover the VCO tuning, conventional coarse tuning capacitances composed of MIM capacitors and switches are used in the switched capacitor array based on binary-weighted architecture. Through switches, the binary-weighted capacitors can be switched in and out of the LC tank[12, 13].

Device sizes are optimized for best performance such as phase noise, phase accuracy and amplitude imbalance, especially the switching pairs in serried with the coupling transistors used in the QVCO. Both oscillators use inductors to improve phase noise performance and reduce power dissipation.

As a result, the first VCO tunes in 3.7–4.9 GHz within a tuning voltage range of 0.2–1.6 V, draws 7 mA (including buffers) from a 1.8 V supply, and simulates the phase noise of –118 dBc/Hz at a 1 MHz offset. Correspondingly, the second QVCO covers 6.75–8.67 GHz and draws 20 mA (including buffers), and the phase noise level is −114 dBc/Hz at 1 MHz offset. A more than 25% tuning range is achieved mainly by digitally controlled MOS capacitors for both VCOs to compensate temperature and process variations.

3.2. Multiplexers

The proposed circuit schematic of the multiplexer (MUX) is shown in Fig. 3. The role of this MUX is to select one out of the two frequencies at one time and feed it to the subsequent tri-mode-divider. The MUX is based on two differential pairs sharing a common resistive load. Their activations and deactivations are through a clock signal to enable or disable the tail current. When the wanted band is selected, the corresponding current source is turned on and the frequency deviation signals are delivered from the PLL towards the pair of switching quads. The reverse isolation from the switching signals to the MUX will be enhanced. When another band is chosen, the corresponding current source is activated and only the DC bias currents will be passed to the switching quads.

It must provide fast switching action and good isolation. Since strong signals continuously exist in both inputs, the isolation is very necessary for avoiding the mixing of the two signals in the subsequent blocks. The use of input dummy differential pairs improves the isolation between the two stages and enhances the circuit linearity, while consuming no extra power. Apart from providing frequency selection, these stages also reinforce the signal strength. The two current sources must be well matched. There is no DC voltage drop required for the resistors (R2–R5) because no currents flow through them.

The simulated switching time of this MUX was less than 3 ns as shown in Fig. 4, which was much less than the required 9.47 ns.

The proposed MUX with coupling cancellation technique provides up to −47 dBc of sideband rejection as the simulation result showed in Fig. 5.

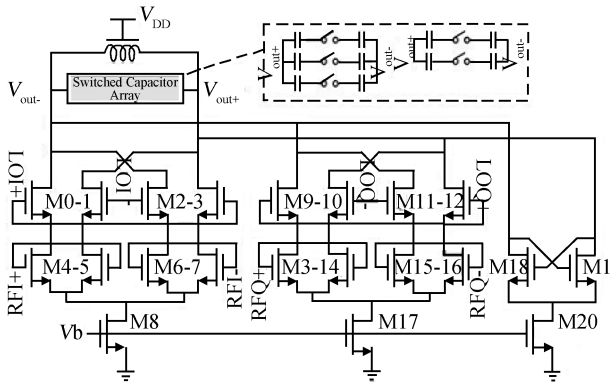

Fig. 6. Schematic of the proposed SSB mixer cell.

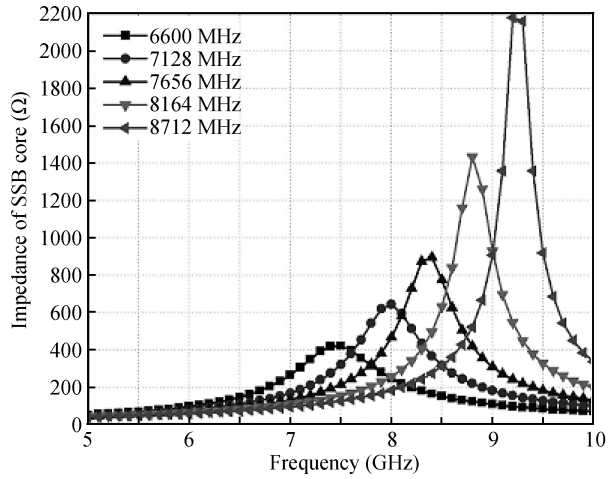

Fig. 7. Simulated single-port output impedance of the SSB mixer.

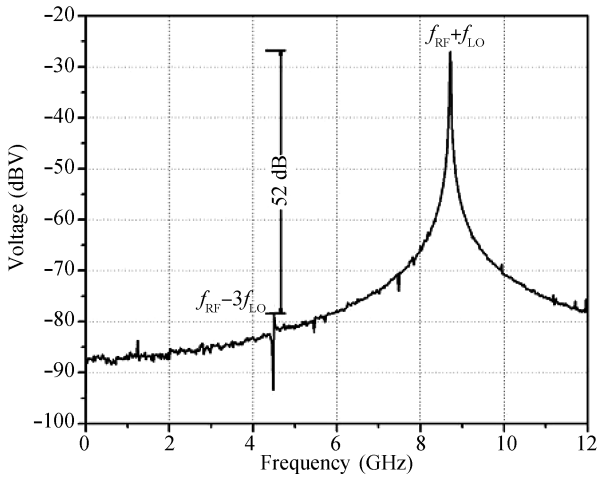

Fig. 8. Simulated spectrum of the proposed SSB mixer.

3.3. SSB mixer

Figure 6 illustrates the core of the SSB mixer implementation, which incorporates band-pass LC-type loads and source degeneration techniques to suppress sidebands. The nonlinearities of the mixers generate harmonics that may propagate throughout the system, getting mixed with other tones and creating undesired frequencies. To provide further attenuation to the unwanted sidebands and spurs, filtering in the form of LC tunable resonators as loads was used in the SSB mixers. With switched-capacitor LC tanks, a wide bandwidth of 3 GHz is needed and it should provide sufficient selectivity to lower the sideband level. Traditional shunt- and series-peaking techniques provide a wide and flat response, but lack enough voltage gain and selectivity. Single switched-capacitor LC tank mixers suffer from gain and selectivity degradations due to the decreased quality factor at lower frequencies. To alleviate this problem, five switched-capacitor LC tanks, which can be programmed to the desired group with flat enough voltage gain, are incorporated. The center frequency of the resonator is adjusted by tuning a capacitor bank along with the band switching of the frequency synthesizer. Band selection is accomplished by adding capacitor arrays to change the tank resonance frequency. By turning the switches on or off, five bands distributed from 7.4–9.2 GHz with more than 500 MHz margin for pre-simulation can be achieved as shown in Fig. 7.

To improve linearity, the mixers employ source degeneration techniques in LO ports. Also the quality factor of the resonator is enhanced by parallelly connecting a negative-g_m cross-coupled pair (M18 and M19) to the mixer differential loads to improve the output signal purity[9]. Cross coupling creates a positive feedback amplifier with two stages. As a result, the differential resistance becomes negative. This negative resistance is easily controlled through the current. Making all devices the same cancels the AC current in this circuit, causing the differential impedance to be very high (infinity if matching is perfect). The transconductance of the negative-g_m cross-coupled pair is appropriately chosen to keep the Q enhance circuit from oscillating, and furthermore to optimize the trade-off between the enhancement of the output signal purity and the degradation of the acceptable switching time due to the high quality factor.

The simulation results in Fig. 8 show that the structure of the circuit has a good spur suppression capability, over 52 dB. The highest spurs actually occurs at $f_{RF}-3f_{LO}$, resulting from the mixing of the RF signal and the third-order harmonic of the LO signal.

The quadrature SSB mixer operates quadrature inputs so as to perform frequency additions and subtractions without generating mirror signals. In contrast to a phase shifter that operates only narrow bands, a static frequency divider manifests itself in providing quadrature outputs across a wide frequency range. The divider is modified by combining two opposite routing configurations. Furthermore, the generation of DC signals can also be merged into the divider, which results in the tri-mode divider depicted in Ref. [6]. Inverting the sign of the 528 MHz and 1056 MHz frequencies is achieved by inverting one of the I and Q signals through tri-mode divider.

3.4. Layout consideration

A lot of special considerations were paid to the chip layout. Lager-signal blocks, weak-signal blocks, and the digital-signal blocks were carefully distributed. The two VCOs were placed far away from each other as much as possible to avoid harmonic pulling. Double guard rings were used to minimize the noise coupling between and around each building block, especially digital and analog/RF parts. The control lines between

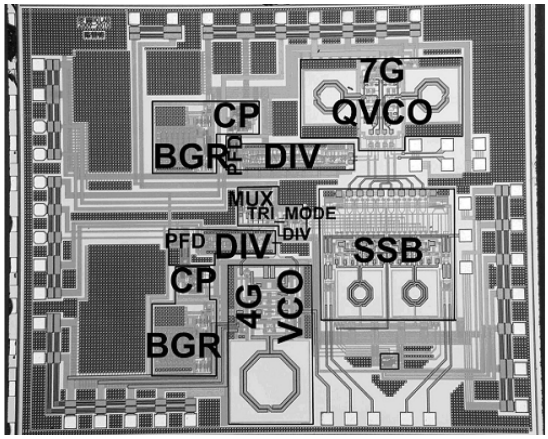

Fig. 9. Chip photograph of the synthesizer.

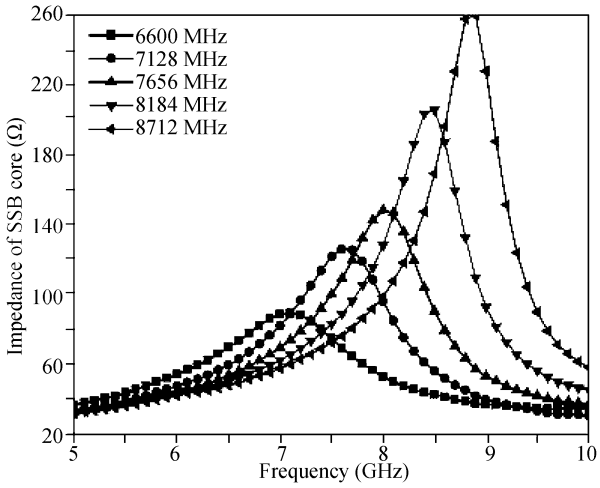

Fig. 10. Measured single-port output impedance of the SSB mixer.

VCO (QVCO) and LPF were protected by grounded metals. Symmetric inductors were utilized to minimize die area. Phase and gain mismatches between internal signals were minimized by symmetric layouts. All power supplies were on-chip decoupling, and the simulation results showed more than 50 dB reduction of noise from the chip power supply.

4. Experimental results

The experimental prototype of the proposed UWB frequency synthesizer is implemented in a 0.18 μm CMOS technology. It provides I/Q signals for the 5-band carriers of 6600 MHz, 7128 MHz, 7656 MHz, 8184 MHz, and 8712 MHz. Its chip micrographic image is shown in Fig. 9. The chip consumes 40 mA from a single 1.5–1.8 V supply voltage. This chip was mounted on FR4 PCB, and an Agilent N9020A MXA analyzer and an Agilent DSA9134A digital signal analyzer were used to measure the chip parameters.

The single-port output impedance of the proposed SSB mixer is measured. As shown in Fig. 10, the measured center frequencies are shifted higher than expected from 7.0 to 9.0 GHz with relative close impedance because of process variation.

Figure 11 shows the measured tuning curves of the proposed 7 GHz QVCO, which achieves a tuning range of 22.7%, from 6.95 to 8.73 GHz. Also, the measured 4 GHz VCO frequency tuning range from 3.75 to 4.95 GHz (27.6%) is achieved with the tuning voltage from 0 to 1.8 V.

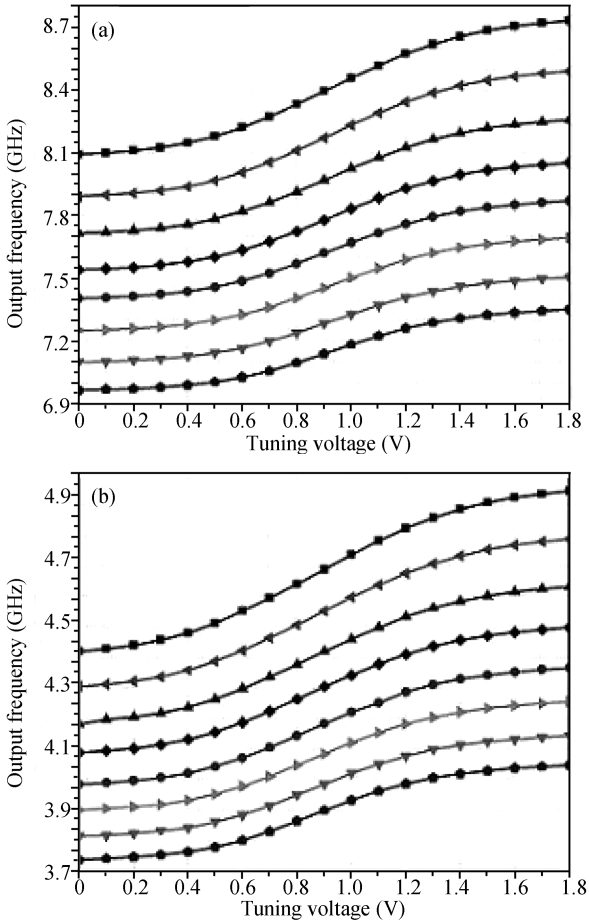

Fig. 11. Measured tuning characteristics of (a) 7 GHz QVCO and (b) 4 GHz VCO.

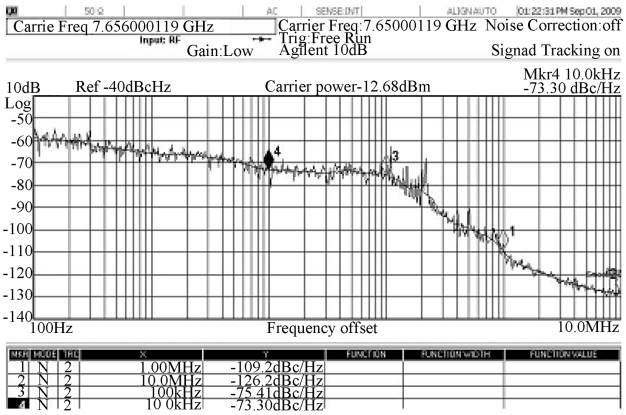

Fig. 12. Measured phase noise at 7656 MHz.

As shown in Fig. 12, the measured phase noise from the 7656 MHz carrier is about –109.6 dBc/Hz at 1 MHz offset, and is suppressed to below –128 dBc/Hz at 10 MHz offset. Since the best in-band phase noise for the external reference of 66 MHz generated from our Agilent N5182A MXG vector signal generator is limited to around –110 dBc/Hz, a good phase noise

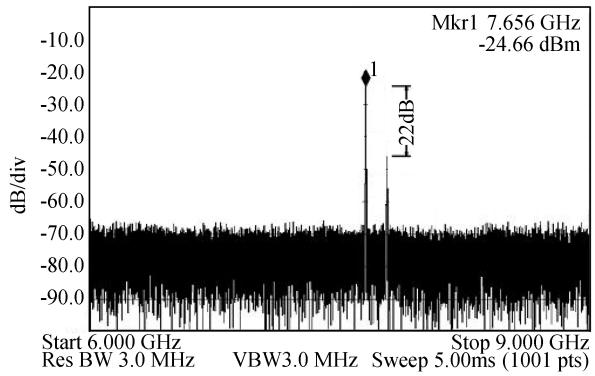

Fig. 13. Measured output spectrum at 7.656 GHz.

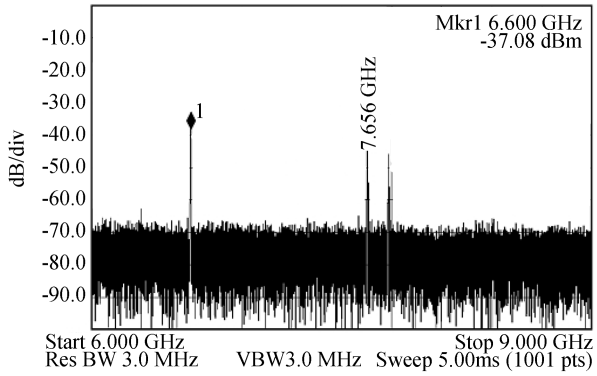

Fig. 14. Measured output spectrum at 6.6 GHz.

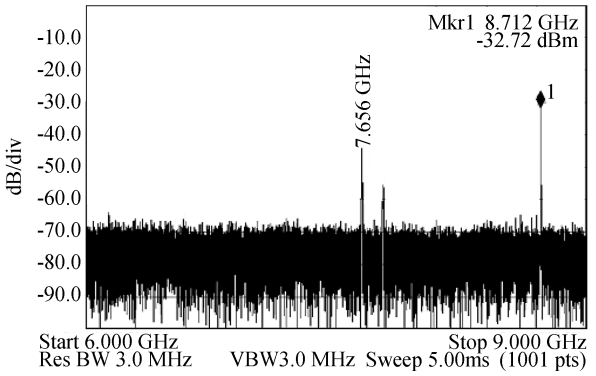

Fig. 15. Measured output spectrum at 8.712 GHz.

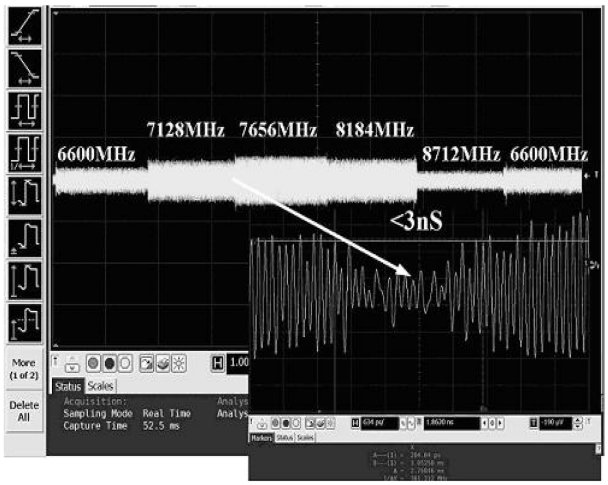

Fig. 16. Measured switching time from 7128 to 7656 MHz band.

can be easily achieved with a better reference from either a good crystal oscillator or a better signal generator.

Some imperfections exist in the experimental results. The first is the high shift of the LC resonant frequency, which resulted in the attenuation of wanted signals and decreased the rejection of unwanted signals. Another is the gain drop of the buffers used in the SSB mixer, which resulted from the negative gain of the source follower structure and the validity of the inductor in external Bias-Tee as a source-side load when testing. Additionally, due to the leakage of PLL signals into the SSB mixer, the spectral purity is not as good as we were targeting. PCB crosstalk can also affect the performance of frequency synthesizer among board-level test. This issue must be emphasized in future research by detailed layout designing and coupling modeling.

Because of the above shortcomings, the harmonic sidebands are somewhat lower than expected, and one measurement result depicted in Fig.13 shows approximately –22 dBc of the image spur occurring for band-7 frequency synthesis (7.656 GHz). Another two measurements were not as good as expected as shown in Figs. 14 and 15.

The fast switching property of the carrier frequency generator was measured with a 40-Gsa/s digitizing oscilloscope (DSA9134A) and the result is shown in Fig. 16. From Fig. 16, it is seen that the signal hopping from band 8 to band 9 recovers within 3 ns. Transitions between other bands are very similar. However, due to the above mentioned reasons about poor sideband rejection, transitions are not as clear as the simulated result depicted in Fig. 4. If delay due to various parasitic effects such as PCB traces and bondwires is ignored, the actual internal switching time would be smaller.

The performance of the proposed local signal generator is summarized in Table 1 along with that of the other reported configurations. Table 1 shows that the proposed synthesizer can provide 5 I/Q bands from 6 to 9 GHz while incorporating the least inductors, which means the core area of the circuit is the smallest.

5. Conclusion

A fast-hopping synthesizer designed for WiMedia UWB applications has been presented in this paper. This synthesizer is fabricated in 0.18 μm CMOS technology. It is composed of two PLLs and one MUX, which shows good potential for UWB radio operating in 6–9 GHz with fast switching and good spectral purity. The implemented chip is able to provide I/Q signals of 6600 MHz, 7128 MHz, 7656 MHz, 8184 MHz, and 8712 MHz with 3 ns switching time. It consumes less than 40 mA current at 1.5–1.8 V supply voltage. The measured sideband rejection is about –22 dBc and the phase noise is –128 dBc/Hz at 10 MHz offset at 7.656 GHz.

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Table 1. Performance summary and comparison.

Parameter	This work	Zheng[5]	Lee[6]
Frequency scheme	Direct conversion	Dual conversion	Direct conversion
Number of bands	5	9	7
Number of inductors	5	11	12
LO frequency (GHz)	6.6−8.712 (IQ)	6.336−10.56 2.904 (IQ)	3.432−7.92
Switching time (ns)	3	1	1
Sideband suppression (dBc)	−22 @ 7.656 GHz	−38.6 @ 6.336 GHz	−37
Phase noise (dBc/Hz)	< -128 @ 10 MHz	< -124 @ 10 MHz	−110 @ 1 MHz (VCO)
Supply voltage (V)	1.5–1.8	1.5	2.2
Power consumption	40 mA	59 mA	48 mW
Technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS

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