A low power 8-bit successive approximation register A/D for a wireless body sensor node*

Liu Liyuan(刘力源)[1], Li Dongmei(李冬梅)[2,†], Chen Liangdong(陈良栋)[2], Zhang Chun(张春)[1], Wei Shaojun(魏少军)[1], and Wang Zhihua(王志华)[1]

(1 Institute of Microelectronics, Tsinghua University, Beijing 100084, China)
(2 Department of Electronic Engineering, Tsinghua University, Beijing 100084, China)

Abstract: A power efficient 8-bit successive approximation register (SAR) A/D for the vital sign monitoring of a wireless body sensor network (WBSN) is presented. A charge redistribution architecture is employed. The prototype A/D is fabricated in 0.18 μm CMOS. The A/D achieves 7.5ENOB with sampling rate varying from 64 kHz to 1.5 MHz. The power consumption varies from 10.8 to 225.7 μW.

Key words: successive approximation register; A/D; low power; wireless body sensor node
DOI: 10.1088/1674-4926/31/6/065004 **EEACC:** 1265H

1. Introduction

Recently, medical healthcare SoC systems have become a new research hot topic. The wireless body sensor network composited of many wireless body sensor nodes (WBSN) is a typical application. Every WBSN is able to capture signals by its integrated sensors and make an analysis. Different WBSNs are capable of self-organization into a collaborative network. Nowadays, WBSN is widely used in sign monitoring, diagnosis assistance and drug delivery and brings great convenience to people's lives.

The WBSN hardware design faces some constraints. Firstly, WBSN is usually a portable device and is powered by a small battery with a limited amount of energy. Some intelligent WBSNs even harvest energy by themselves. So the design of the circuits must adopt low-power strategies. Secondly, the wide application range calls for highly adaptive system architecture. Fundamentally, the architecture of any WBSN consists of an analog-to-digital converter for digitizing the signal from the sensors, a digital signal processor for post signal processing and an RF block for communications[1].

This work describes the design of an A/D for a WBSN SoC. The A/D has a resolution of 8-bit. This is enough for applications such as temperature, heart rate and blood-pressure monitoring. The charge redistribution successive approximation register A/D is employed. This architecture has no static current, and the power dissipation is proportional to the sampling rate. The prototype A/D is fabricated in 0.18 μm CMOS, and the power consumption varies from 10.8 to 225.7 μW when the sampling rate varies from 64 kHz to 1.5 MHz with 1.8 V power supply.

2. Architecture and operations

The architecture of the SAR A/D is shown in Fig. 1. The A/D comprises one charge redistribution DAC, one comparator and one control block. The sampling switches are firstly closed and the top plates of the capacitors track the input signal while the bottom plates of the capacitors are connected to the common mode voltage. When the sampling switches are opened an amount of charge proportional to the input signal is stored. The comparator is reset in the meantime. After that the comparator starts to operate and determines the output code bit-by-bit. According to each generated bit, the switches connected to the bottom plates of the DAC are turned to the positive reference (VRP) or the negative reference (VRN). The voltages at the top plates of the capacitor will approach zero in a successive approximation manner.

The control timing of the successive-approximation register A/D is shown in Fig. 2. The sampling clock is generated by dividing the input by a factor of 16, denoted as CLK_DIV16 in the figure. During the high voltage level the sampling switches are closed and the top plates of the capacitors track the input signal. During the low voltage level the sampling switches are opened and the comparator generates every bit of the output code.

The detailed operation is described with the help of the diagram in Fig. 2. When CLK_DIV16 is high and its complementary signal is low, all the flip-flops are reset, the SWP signal is '1' and the SWN signal for each stage is '0'. The bottom plates of the capacitors are connected to the common mode voltage. Immediately after CLK_DIV16 goes low and the complementary signal goes high, the flip-flops are free from the reset state. The bit-cycling is triggered by the falling edge of CLK_DIV16. There are eight pulses during the bit-cycling period corresponding to 8 comparisons. The comparator is aware of the rising edge of the pulse and makes a decision during the high level of the pulse. The decision result is latched when the pulse goes low. If the result is '0' the control signal will make the bottom plates of the capacitor on the top half of the figure connect to V_{RP} and the bottom plates of the capacitor on the bottom half of the figure connect to V_{RN}. The reverse will take place if the decision result is '1'.

* Project supported by National High Technology Research and Development Program of China (No. 2008AA010700).
† Corresponding author. Email: lidmei@tsinghua.edu.cn
Received 12 November 2009, revised manuscript received 6 December 2009

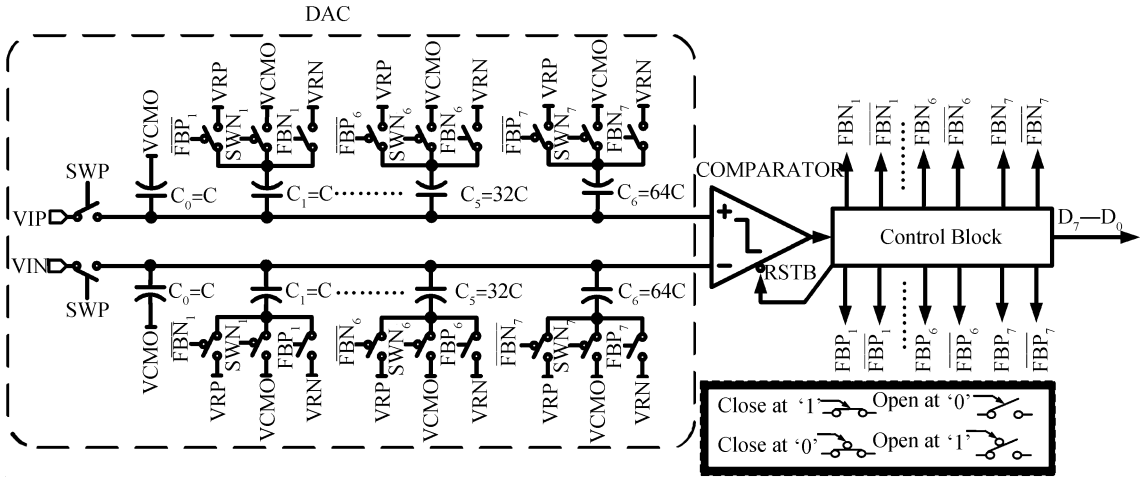

Fig. 1. The system architecture.

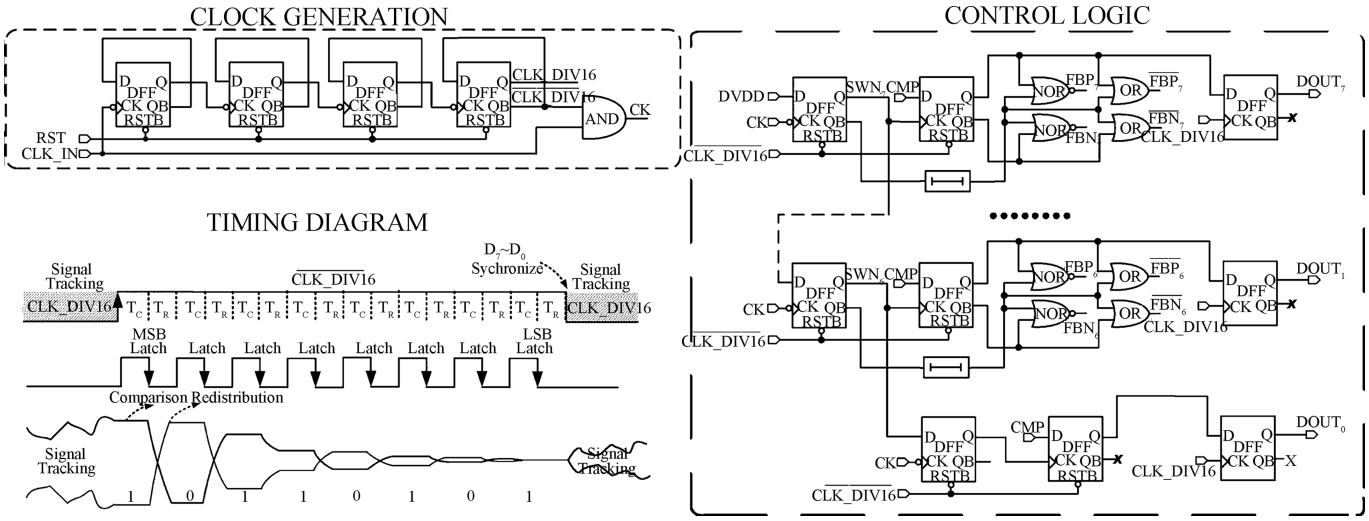

Fig. 2. The control logic and timing diagram.

The charge redistribution is performed during the low level between the pulses. The top plates of the capacitors on the top half of the figure will rise by $1/4V_i D_3$ ($V_{RP}-V_{RN}$) and the top plates of the capacitors on the bottom half will fall by $1/4V_i D_3 \times (V_{RP}-V_{RN})$, after the first charge redistribution of the voltage of the top plates with a decision result of '0'. If the comparison result is '1', the top plates of the capacitors on the top half will fall and the top plates of the capacitors on the bottom half will fall.

It is noted that the bottom plate of the capacitor should be kept connected to the common mode voltage when the preceding charge redistribution is ongoing. Signals SWN_j ((j = 7, 6, …, 1) are for this purpose. Suppose the differential voltage stored on the top plates is V_x and after all the comparisons the final voltage will be $V_x - 1/256\,[\sum 2^j \times D_j] \times (V_{RP}-V_{RN})$ ($D_j = -1, 1, j = 7, 6, \ldots, 1, 0$). This voltage will approach zero after 8 successive approximation charge redistribution processes.

3. Circuit design

The comparator should have no DC quiescent current to reduce the power consumption. Figure 3 shows the comparator employed in this work proposed in Ref. [2]. During the reset phase, nodes N and P are forced "high" and Q and QB are forced "low". During the comparison phase the initial voltage at V_{IP} and V_{IN} will establish a voltage difference at P and N, since the initial common mode voltage of P and N is as high as V_{DD} and so the voltage difference is not large enough to change the state of the latch. The transistor Mt which is turned on dur-

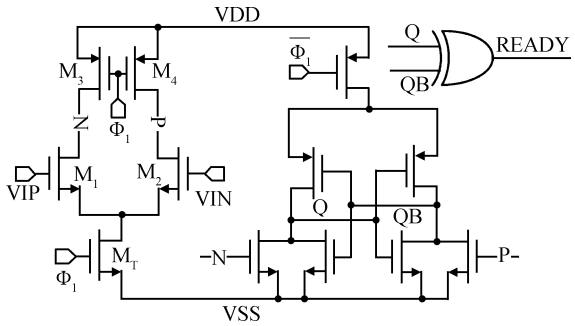

Fig. 3. Comparator.

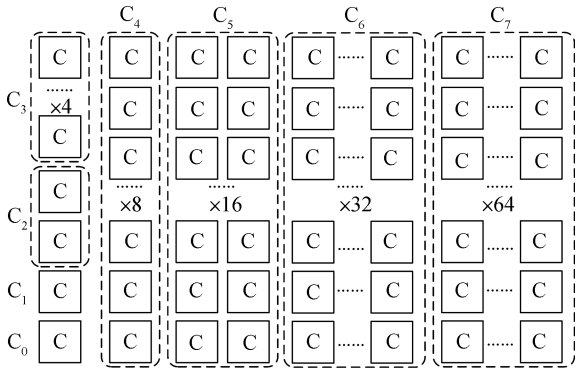

Fig. 4. Layout of the capacitor array.

ing the comparison phase will provide a current and discharge the common mode level at N and P. When the common mode voltage decreases to some extent, the voltage difference will be amplified by the gain stage provided by M1–M4 and this voltage difference will eventually change the state of the latch. The offset of the latch will be suppressed by this gain stage. The matching of the capacitor in the DAC also has a significant impact on the overall performance.

The layout of the DAC array (single-ended) is shown in Fig. 4. The unit capacitance is chosen as $10 \times 10\ \mu\text{m}^2$ ($\sim$100 fF), which is enough for 0.1% matching according to the report provided by the foundry. The layout style makes the parasitic capacitance between the top plate and the bottom plate of the unit capacitor equal to each other. This will maintain the binary weight property of C_7–C_0.

4. Power consumption

The power consumption of the successive approximation A/D is composed of three parts: the power consumption of the DAC, the power consumption of the control logic and the power consumption of the output buffer. The total power consumption can be expressed as:

$$P = P_{\text{DAC}} + P_{\text{Logic}} + P_{\text{Buffer}}, \tag{1}$$

where P_{Logic}, P_{Buffer} are power consumption caused by digital circuits which can be expressed as:

$$P_{\text{Logic}} = \alpha_{\text{Logic}} C_{\text{EFF, logic}} V_{\text{DD}}^2 f_{\text{S}}, \tag{2}$$

$$P_{\text{Buffer}} = \alpha_{\text{Buffer}} C_{\text{EFF, Buffer}} V_{\text{DD}}^2 f_{\text{S}}. \tag{3}$$

The power is proportional to the square of the supply voltage (V_{DD}^2), circuit operational speed (sampling frequency f_{S}), the effective load capacitance ($C_{\text{EFF, logic}}$, $C_{\text{EFF, Buffer}}$) and the switching activity factor (α_{Logic}, α_{Buffer})[3].

The analysis of the DAC is a little complex. This is explained with the help of Fig. 5. During the sampling phase the input is sampled on the top plates of the capacitor array. Suppose differential voltage V_{x} is stored on the top plates of the capacitor array. The bottom plates of the DAC are connected to the common mode voltage (V_{CMO}) which can be treated as AC ground. After the successive approximation operation, the voltage of the top plates will converge to V_{CMO} (AC ground) and the voltage of the bottom plates will be $-V_{\text{x}}$. Suppose the

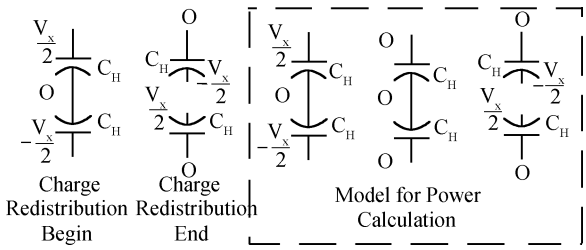

Fig. 5. Power calculation.

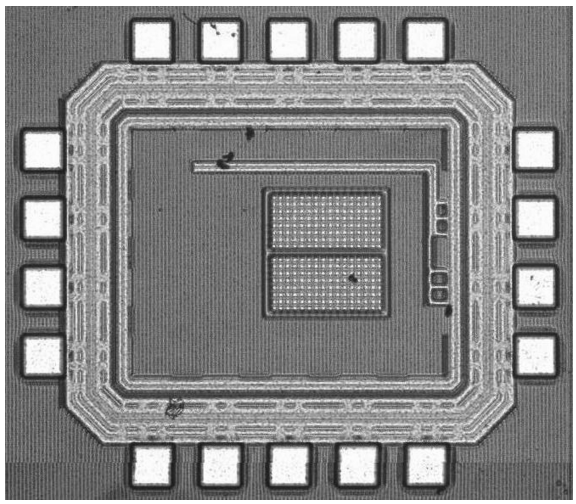

Fig. 6. Die photograph of SAR.

total capacitance of half the capacitor array is C_{H}. The energy consumption in every conversion will be $1/2 C_{\text{H}} V_{\text{x}}^2$. If the input signal is $V_{\text{m}}\sin(2\pi f_{\text{sig}} t)$, after sampling the signal will be:

$$V_{\text{x}}(n) = V_{\text{m}} \sin(2\pi f_{\text{sig}} n T_{\text{s}}) = V_{\text{m}} \sin\left(2\pi \frac{f_{\text{sig}}}{f_{\text{s}}} n\right)$$
$$= V_{\text{m}} \sin(\Omega n). \tag{4}$$

The power consumption can be calculated as:

$$P_{\text{DAC}} = \lim_{N\to\infty} \frac{1}{N T_{\text{s}}} \sum_{n=1}^{N} \frac{1}{2} C_{\text{H}} V_{\text{m}}^2 \sin^2(\Omega n)$$
$$= \lim_{N\to\infty} \frac{C_{\text{H}} V_{\text{m}}^2}{2 N T_{\text{s}}} \left(\frac{2N+1}{4} - \frac{\sin((2N+1)\Omega)}{4\sin\Omega}\right)$$
$$= \frac{C_{\text{H}} V_{\text{rms}}^2 f_{\text{s}}}{2}. \tag{5}$$

Equation (5) shows that the power of the DAC is proportional to the total capacitance of the capacitor array, the sampling frequency and the root mean square value of the input sine wave. It is noted that the power is related to the amplitude to the input sine wave. The maximum power is consumed when full scale signal is fed. In this design the reference voltages are chosen as V_{DD} and G_{ND}. The maximum amplitude of the input signal is V_{DD}, that is, $V_{\text{m}} = V_{\text{DD}}$ and $V_{\text{rms}} = V_{\text{DD}}/\sqrt{2}$. The maximum power consumption of the DAC is:

$$P_{\text{DAC}} = \frac{C_{\text{H}} V_{\text{DD}}^2 f_{\text{s}}}{4}. \tag{6}$$

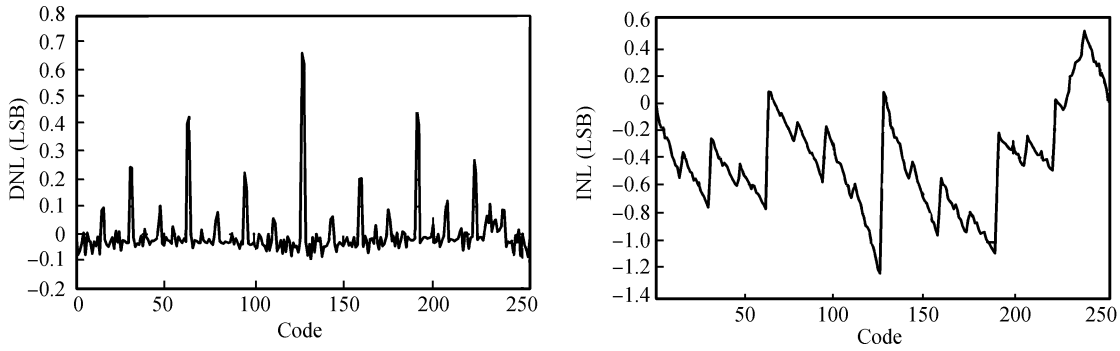

Fig. 7. Measurement DNL and INL.

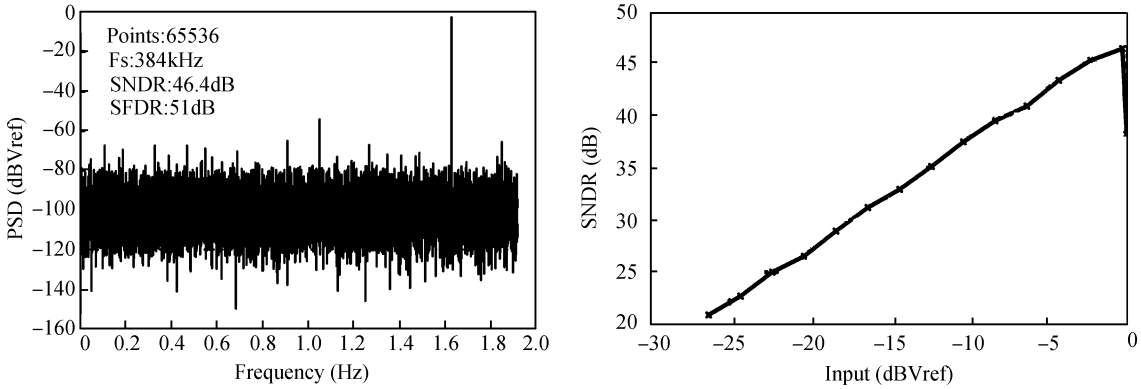

Fig. 8. Measurement spectra.

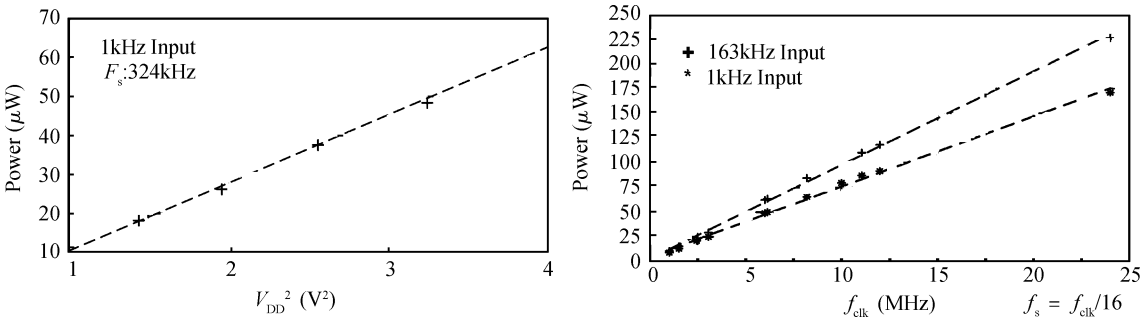

Fig. 9. Measured power consumption.

The total power consumption is then re-written as:

$$P = \frac{C_{\mathrm{H}} V_{\mathrm{DD}}^2 f_{\mathrm{S}}}{4} + \alpha_{\mathrm{Logic}} C_{\mathrm{EFF,\,logic}} V_{\mathrm{DD}}^2 f_{\mathrm{S}} + \alpha_{\mathrm{Buffer}} C_{\mathrm{EFF,\,Buffer}} V_{\mathrm{DD}}^2 f_{\mathrm{S}}. \quad (7)$$

From Eq. (7), we find that this kind of A/D has no static power consumption. The power consumption is more likely a digital circuit. To reduce the power consumption the following method will be effective:

(1) More advanced technology with finer lithography and feature size is better for low power consumption. With more accurate lithography, the matching of the capacitor will be better, so a small size for the unit capacitance can be chosen. Using advanced technology also helps to reduce the power consumption of the logic circuits.

(2) Reducing the supply voltage has a significant effect on reducing the power consumption.

(3) It is better to use separate supplies for the internal circuit and the output buffer circuit. The output buffers have to drive the large capacitance of the bonding pad and the parasitic capacitance on the PCB. If they share the same power supply, the output buffer may dominate the power consumption and one could not identify the power of the core circuits.

5. Experimental results

The SAR was fabricated in 0.18 μm 1P6M CMOS technology. The die photograph is shown in Fig. 6. The total die area including pads is 0.9 × 0.8 mm^2. The active die area is 0.25 × 0.40 mm^2. The DNL and INL is measured and shown in Fig. 7, using the code density analysis. The DNL is less than 0.7 LSB and the INL is less than 1.2 LSB. The spectrum is measured

Table 1. Performance summary.

Parameter	Value
Process	UMC 0.18 μm 1P6M CMOS
Supply voltage	1.8 V
$V_{\rm ref}$	0 V/1.8 V/, 3.6 $V_{\rm pp-diff}$
Sampling frequency	384 kHz
SNDR @ 163 kHz	46.3 dB
ENOB	7.4 bits
SFDR	51 dB
Power	63 μW
FOM	0.97 pJ/step

when a 163 kHz sine wave is fed into the chip as shown in Fig. 8. The chip is clocked at 6.144 MHz, and the sampling frequency is 384 kHz. The SNDR with varying input amplitude is also measured. The A/D achieves 46.4 peak SNDR and 51 dB SFDR. The effective number of bits (ENOB) is 7.4.

Power consumption is measured under different power supply and clock frequency conditions as shown in Fig. 9. The power is inversely proportional to the square of the power supply voltage and is proportional to the input clock frequency. The power consumption also depends on the input signal frequency. From Eq. (7), the power consumption seems to be independent of the input signal. In fact the effect of the input signal on the power consumption is reflected by the activity factor $\alpha_{\rm Buffer}$. If the input signal varies fast, the output signals need to switch all the time; this will significantly increase the power of the output buffer circuits. Because the output buffers switch more frequency with 163 kHz input than with 1 kHz input, the power consumption under 163 kHz is larger than that under 1 kHz input.

The performance is summarized in Table 1. The figure of merit can be used to evaluate the power efficient of a design. The definition is FOM = Power/$2^{\rm ENOB}$ $f_{\rm S}$. According to Table 1, the FOM of this design is nearly 1 pJ/step while the current state-of-the-art design can achieve an FOM of only 1.4 fJ/step in Ref. [4] and 65 fJ/step in Ref. [5].

There is still much to do to improve the design. Firstly, the power supply voltage should be lowered to reduce the power consumption. In Refs. [4, 5], the supplies are both 1 V while in this design the supply voltage is 1.8 V. Secondly, advanced technology can be used to obtain more compact and low power design of the digital control logic. Another benefit is that good matching of the capacitor can achieved under advanced technology and unit capacitance as well as the total capacitance can be reduced. Thirdly, the supply of the output buffers should be separate from the core circuits so that the power can be measured separately. Because the bonding PAD and the route of the PCB have a significantly larger capacitance than that inside the chip, a large proportion of the power is consumed in the output stages which can not be distinguished from that consumed by the core circuit.

6. Conclusion

An 8-bit low power successive approximation register A/D for WBSN is designed and fabricated in 0.18 μm CMOS. In order to achieve a low power design, the charge redistribution D/A is embedded in the A/D. A simple dynamic comparator is adopted. The prototype achieves 7.5ENOB when the sampling frequency varies from 64 kHz to 1.5 MHz. The power consumption varies from 10.8 to 225.7 μW. There is no static power consumption. This A/D has been used in a WBSN SoC for body temperature measurement.

References

[1] Verma N, Chandrakasan A P. An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes. IEEE J Solid-State Circuits, 2007, 42(7): 1196

[2] Schinkel D, Mensink E, Klumperink E, et al. A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 2007: 314

[3] Rabaey J M, Chandrakasan A, Nikolic B. Digital integrated circuits: a design perspective. 2nd ed. Pearson Education, 2003: 216

[4] Van Elzakker M, van Tuijl E, Geraedts P, et al. A 1.9 μW 4.4 fJ/conversion-step 10 b 1 MS/s charge-redistribution ADC. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 2008: 224

[5] Craninckx J, der Plas G V. A 65 fJ/conversion-step 0-to-50 MS/s 0-to-0.7 mW 9 b charge-sharing SAR ADC in 90 nm digital CMOS. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 2007: 246