An ultra-low-power 1 kb sub-threshold SRAM in the 180 nm CMOS process*

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Abstract: This paper presents a 1 kb sub-threshold SRAM in the 180 nm CMOS process based on an improved 11T SRAM cell with new structure. Final test results verify the function of the SRAM. The minimal operating voltage of the chip is 350 mV, where the speed is 165 kHz, the leakage power is 42 nW and the dynamic power is about 200 nW. The designed SRAM can be used in ultra-low-power SoC.

Key words: sub-threshold SRAM; 11T SRAM cell; ultra-low-power SoC

DOI: 10.1088/1674-4926/31/6/065013 **EEACC:** 2570

1. Introduction

Due to an extensive increase in the number of mobile and wireless applications, the need for low power circuits is growing rapidly. Sub-threshold logic is a potential ultra-low-power solution for those applications by lowering the operating voltage into the sub-threshold domain. Although the power consumption can be decreased to about negative two or three orders of magnitude compared to normal conditions, sub-threshold logic faces some critical problems such as low speed, process variation impact, circuit robustness, leakage, and energy efficiency.

The sub-threshold SRAM is one of the key components for sub-threshold circuits. The classical cell that contains six transistors (6T cell) is proved to malfunction under the sub-threshold voltage due to the reduction of $I_{\rm on}/I_{\rm off}$. Several papers[1−4] have been published to provide solutions.

This paper presents a 180 nm, 128 × 8 bit sub-threshold SRAM based on a type of improved 11 transistor cell (called an 11T cell). The structure was optimized to suppress the leakage current and improve the performance. This paper analyzes the 11T cell in terms of robustness, and provides the system design.

2. Cell design

The static noise margin (SNM) analysis is an effective method to analyze the robustness of a cell. In Ref. [5], an SNM analysis model was provided. Based on the principle, a conventional 6T cell is simulated. Figure 1 plots the hold and read SNM of the 6T cell from 180 mV to 1 V. 50% of the supply voltage (VDD) is taken as threshold voltage and is plotted as ideal curve. From Fig. 1, the read SNM is degraded greatly which means that the 6T cell cannot be read properly. Another severe problem is the process variation. Monte Carlo (MC) analysis is another simulation method to find the impacts of process variation. A 5000 point MC simulation was carried out to find the impact on read and hold SNM caused by the size fluctuations, plotted in Fig. 2. The x axis is the static noise margin and the y axis records the statistics occurrences of SNM. The read occurrences of logic ‘1’ distribute mostly between 0 and 0.05 V which means that the read SNM is degraded greatly. In contrast, the hold operation does not degrade much.

In order to improve the read SNM, a 10T cell[2] (seen in Fig. 3) is provided. An additional tri-inverter is added to connect node QN to the read-bit-line (RBL) directly. There are three advantages for the 10T cell. Firstly, the tri-inverter between the memory cell and the RBL makes the read SNM almost the same as the hold operation in theory. Secondly, the tri-

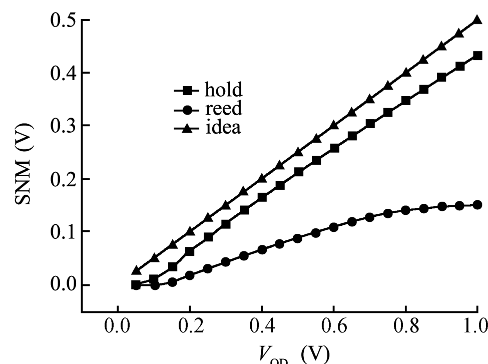

Fig. 1. Hold and read SNM of the 6T cell.

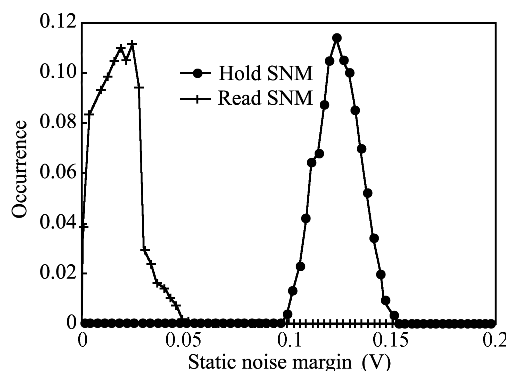

Fig. 2. Monte-Carlo analysis of hold and read SNM of 6T.

* Project supported by the National Natural Science Foundation of China (No. 60906010).

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Received 16 November 2009, revised manuscript received 5 February 2010

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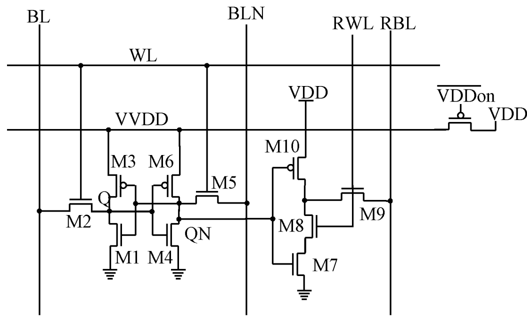


Fig. 3. 10T cell structure.

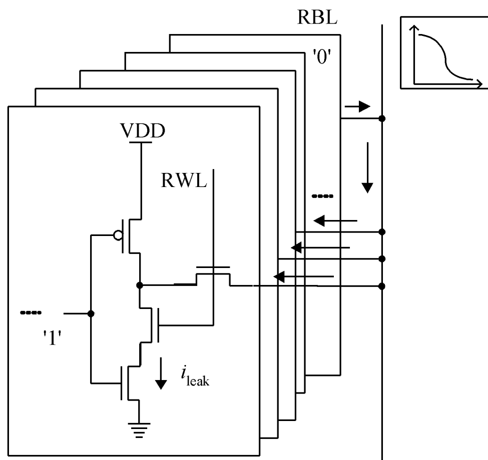


Fig. 4. Data-dependent leakage current.

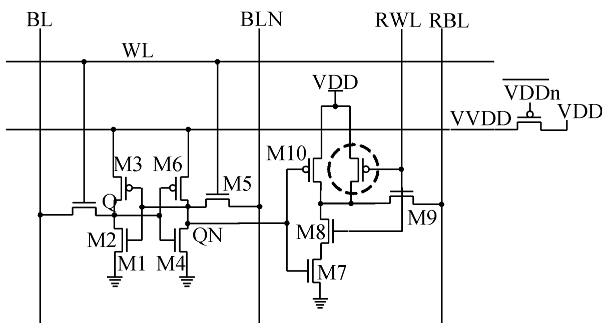
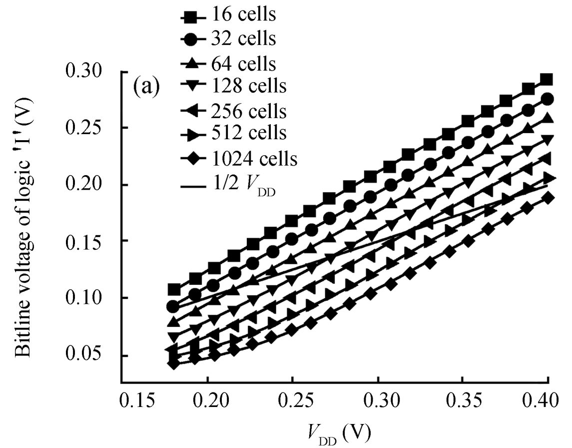


Fig. 5. 11T cell.



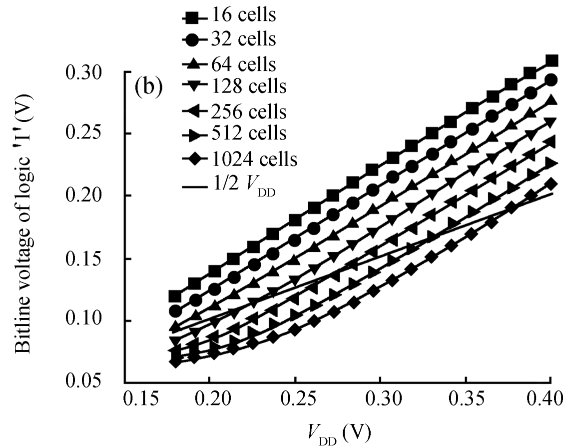


Fig. 6. RBL logic ‘1’ of different cell numbers. (a) 10T. (b) 11T.

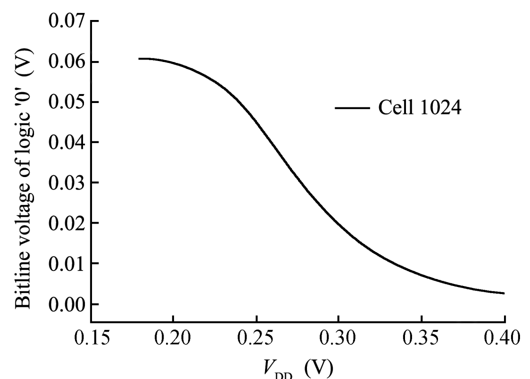


Fig. 7. Logic ‘0’ of RBL under different V_{DD} (1k cells per bit-line).

inverter is also designed to reduce the leakage from the buffer into the RBL when the cell is not enabled. This allows more cells to share the same RBL. Finally, another improvement is the use of virtual-VDD (VVDD) to improve the write stability by increasing the write SNM[2].

However, there is a drawback of 10T. When N 10T cells are connected by one RBL, the value of RBL depends on the value of untouched cells due to the leakage path from the RBL to ground during the read operation. In the extreme case, $N-1$ cells hold ‘0’ and one holds ‘1’. The leakage current from the RBL to the ground through $N-1$ cells would lower the logic ‘1’ (seen in Fig. 4). That would limit the number of cells that can be connected together.

An 11T cell (seen in Fig. 5) is designed to mitigate the leakage problem of 10T. An extra M_{11} (circled in Fig. 5) is added to 10T. The unselected cells seem like ‘1’ to RBL. There are two cases to be considered. One is that only one cell saves ‘0’. Figure 6 shows a comparison between the two types of cell. The simulations indicate that the number of 11T cells can be twice that of 10T cells. In Fig. 6, the threshold voltage of ‘1’ is set as 50% V_{DD} for safety. Another condition is that only one cell holds ‘1’. Figure 7 illustrates the simulation results of 1 k 11T cells per RBL under different supply voltages. In this 180 nm process, the logic ‘0’ of RBL is not affected greatly because the low voltage level is less than 0.06 V.

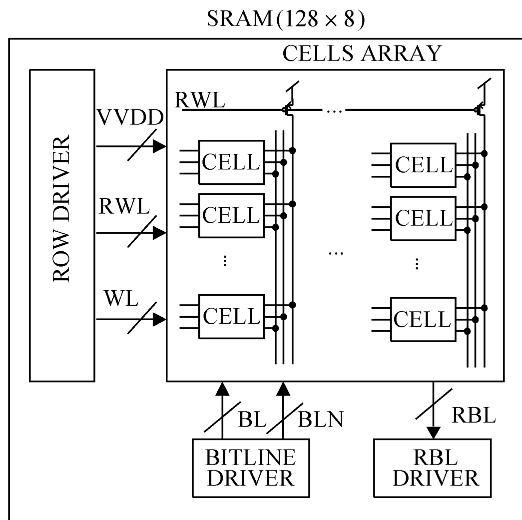


Fig. 8. SRAM structure.

Table 1. Performance summary.

Parameter	Value			
Voltage (mV)	350	400	450	500
Leakage power (μW)	0.042	0.504	1.089	1.810
Dynamic power (μW)	0.2	4.456	5.859	7.540
Operating frequency (kHz)	165	250	500	1000

3. System structure

Based on the designed 11T cell, a 128 × 8 bit SRAM (seen in Fig. 8) was put forward. It mainly contains three parts: a 128 × 8 cell core; an ROW DRIVER that is synthesized by a standard library and can generate the decoded signals as RWL, WL and VVDD; IO drive modules (BITL Driver and RBL Driver). Unlike the classic structure, the RBL is pulled up to V_{DD} by a PMOS transistor during the idle time and floats during the read operation. There are four reasons for this:

(1). The conventional pre-charge process of the RBL is bypassed to accelerate the speed. In the classical structure, the RBL and BL are the same line. Before read operation, the bit-line should be pre-charged to V_{DD}. The 11T cell separates the bit-line and read-bit-line to provide a possibility of bypassing the pre-charge process.

(2). There is an obvious drawback to connecting the RBL to VDD directly because of the leakage current through the tri-buffer when all 10T cells save ‘0’ (seen in Fig. 7). However the M11 makes all 11T cells seem like ‘1’ to RBL to suppress the leakage problem.

(3). The system stability is enhanced. In the ultra-low voltage domain, the float RBL will be disturbed easily due to the random noise by parasitic capacitance.

(4). The speed is accelerated because the delay time of reading logic ‘1’ is zero, which means that the delay only depends on the current discharge through the NMOS stack. In this technology, NMOS is much stronger than PMOS (by about ten times). The reverse-short-channel-effect (RSCE)[6] is a very effective method to accelerate the speed. As a byproduct of HALO, the RSCE can increase the I_{on} effectively by enlarging the length of NMOS.

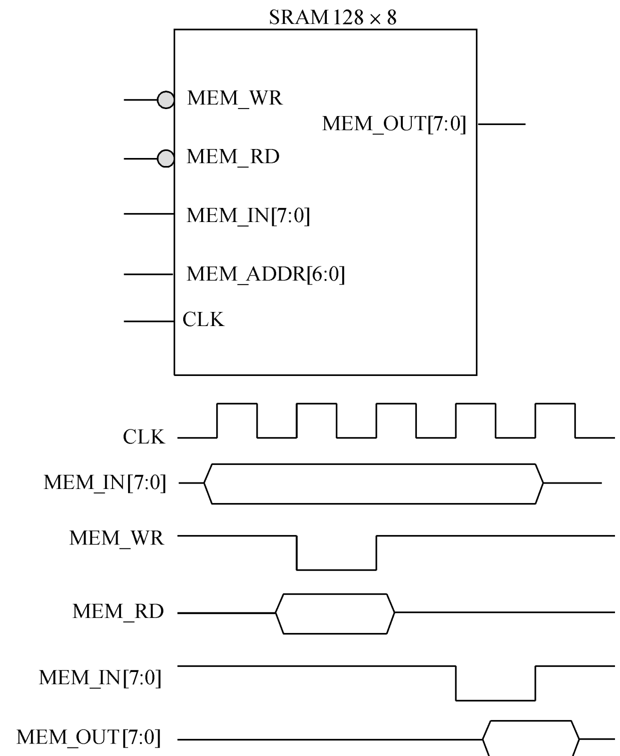


Fig. 9. Interface and timing diagram of SRAM 128 × 8.

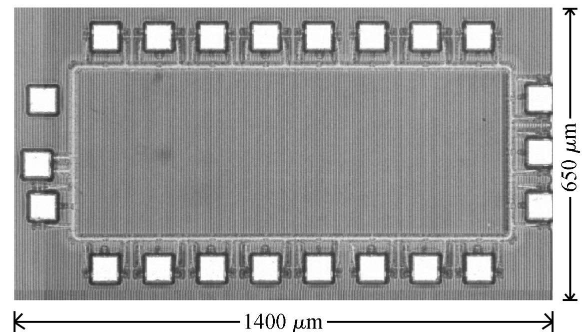


Fig. 10. Die photo.

The SRAM’s top interface and timing diagram are plotted in Fig. 9. The MEM_WR and MEM_RD that is valid in low level is an input signal to control the reading and writing operation. The MEM_IN and MEM_OUT are input and output separately. The MEM_ADDR[6:0] is the address. The operating mode of the SRAM is asynchronous; however, the clock signal (‘CLK’ in Fig. 9) appears to generate the VVDD signal. The interface is simple and compatible with 8051. The timing is flexible in that the setup and hold time of the input data can even be zero due to the low speed. For the same reason, the hold time of the output data is long enough for external reading.

4. Test results

The chip size is about 1400 × 650 μm^2 (seen in Fig. 10). It is fabricated by standard UMC 180 nm technology. The test results of the chip are listed in Table 1.

The final test verifies the SRAM function. The chip can run up to 165 kHz @ 350 mV, where leakage power is 42 nW and

dynamic power is about 200 nW. From Table 1, the lowest operating voltage is 350 mV and leakage power is 42 nW, which fits for ultra-low-power applications. The results are close to the post simulation result of TT mode. The speed bottleneck is the decoding time of the address, which is about 70% of the whole time. The ROW DRIVER (seen in Fig. 8) part is synthesized by a conventional standard library. The fast decoder should be designed to accelerate the speed. Another problem is the lowest operating voltage that is beyond expectations due to the parasitic capacity and transistor characteristic.

5. Conclusions

From the test results, three conclusions can be made as follows. Firstly, it is possible to design a sub-threshold SRAM under the standard 180 nm CMOS process. Secondly, post-simulation can be close to a real test to some extent, which is very important for designers. Finally, careful fan-out design can optimize the performance of the SRAM.

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