A 1.5 V 7.656 GHz PLL with I/Q outputs for a UWB synthesizer*

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Abstract: A fully integrated CMOS phase-locked loop (PLL) which can synthesize a quadrature output frequency of 7.656 GHz is presented. The proposed PLL can be employed as a building block for an MB-OFDM UWB frequency synthesizer. To achieve fast loop settling, integer-N architecture operating with 66 MHz reference frequency and wide-band QVCO are implemented. I/Q carriers are generated by two bottom-series cross-coupled LC VCOs. Realized in 0.18 μm CMOS technology, this PLL consumes 16 mA current (including buffers) from a 1.5 V supply and the phase noise is –109.6 dBc/Hz at 1 MHz offset. The measured oscillation frequency shows that the QVCO has a range of 6.95 to 8.73 GHz. The core circuit occupies an area of 1×0.5 mm^2.

Key words: 7.656-GHz; frequency synthesizer; PLL; MB-OFDM; CMOS
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1. Introduction

Nowadays, the prospect of wireless data transmission at rates of hundreds of Mbps arouses the interest of consumer electronics in wireless personal area network (WPAN) communication systems with ranges of 10 m. Ultra-wideband (UWB) is becoming a promising technique to achieve higher data rates in wireless communications. These networks are designed to replace cables between different devices in the home and to provide new applications. Examples of possible applications include wireless USB and high-definition video streaming[1].

The multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB proposal divides the spectrum into 14 channels (bands) with a bandwidth of 528 MHz from 3.1 to 10.6 GHz, using frequency hopping methods for signal transmission, where a switching time of less than 9.47 ns is required[2].

As it is very difficult to implement a phase-locked loop (PLL) which settles in nanoseconds, several frequency synthesizers based on SSB frequency mixing have been proposed recently[1,3–5]. Among them, a frequency synthesizer for hopping carrier generation usually consists of a multiplexer (MUX), a PLL and a single-sideband (SSB) mixer. The main problem of this synthesizer is poor image subjection as it uses many nonlinear components, such as dividers, MUXs and SSB mixers on the signal route. Similar to Ref. [5], we propose a synthesizer for bands 7 to 11, alleviating the image subjection problem and achieving a good compromise between performance and silicon area.

The objective in this design is to provide a fixed frequency at 7.656 GHz, which is the central carrier frequency from bands 7 to 11,with quad phases for further operation in frequency additions and subtractions. The PLL circuit is implemented as a part of a frequency synthesizer for UWB band groups 3 and 6.

2. Synthesizer and PLL architectures

The proposed synthesizer depicted in Fig. 1 can be an alternative solution for MB-OFDM UWB carrier generation. It employs only one SSB mixer, one MUX and two PLLs to generate 5 bands of band groups 3 and 6 distributed from 6 to 9 GHz with less than 3 ns switching time. Because fewer nonlinear components are used in our design, spurious tones are alleviated a lot.

The principle of operation is as follows: the upper PLL generates a fixed I/Q frequency of 7.656 GHz, whereas the lower PLL produces a fixed frequency of 4.224 GHz. A frequency multiplexer (MUX) in front of the tri-mode divider[5] selects the 2112 MHz and 1056 MHz signals for frequency additions and subtractions, which are produced by two stages of a static divide-by-2 frequency divider in the feedback path of the 4.224 GHz PLL. The subsequent programmable tri-mode divider provides DC or quadrature signals with different I/Q phase sequences of 528 MHz and 1056 MHz, allowing the SSB mixer to create 5 synthesized frequencies. By quadrature mixing the 7.656 GHz signal with either $\pm$1056 MHz or $\pm$528 MHz or DC using a quadrature SSB mixer, the I/Q frequencies of bands 7 to 11 are generated respectively.

The 7.656 GHz PLL can be used as a building block for the frequency synthesizer shown in Fig. 2. This PLL is implemented by using conventional charge pump integer-N ar-

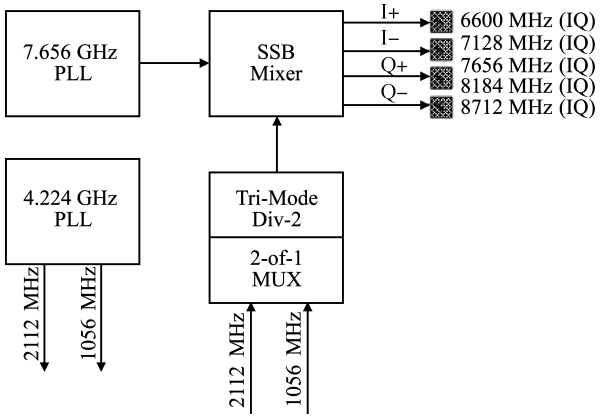

Fig. 1. Diagram of the proposed frequency synthesizer.

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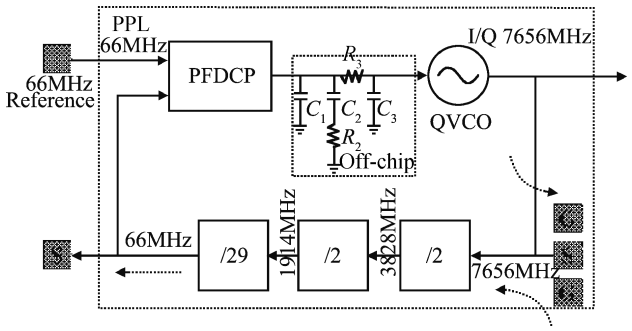

Fig. 2. Diagram of the 7.656 GHz PLL.

Table 1. Summary of the PLL parameters.

Parameter	Value
Loop bandwidth	$2\pi \times 125$ kHz
I_{cp}	1 mA
Division ratio	116
K_{VCO}	$2\pi \times 175$ MHz/V
Phase margin	60°
C_1	470 pF
C_2	8.88 nF
C_3	47 pF
R_2	560 Ω
R_3	2.7 kΩ

chitecture to generate a signal of 7.656 GHz by a divider of 29 and a 66 MHz reference clock, as shown in Fig. 3. This architecture possesses lower complexity than other architectures such as fractional-N architecture. It comprises two bottom-series cross-coupled VCOs for generating in-phase and quadrature-phase outputs, a frequency divide-by-29 circuit, a tri-state phase-frequency detector (PFD), a current-steering charge pump (CP), and an off-chip third-order passive loop filter. As MUX based synthesizers do not require a fast settling time from the PLL (all PLLs are active all the time), the major work in our design is to improve the signal purity and decrease the reference spurs.

Spurious tones resulting from the ripple on the VCO control line do not get much attenuation from the loop filter because of the wide loop bandwidth. Matching of the current sources in the charge pump is critical to minimize these tones.

3. Circuit implementation

3.1. LPF phase-locked loop design

The design of the loop filter is a compromise between the area consumed in the components and the attenuation to the ripple and phase noise. To gain better phase noise performance, a passive third-order filter is used, as shown in Fig. 2. The low-pass filter has a zero and two poles comprising a third-order system to accomplish the maximum attenuation to the spurious tones and phase noise. The loop bandwidth is controlled by the charge pump current and it is computed to be around 125 kHz. The third-order loop filter is implemented with off-chip discrete components, providing more flexibility than an on-chip solution. The calculated component values of the loop filter are listed in Table 1.

3.2. Quadrature VCO

Conventionally, an oscillation signal with quad phases can be realized by a VCO driving a poly-phase phase-shifting network, a doubled-frequency VCO following a frequency divider, two oscillators coupled by each other, or a ring oscillator. For such a high frequency, the former two approaches are impractical for the large amount of power consumption required in the drivers compensating the power loss in the passive poly-phase network and the high-speed dividers respectively.

As shown in Fig. 3, the 7 GHz quadrature VCO employs a modified bottom-series structure with two symmetric coupled LC oscillators[6,7]. The LC-type VCOs include a complementary cross-coupled NMOS/PMOS pair for generation of negative conductance and LC resonators consisting of a differential coil, accumulation-mode nMOS varactors and coarse tuning capacitor array. To cover the VCO tuning range, conventional coarse tuning capacitances composed of MIM capacitors and switches are used in the switched capacitor array based on binary-weighted architecture. Through switches, the binary-weighted capacitors can be switched in and out of the LC tank[8].

The device sizes are optimized for best performance such as phase noise, phase accuracy and amplitude imbalance, especially the switching pairs in series with the coupling transistors used in the QVCO. Inductors are used to improve the phase noise performance and reduce the power dissipation. A MIM capacitor is used to increase the overall quality factor of the LC tank. The inductor is designed to have a quality factor of more than 10 over the operating frequency.

As a result, the QVCO covers 6.75–8.67 GHz and draws 12 mA (including buffers) from 1.5 V supply, and the phase noise level is –114 dBc/Hz at 1 MHz offset. A greater than 25% tuning range to compensate for process, voltage, and temperature (PVT) variations is achieved mainly by digitally controlled MOS capacitors.

3.3. Dividers

The prescaler is a crucial block in the PLL since it works at the highest frequency. It includes a chain of dividers with division ratios of two, two and twenty-nine ($2 \times 2 \times 29 = 116$) as depicted in Fig. 4. The first two stages are divide-by-2 circuits, while the divide-by-29 circuit consists of 4 stages of divide-by-2or3 circuits. All dividers are based on D-flip-flops, and each flip-flop includes two current-mode logic (CML) D-latches as shown in Fig. 5. Furthermore, they are optimized with different sizes for different frequency requirements.

One of the critical contributions to the I/Q phase mismatch of the QVCO outputs is the mismatch in its output loading, which is typically dominated by the input capacitance of the subsequent circuit. A usual approach is to add a dummy divide-by-2 circuit at the output of the QVCO to preserve the symmetry with a waste of power consumption. In our design, a subsequent dummy buffer instead of a dummy divide-by-2 circuit is added. The buffer can be optimized as a low power block and maintain the symmetry.

The whole divider chain is implemented with differential signaling, which is necessary for correct PFD operation.

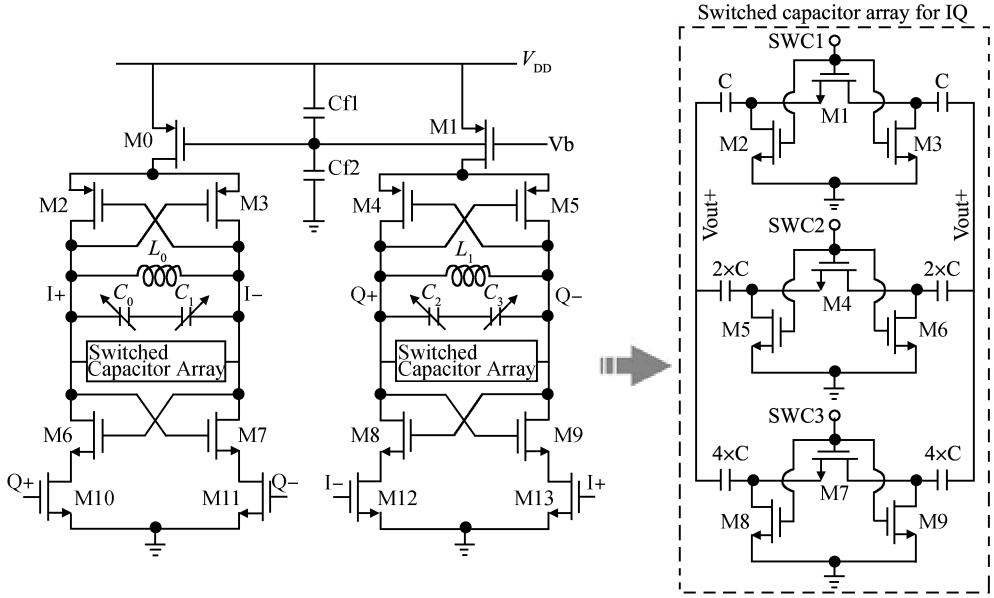

Fig. 3. Schematic of the improved QVCO.

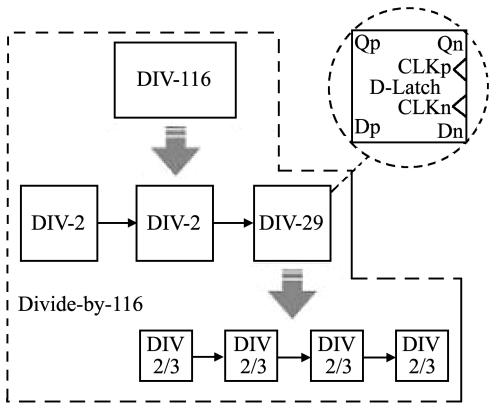

Fig. 4. Diagram of the dividers in the 7.656 GHz PLL.

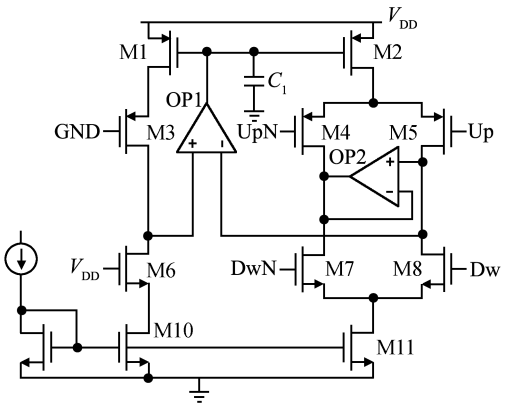

Fig. 6. Schematic of the improved charge-pump circuit.

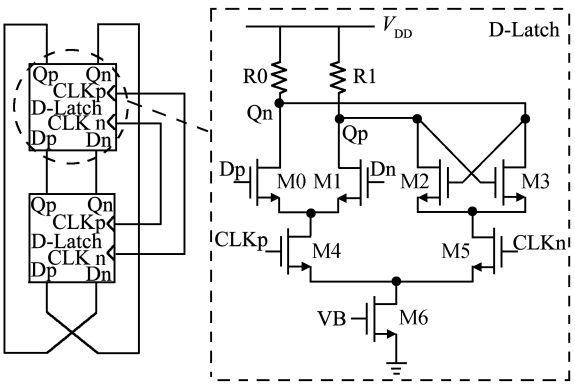

Fig. 5. Schematic of the divide-by-2 circuit.

3.4. CP and PFD

An improved charge-averaging charge pump as proposed in Ref. [9] is implemented in this PLL shown in Fig. 6. The original charge-averaging charge pump is proposed by Koo[10]. There are still some defects in his scheme. The first arises from the four current sources, which are difficult to match in practice. The paths from the PFD output to these four current sources make it difficult to equalize the delays. These non-idealities lead to spurs in the output spectrum. In our design, a new scheme is proposed as shown in Fig. 7. This new scheme decreases the power by 1/3 and eliminates the practical defects in the original. The proposed scheme can strongly reduce the energy of spurs. The simulation results show this new scheme outputs a flat voltage curve in a locked state and can thus effectively suppress fraction spurs.

The phase-frequency detector uses a dual D-flip-flop structure. When the PLL is in the locked state, some delay is inserted in the reset path of the PFD to generate a minimum pulse width to prevent a dead zone, referenced in Ref. [11]. The buffers and inverters at the outputs are used to minimize the timing error between the UP and UP-/DN and DN- signals. The NAND and OR gates as the basic building blocks of the PFD are implemented with differential cascaded voltage switching logic (DCVSL). With this kind of PFD, the complementary control signals at the charge pump input can be perfectly matched by

Table 2. Performance summary and comparison.

Parameter	This work	Leung[12]	Chiu[13]
Output frequency (GHz)	6.95–8.73	5.45–5.65	5.47–5.65
Quadrature output	Yes	Yes	No
Phase noise @ 1 MHz (dBc/Hz)	−109.6	−111	−110.8
Supply voltage (V)	1.5	1	1.8
Power consumption (mA)	16 (including buffers)	27.5	9
Reference frequency (MHz)	66	10	10
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Core area (mm^2)	1 × 0.5	1.3 × 0.76	0.83 × 0.74

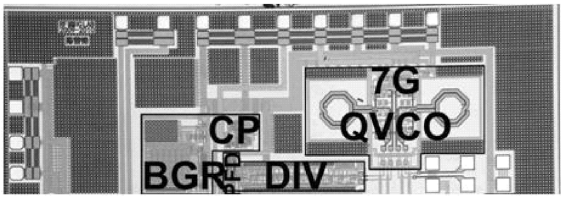

Fig. 7. Chip photograph.

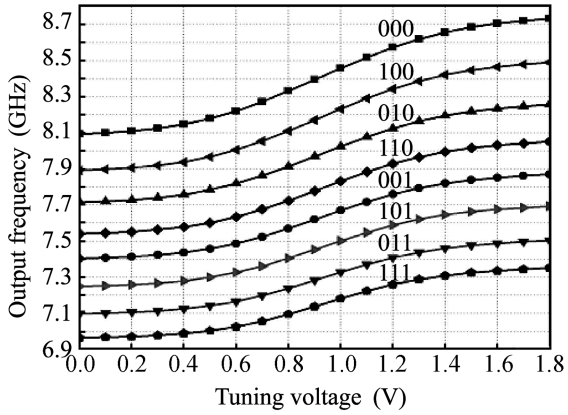

Fig. 8. Measured tuning curves of QVCO.

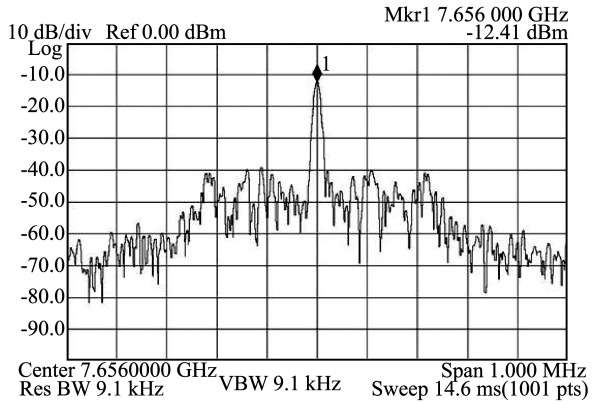

Fig. 9. Measured output spectrum of the locked PLL

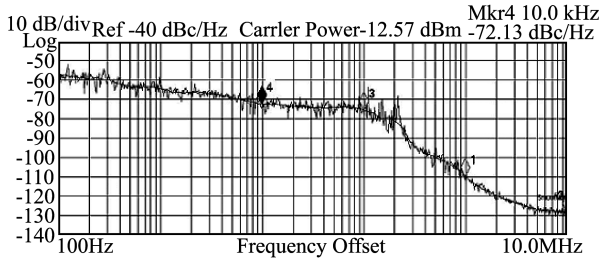

Fig. 10. Measured phase noise performance.

a symmetrical layout. The phase noise and spurs are hence greatly reduced.

4. Experimental results

This PLL has been realized in a 0.18 μm CMOS process. The chip photograph is shown in Fig. 7. It has an active area of 1 × 0.5 mm^2. The power dissipation is 16.5 mW from a 1.5 V supply including buffers. The chip was mounted on a 2-layer FR4 board for testing.

As shown in Fig. 8, the VCO can be tuned from 6.95 to 8.73 GHz. The eight curves are obtained by changing the digital tuning word A0–A1–A2. Overlaps between curves occur approximately 50%.

As shown in Figs. 9 and 10, the PLL is locked at 7.656 GHz and achieves a phase noise of –109.6 dBc/Hz at 1 MHz offset, with an external reference of 66 MHz generated from our Agilent N5182A MXG vector signal generator. A good phase noise can be easily achieved with a better reference from either a good crystal oscillator or a better signal generator.

Table 2 summarizes the measured performance of the proposed PLL and presents a performance comparison with some other PLLs. As the results in Table 2 demonstrate, the proposed PLL achieves higher frequency, wider tuning range, and smaller chip core area than previous work with similar phase noise and low power consumption in the same technology.

5. Conclusion

A fully integrated 7.656 GHz CMOS PLL for UWB applications was described. This PLL was implemented as a part of an SSB-mixing-based synthesizer for an MB-OFDM UWB system for band groups 3 and 6. The PLL consumes 24 mW power and the phase noise is –109.6 dBc/Hz at 1 MHz offset. The core area of the chip is 0.5 mm^2. Operating at 66 MHz reference frequency, the proposed PLL can synthesize a quadrature output frequency from 6.95 to 8.73 GHz.

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