Growth of strained-Si material using low-temperature Si combined with ion implantation technology*

Yang Hongdong(杨洪东)†, Yu Qi(于奇), Wang Xiangzhan(王向展), Li Jingchun(李竞春), Ning Ning(宁宁), and Yang Mohua(杨谟华)

(State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology, Chengdu 610054, China)

Abstract: In order to fabricate strained-Si MOSFETs, we present a method to prepare strained-Si material with high-quality surface and ultra-thin SiGe virtual substrate. By sandwiching a low-temperature Si (LT-Si) layer between a Si buffer and a pseudomorphic $Si_{0.8}Ge_{0.2}$ layer, the surface roughness root mean square (RMS) is 1.02 nm and the defect density is 10^6 cm^{-2} owing to the misfit dislocations restricted to the LT-Si layer and the threading dislocations suppressed from penetrating into the $Si_{0.8}Ge_{0.2}$ layer. By employing P^+ implantation and rapid thermal annealing, the strain relaxation degree of the $Si_{0.8}Ge_{0.2}$ layer increases from 85.09% to 96.41% and relaxation is more uniform. Meanwhile, the RMS (1.1 nm) varies a little and the defect density varies little. According to the results, the method of combining an LT-Si layer with ion implantation can prepare high-quality strained-Si material with a high relaxation degree and ultra-thin SiGe virtual substrate to meet the requirements of device applications.

Key words: low-temperature silicon; strained silicon; ion implantation; SiGe virtual substrate
DOI: 10.1088/1674-4926/31/6/063001 **PACC:** 8115N; 6170T; 7360F

1. Introduction

Because of the ability to enhance the electron and hole mobility[1−3], strained-Si technology including process-induced uniaxial[4−7] and substrate-induced biaxial stress[8] has been widely researched and applied. Process-induced strain is used in industrial production, attributed to its relatively simple implementation, while substrate-biaxial strain has not been adopted yet. The main reason is the difficulty of growing the low defect density, low surface roughness, high relaxation degree and thin SiGe virtual substrate.

To grow relaxed SiGe virtual substrate, several technologies have been developed, such as the grading SiGe buffer layer technique[9, 10], ion implantation technology[11−14] and low-temperature Si (LT-Si) technology[15−18]. A high-quality and high relaxation degree SiGe virtual substrate can be obtained by sufficiently thick grading SiGe buffer, but a SiGe buffer layer of several microns is so thick that it may deteriorate the performance of the device due to the self-heating effect[19]. Ion implantation technology can achieve a high relaxation degree and ultra-thin SiGe virtual substrate, while the quality of the relaxed SiGe layer is usually destroyed[11]. The LT-Si technology has availability of a high-quality and thin relaxed SiGe virtual substrate, but the degree of strain relaxation is limited by the thickness of the SiGe layer[20].

In this paper, a high-quality strained-Si material is firstly grown using solid-source molecular beam epitaxy (MBE) with sandwiching an LT-Si layer between a Si buffer and a pseudomorphic $Si_{0.8}Ge_{0.2}$ layer. Then, P^+ implantation, due to the increasing amount of dislocation nucleation sources, is employed to increase the degree of strain relaxation. Rapid thermal annealing (RTA), due to gliding of dislocations, is used to improve the strain uniformity.

2. Experiment

A key factor of biaxial strained-Si devices is the preparation of high-quality biaxial strained-Si material with low defect density, low surface roughness, high relaxation degree, and thin relaxed SiGe virtual substrates. For one thing, the stress in pseudomorphic SiGe is released under the critical thickness by misfit dislocation formation in the LT-Si layer, which simultaneously suppresses threading dislocation formation in relaxed SiGe[16−18]. This characteristic of the LT-Si layer can obtain high-quality biaxial strained-Si material with thin relaxed SiGe virtual substrate. For another, ion implantation can induce point defects to form misfit dislocations with lower nuclear energy due to heterogeneous nucleation and dislocation slip easily in the thermal process. So the relaxation degree and uniformity of strain are improved by increasing the point defects in the LT-Si layer induced by ion implantation and the rapid thermal annealing (RTA) process respectively.

According to the discussion above, we designed the epitaxial structure shown in Fig. 1. All epitaxial layers are grown on ϕ-75-mm ⟨100⟩ N-type Si substrate using solid-source MBE. The key processing is as follows.

Firstly, a 10 nm Si buffer layer was grown at a temperature of 700 °C after cleaning. Secondly, a 100 nm LT-Si layer was grown at 400 °C. Following the LT-Si layer, a 500 nm $Si_{0.8}Ge_{0.2}$ layer was grown at 550 °C. Finally, an 18 nm Si layer was grown at 550 °C as well and the ultimate material structure was strained-Si/relaxed $Si_{0.8}Ge_{0.2}$/ LT-Si/Si buffer/Si

* Project supported by the Funds of the State Key Laboratory of Electronic Thin Films and Integrated Devices, China (No. D0200 401030108KD0022).
† Corresponding author. Email: hongdong_yang@163.com
Received 20 November 2009, revised manuscript received 12 February 2010

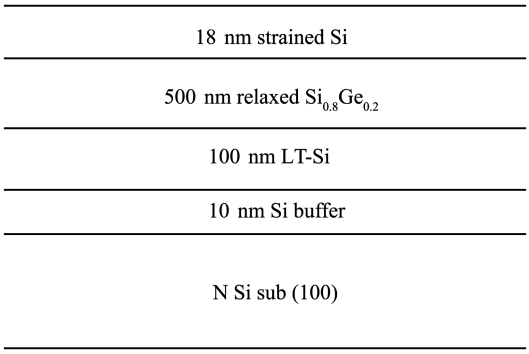

Fig. 1. Structure of the epitaxy layers for biaxial strained-Si material based on LT-Si technology.

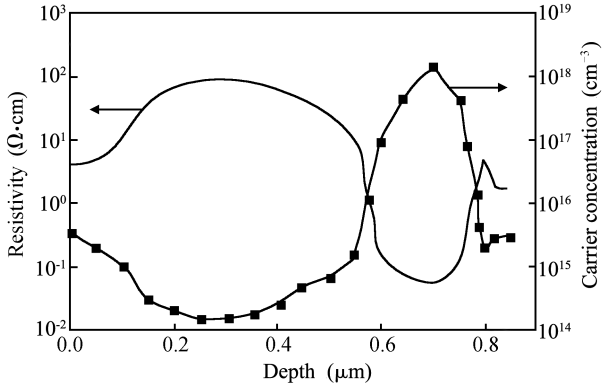

Fig. 2. P^+ distribution within the sample after ion implantation and RTA.

substrate.

In addition, to protect the surface from destruction by ion implantation, a 20 nm SiO_2 layer was deposited on the surface before ion implantation. Subsequently, P^+ implantation was carried out at an energy of 140 keV and dose of 6×10^{12} cm^{-2}. Finally, the sample was rapid thermal annealed for 15 s at 1000 °C in N_2 atmosphere and then cleaned by HF solution to remove the SiO_2 layer.

The sample was investigated by atomic force microscopy (AFM), transmission electron microscopy (TEM), double crystal X-ray diffraction (DCXRD) and a spreading resistance tester.

3. Results and discussion

P^+ distribution within the sample after ion implantation and RTA is investigated by a spreading resistance tester. As shown in Fig. 2, the P^+ peak value is 2×10^{18} cm^{-3} and the position lies at a depth of 0.7 μm. The resistivity nearly equals that of Si substrate at the 0.5 μm position. From the data, P^+ mainly distributes underneath the LT-Si layer with little P^+ in the $Si_{0.8}Ge_{0.2}$ layer, which meets the design goal. Meanwhile, the results also suggest that the implantation energy is reasonable. Induced by P^+ implantation in the LT-Si layer, the point defects act as the nuclear sources of misfit dislocations. Due to heterogeneous nucleation, the dislocation nuclear energy of point defects is so low that numerous dislocations are easily formed in the annealing process. The result leads to improvement of the strain relaxation degree of the $Si_{0.8}Ge_{0.2}$ layer. At the same time, P^+ is prevented from implanting into the relaxed $Si_{0.8}Ge_{0.2}$ layer, which avoids inducing point defects in the relaxed $Si_{0.8}Ge_{0.2}$ and strained-Si layers and protects crystal quality.

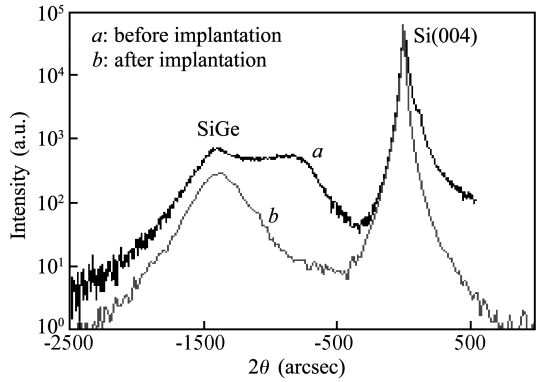

Fig. 3. DCXRD rocking curves of the sample before (curve *a*) and after (curve *b*) P^+ implantation and RTA.

The strain relaxation degree of $Si_{0.8}Ge_{0.2}$ virtual substrate is investigated by DCXRD technology before and after P^+ implantation respectively. As shown in Fig. 3, curves *a* and *b* are the rocking curves of the sample before P^+ implantation and RTA respectively. CuKα1 acts as an X-ray source, whose wave length is $\lambda = 0.154056$ nm. The Bragg angle of the Si substrate on (004) is $\theta_{\text{Bragg}} = 34.5646^{\circ}$. Because of having a greater lattice parameter, the diffraction peak of the $Si_{0.8}Ge_{0.2}$ layer lies to the left of the Si substrate. From the DCXRD data, the degree of strain relaxation is 85.09% through calculation[21], which is incompletely relaxed. At the same time, the full width of half maximum (FWHM) of relaxed $Si_{0.8}Ge_{0.2}$ is much wider, which indicates that the strain has a poor uniformity of relaxation. The reason for the low relaxation degree and nonuniform strain is that the relaxation mechanism changes at low temperature compared with high temperature. The relaxation mechanism of pseudomorphic SiGe is a dislocation propagating mechanism at high temperature to release misfit strain, while it is a dislocation forming mechanism at low temperature[22]. So, the degree of strain relaxation is mainly decided by the amount of dislocation nuclear sources in the LT-Si layer.

After P^+ implantation and RTA, the peak of relaxed $Si_{0.8}Ge_{0.2}$ (curve *b* in Fig. 3) shifts to the right due to shortening of the lattice vertical spacing. This suggests that the strain relaxation degree of relaxed $Si_{0.8}Ge_{0.2}$ layer increases. By calculation, the strain relaxation degree increases to 96.41%. The point defects, induced by P^+ implantation in the LT-Si layer, become misfit dislocation heterogeneous nucleation sources[13, 23]. Then, a large number of misfit dislocations forms to release the strain in the incompletely relaxed $Si_{0.8}Ge_{0.2}$ layer at RTA processing. Therefore, the strain can be completely relaxed by increasing the dose of ion implantation. Furthermore, the FWHM of the relaxed $Si_{0.8}Ge_{0.2}$ peak is noticeably narrower compared to that before P^+ implantation and RTA. This indicates that the uniformity of strain relaxation increases, attributed to dislocation slip at RTA processing and realignment of the misfit dislocation network[17].

As shown in Fig. 4, we study the dislocation formation in-

Fig. 4. TEM image of a cross section of $Si_{0.8}Ge_{0.2}$/LT-Si/Si after RTA.

side the sample by TEM. From the TEM image, it is clearly seen that there are many defects in the Si buffer near the surface of the Si substrate, which result from surface damage by chemical mechanical polishing (CMP) etc. The Si buffer grown at 700 °C separates the overgrown layer and improves the quality of the following LT-Si layer, providing a good surface to grow pseudomorphic $Si_{0.8}Ge_{0.2}$ with a smooth $Si_{0.8}Ge_{0.2}$/LT-Si interface. Furthermore, it is found that numerous dislocations form in the LT-Si layer to release the strain in the pseudomorphic $Si_{0.8}Ge_{0.2}$ layer. However, the dislocations are held back from climbing up into the relaxed $Si_{0.8}Ge_{0.2}$ layer and no dislocation is observed in the relaxed $Si_{0.8}Ge_{0.2}$ layer under the TEM test resolution. This result indicates that the LT-Si layer not only generates misfit dislocations to release the strain of the pseudomorphic $Si_{0.8}Ge_{0.2}$, but also suppresses the threading dislocation penetration into the relaxed $Si_{0.8}Ge_{0.2}$ layer. The result provides the condition to obtain a high-quality surface with a low defect density by suppressing threading dislocations in the $Si_{0.8}Ge_{0.2}$ layer.

The surface morphology of the sample is investigated by AFM before and after P^+ implantation and RTA. Figure 5(a) shows an AFM testing photo with a scanning range of 5×5 μm^2 before P^+ implantation. Figure 5(b) shows an AFM testing photo with a scanning range of 10×10 μm^2 after P^+ implantation and RTA and removing the SiO_2 layer. From Fig. 5, it is clearly seen that there is cross-hatching along direction [110] which is caused by surface fluctuations arising from the misfit dislocation network around the $Si_{0.8}Ge_{0.2}$/LT-Si interface. By calculation, the surface roughness root mean square (RMS) is 1.02 nm before P^+ implantation and the defect density is 10^6 cm^{-2}, which is less than that from using ion implantation solely [(3–4) $\times$ 10^7 cm^{-2}][11]. The results indicate that threading dislocations are suppressed effectively when pseudomorphic $Si_{0.8}Ge_{0.2}$ releases the strain. After P^+ implantation and RTA, the RMS becomes 1.1 nm partly due to the different scanning scope and the defect density hardly varies. The results suggest that the SiO_2 layer is able to protect the surface from

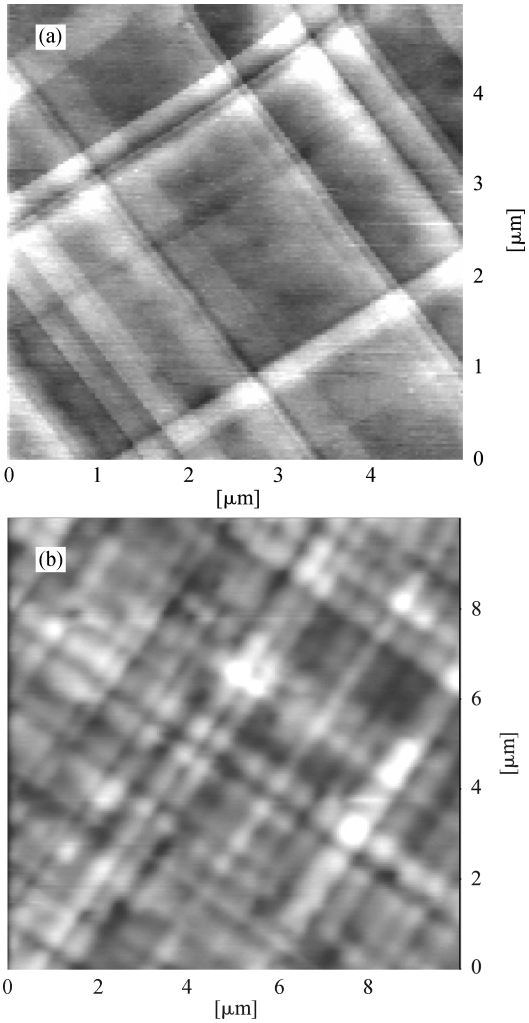

Fig. 5. AFM testing photos of the sample. (a) Before P^+ implantation and RTA. (b) After P^+ implantation and RTA.

damage by ion implantation. The surface is sufficiently flattened and perfect to fabricate high performance devices compared with that using ion implantation technology[11] only.

4. Conclusion

Employing an LT-Si layer, high-quality biaxial strained-Si material is successfully grown on thin relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate with an RMS of 1.02 nm, defect density of 10^6 cm^{-2} and strain relaxation degree of 85.09%. The misfit dislocations, formed in the LT-Si layer, release the strain and threading dislocation is effectively suppressed in the pseudomorphic $Si_{0.8}Ge_{0.2}$ layer. Furthermore, the strain relaxation degree varies from 85.09% to 96.41% by the point defects introduced into the LT-Si layer after P^+ implantation and RTA, while the surface roughness RMS only increases 7.8% and defect density varies little.

According to the experimental results we can conclude that the LT-Si layer can obtain a high-quality surface and ion implantation can offer a high strain relaxation degree. So, it is by the LT-Si layer method combined with ion implantation that a high-quality strained-Si material can be prepared with low defect density, low surface roughness, high degree of relaxation

and ultra-thin relaxed $Si_{1-x}Ge_x$ virtual substrate for high performance strained-Si device applications.

References

[1] Arghavani R, Derhacobian N, Banthia V, et al. Strain engineering to improve data retention time in nonvolatile memory. IEEE Trans Electron Devices, 2007, 54(2): 362

[2] Sun Y, Sun G, Parthasarathy S, et al. Physics of process induced uniaxially strained Si. Mater Sci Eng B, 2006, 135(3): 179

[3] Arghavani R, Yuan Z, Ingle N, et al. Stress management in sub-90-nm transistor architecture. IEEE Trans Electron Devices, 2004, 51(10): 1740

[4] Wu X, Baribeau J M. Composition and strain contrast of $Si_{1-x}Ge_x$ ($x = 0.20$) and $Si_{1-y}C_y$ ($y = 0.015$) epitaxial strained films on (100) Si in annular dark field images. J Appl Phys, 2009, 105(4): 435171

[5] Yeo Y. Enhancing CMOS transistor performance using lattice-mismatched materials in source/drain regions. Semicond Sci Technol, 2007, 22(1): 177

[6] Pidin S, Mori T, Inoue K, et al. A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films. International Electron Devices Meeting (IEDM), 2004: 213

[7] Chen C, Lee T L, Hou T H, et al. Stress memorization technique (SMT) by selectively strained-nitride capping for sub-65 nm high-performance strained-Si device application. Symposium on VLSI Technology, 2004: 56

[8] Welser J, Hoyt J L, Gibbons J F. NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures. International Electron Devices Meeting (IEDM), 1992: 1000

[9] Xie Y H, Fitzgerald E A, Silverman P J, et al. Fabrication of relaxed GeSi buffer layers on Si(100) with low threading dislocation density. Mater Sci Eng, 1992, 14(3): 332

[10] Liu J L, Moore C D, U'Ren G D, et al. A surfactant-mediated relaxed $Si_{0.5}Ge_{0.5}$ graded layer with a very low threading dislocation density and smooth surface. Appl Phys Lett, 1999, 75(11): 1586

[11] Buca D, Minamisawa R A, Trinkaus H, et al. Si^+ ion implantation for strain relaxation of pseudomorphic $Si_{1-x}Ge_x$/Si (100) heterostructures. J Appl Phys, 2009, 105(11): 114905

[12] Sawano K, Fukumoto A, Hoshi Y, et al. Fabrication of high quality SiGe relaxed thin layers by ion implantation technique with Ar, Si and Ge ions. Thin Solid Films, 2008, 517(1): 87

[13] Trinkaus H, Hollander B, Rongen S, et al. Strain relaxation mechanism for hydrogen-implanted $Si_{1-x}Ge_x$/Si(100) heterostructures. Appl Phys Lett, 2000, 76(24): 3552

[14] Kasper E, Lyutovich K, Bauer M, et al. New virtual substrate concept for vertical MOS transistors. Thin Solid Films, 1998, 336(1/2): 319

[15] Yang H, Fan Y. Effect of Si intermediate layer on high relaxed SiGe layer grown using low temperature Si buffer. Chinese Journal of Semiconductors, 2006, 27: 144

[16] Luo Y H, Wan J, Forrest R L, et al. High-quality strain-relaxed SiGe films grown with low temperature Si buffer. J Appl Phys, 2001, 89(12): 8279

[17] Chen H, Guo L W, Cui Q, et al. Low-temperature buffer layer for growth of a low-dislocation-density SiGe layer on Si by molecular-beam epitaxy. J Appl Phys, 1996, 79(2): 1167

[18] Linder K K, Zhang F C, Rieh J S, et al. Reduction of dislocation density in mismatched SiGe/Si using a low-temperature Si buffer layer. Appl Phys Lett, 1997, 70(24): 3224

[19] Jenkins K A, Rim K. Measurement of the effect of self-heating in strained-silicon MOSFETs. IEEE Electron Device Lett, 2002, 23(6): 360

[20] Peng C S, Chen H, Zhao Z Y, et al. Strain relaxation of GeSi alloy with low dislocation density grown on low-temperature Si buffers. J Cryst Growth, 1999, 201: 530

[21] Hartmann J M, Gallas B, Zhang J, et al. Gas-source molecular beam epitaxy of SiGe virtual substrates: II. strain relaxation and surface morphology. Semicond Sci Technol, 2000, 15(4): 370

[22] Vescan L, Wickenhauser S. Relaxation mechanism of low temperature SiGe/Si(001) buffer layers. Solid-State Electron, 2004, 48(8): 1279

[23] Christiansen S H, Mooney P M, Chu J O, et al. Strain relaxation mechanisms in He^+-implanted and annealed $Si_{1-x}Ge_x$ layers on Si(001) substrates. Materials Research Society Symposium, 2002: 27