A new integrated SOI power device based on self-isolation technology

Gao Huanmei(高唤梅)†, Luo Xiaorong(罗小蓉), Zhang Wei(张伟) , Deng Hao(邓浩), and Lei Tianfei(雷天飞)

(State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China)

Abstract: A new SOI LDMOS structure with buried n-islands (BNIs) on the top interface of the buried oxide (BOX) is presented in a p-SOI high voltage integrated circuits (p-SOI HVICs), which exhibits good self-isolation performance between the power device and low-voltage control circuits. Furthermore, both the donor ions of BNIs and holes collected between depleted n-islands not only enhance the electric field in BOX from 32 to 113 V/μm, but also modulate the lateral electric field distribution, resulting in an improvement of the breakdown voltage of the BNI SOI LDMOS. A 673 V BNI SOI LDMOS is experimentally obtained and presents an excellent self-isolation performance in a p-SOI HVIC.

Key words: buried n-islands; self-isolation; breakdown voltage; electric field; SOI
DOI: 10.1088/1674-4926/31/8/084012 **EEACC:** 2560B; 2560P

1. Introduction

Silicon-on-insulator (SOI) technology has been widely applied due to its high speed, low power loss, superior isolation and high reliability[1, 2]. There are two major challenges in high voltage integrated circuits (HVICs) on a thick SOI layer: (1) to isolate the high voltage devices from adjacent CMOS circuits effectively, and (2) to achieve a high BV. The deep trench isolation (DTI) in SOI technology has many advantages such as weak parasitic effects, small lateral dimensions and high circuit density[3]. However, for the HVIC on a thick SOI layer (e.g. > 20 μm), DTI by using trenches filled with dielectric or dielectric/poly material is complex and costly[4−6]. Consequently, research on other isolation technologies is of vital importance. One effective method for enhancing the vertical BV is to increase the electric field in BOX by introducing charges at the BOX's top interface. Many efforts have been devoted to this field: single-side or double-side trench structures, N buffer layer structure, semi-insulating polycrystalline silicon (SIPOS) and so on[7−12]. Partial silicon-on-insulator (PSOI) devices enhance BV through sharing the vertical voltage drop by the substrate[13, 14]. The combination of a linear variation in the lateral doping and an ultra-thin SOI film simultaneously improve the vertical and the lateral BVs in Refs. [15–17]. The high-voltage devices mentioned above are formed on the n-SOI layer, with dielectric isolation or junction isolation from the low-voltage circuits in HVICs.

To solve the two problems in thick-film SOI HVIC application, we present a novel buried n-island (BNI) SOI LDMOS structure in an HVIC fabricated in a p-SOI layer, with self-isolation instead of the DTI from the adjacent low-voltage control circuits. In the vertical direction, the ionized donors in the BNIs make the electric field in the BNI increase rather than monotonously decrease, leading to a great increase in the field of the BOX and as a result a high vertical BV; moreover, BNIs also modulate the lateral electric field distribution. Hence, both a high BV and an excellent isolation performance are realized in a self-isolation SOI HVIC. Meanwhile, the structure is easily fabricated by adding only one mask to the standard CMOS process.

2. Structure and mechanism

The cross section of a BNI SOI LDMOS is shown in Fig. 1, where t_S, t_i are the thickness of the top silicon layer and the BOX layer respectively. L_d is the length of the drift region, and L, D, Y_j are the length, distance and junction depth of BNI separately. The n-drift region for the BNI SOI LDMOS is formed by ion implantation on the p-SOI surface and a 3 V low voltage (LV) CMOS control circuit in the HVIC is fabricated on the adjacent p-SOI region. In the blocking state, the PN junction formed by p-SOI and the n-drift region of the BNI SOI LDMOS is reverse biased. Meanwhile, the discontinuous n-islands over BOX terminate the high potential inside the BNI

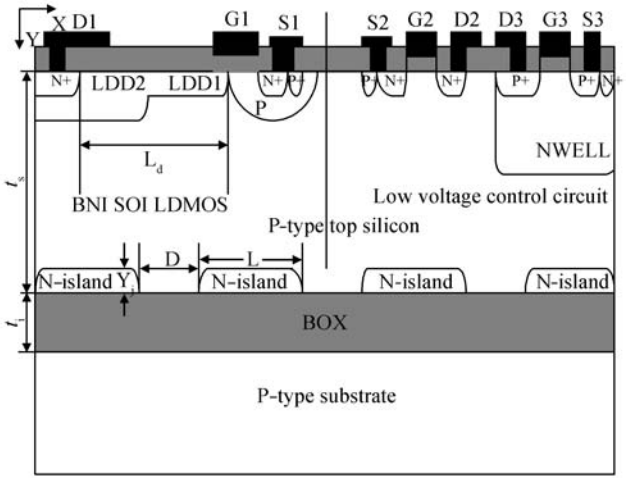


Fig. 1. Cross section of an SOI HVIC with a BNI SOI LDMOS.

† Corresponding author. Email: meifei0622@126.com
Received 20 November 2009, revised manuscript received 29 March 2010

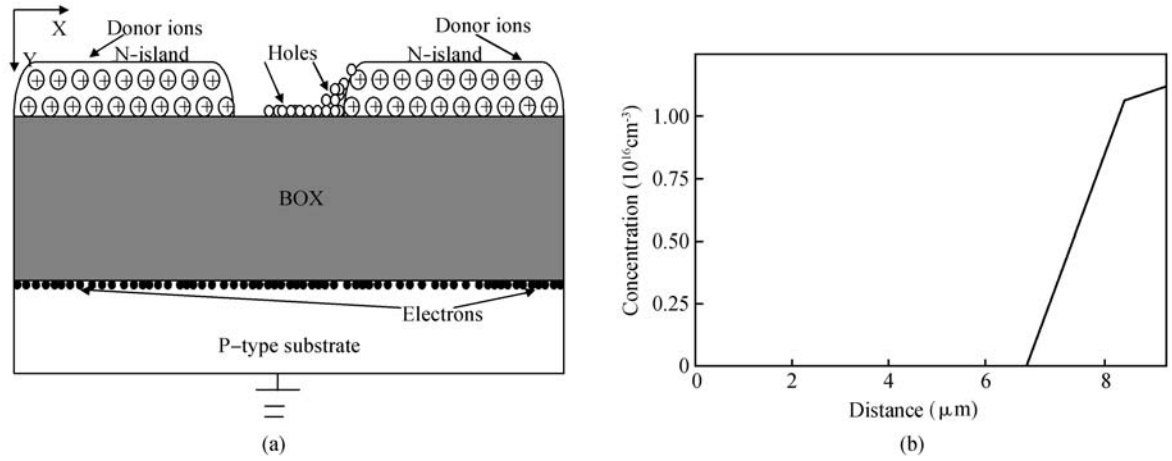


Fig. 2. (a) Two mechanisms of enhancement of the BOX electric field. (b) Hole distribution in a pair of neighboring n-islands.

SOI LDMOS and interrupt the path of the leakage current from the BNI SOI LDMOS to the low voltage region, resulting in an excellent self-isolation effect.

The electric field in the BOX layer is enhanced due to the following two mechanisms, as shown in Fig. 2(a). The first mechanism is that in the n-islands region, when the n-islands are fully depleted, the electric field in n-islands in the y-direction increases according to the following Poisson equation:

$$\frac{\partial E(y)}{\partial y} = \frac{qN_{\rm D}}{\varepsilon_{\rm s}}. \tag{1}$$

It can be seen that the slope of $E(y)$ in the y-direction is determined by the ionized donors with positive charges, and thus the electric field at the bottom interface of n-islands is increased. Consequently, the electric field in the BOX is greatly enhanced according to the Gauss law at the interface of n-islands/BOX:

$$\varepsilon_{\rm i}E_{\rm i} = \varepsilon_{\rm s}E_{\rm s}. \tag{2}$$

Thus BV is greatly improved by a high $E_{\rm i}$, where $E_{\rm s}$ and $E_{\rm i}$ denote the electric fields of SOI layer and BOX at their interface, respectively, and $\varepsilon_{\rm s}$ and $\varepsilon_{\rm i}$ are the permittivity of Si and BOX.

The second mechanism is that holes with a density $\sigma_{\rm s}$, accumulating on the bottom of p-SOI between two adjacent depleted n-islands, as shown in Figs. 2(a) and 2(b), enhance $E_{\rm i}$, based on Eq. (2):

$$\varepsilon_{\rm i}E_{\rm i} = \varepsilon_{\rm s}E_{\rm s} + q\sigma_{\rm s}. \tag{3}$$

The accumulating positive charges increase the electric field in BOX and thus $E_{\rm i}$ largely exceeds $3E_{\rm s}$.

Both mechanisms contribute to a high BV for BNI SOI LDMOS. In addition, two-region step doping in the drift region of the BNI SOI LDMOS is adopted to improve lateral BV through modulating the lateral electric field distribution in the drift region by a new field peak at the two doped region interfaces[18].

3. Results and analysis

In order to verify the breakdown mechanism and isolation performance of the BNI SOI LDMOS, the 2-D numerical simulator MEDICI is implemented. We also compare the results with that of an SOI LDMOS structure without n-islands. Moreover, the influences of device structure parameters on BV are studied by numerical simulation. Finally, the layout and the test result of a sample are presented.

3.1. Analysis on isolation performance

One of the innovations in the BNI SOI LDMOS structure is that we use p-SOI instead of a conventional n-SOI which can help to form self-isolation in the applied HVIC. Most of the high-voltage devices in HVIC are formed on an n-SOI layer, with dielectric-isolation or junction-isolation from the low-voltage circuits. However, most of these fabrication processes are complex and costly for high blocking voltage ICs[4−6], as illustrated in Fig. 3. The schematic cross-section of an HVIC with dielectric-isolation is shown in Fig. 3(a)[4]. The distinctive feature of the device structure is the double buried-oxide layer formed by SIMOX technology; obviously, there are several additional process steps needed for the dielectric-isolation: RIE, ion implantation, high temperature annealing, Si epitaxial growth, surface planarization and so on. Junction-isolation faces the same problem as shown in Fig. 3(b)[19]; the main steps for ensuring junction-isolation are summarized as follows: oxidation, well formation, buried layer diffusion, EPI growth, leveling, N-well formation, P^+ isolation and N^+ sinker diffusion.

Self-isolation technology is the most cost effective isolation technology which is easily applicable to HVICs by simply changing the material wafer to the desired type without process improvement. So, when remembering that the cost is of prime importance for HVICs, the study of self-isolation technology can be said to be one of the key theme for the development of HVICs.

The isolation effect for the BNI SOI LDMOS is compared with that of a buried n-layer (BNL) SOI LDMOS in Fig. 4. In the BNI SOI LDMOS, equi-potential contours are located within the power device, none of them extend into the low-voltage region, and thus the low-voltage region is shielded from the high electric field by the grounded source. However,

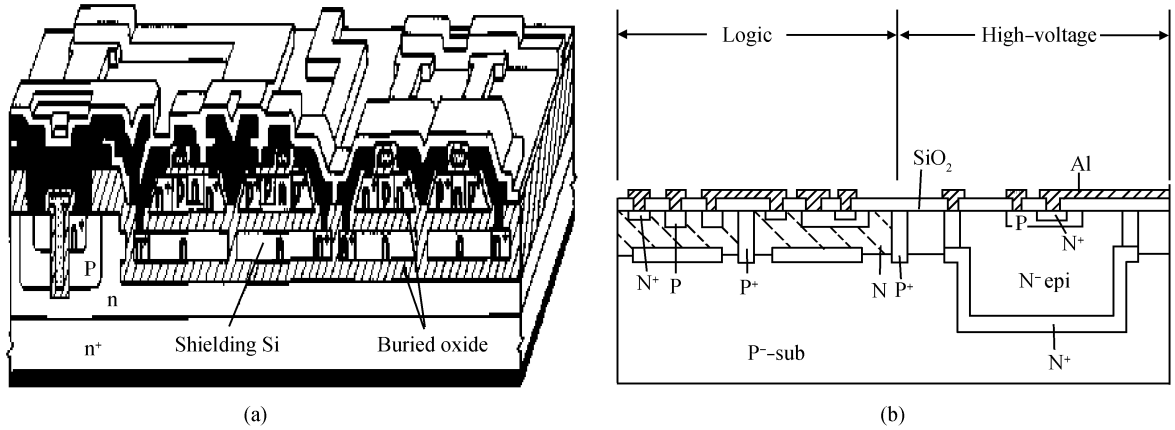


Fig. 3. Cross section of a HVIC with (a) dielectric-isolation or (b) junction-isolation.

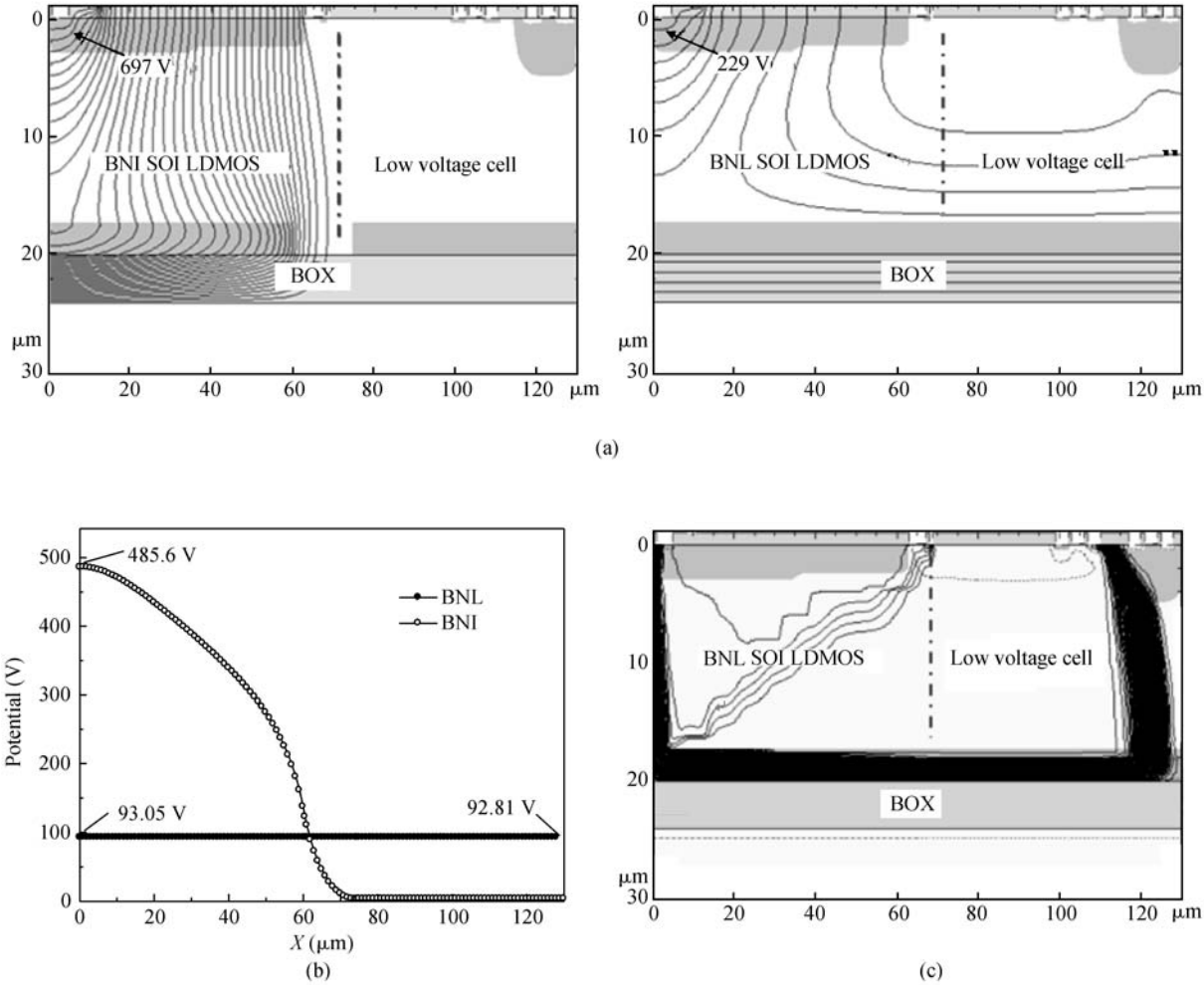


Fig. 4. (a) Comparison of isolation performance. (b) Potential distribution of BNI and BNL. (c) Current distribution of BNL SOI LDMOS.

in the BNL SOI LDMOS, equi-potential contours not only exist in the high-voltage device region, but also extend into the low-voltage circuit region; therefore, there is a large leakage current between the two parts, resulting in a low BV of 229 V. The same conclusion can be derived by analyzing the potential distributions for BNI and BNL, as shown in Fig. 4(b). In the BNI SOI LDMOS, the potential distribution of n-islands decreases gradually, and eventually reaches zero at the terminal of source and remains zero in the low-voltage circuit. Thus a good isolation performance has been attained between the high/low parts. But in the BNL SOI LDMOS, the potential distribution of the n-layer is almost even because the n-layer is an equi-potential body. Figure 4(c) shows the current flow lines, the equi-potential body of the n-layer offers a path to leakage

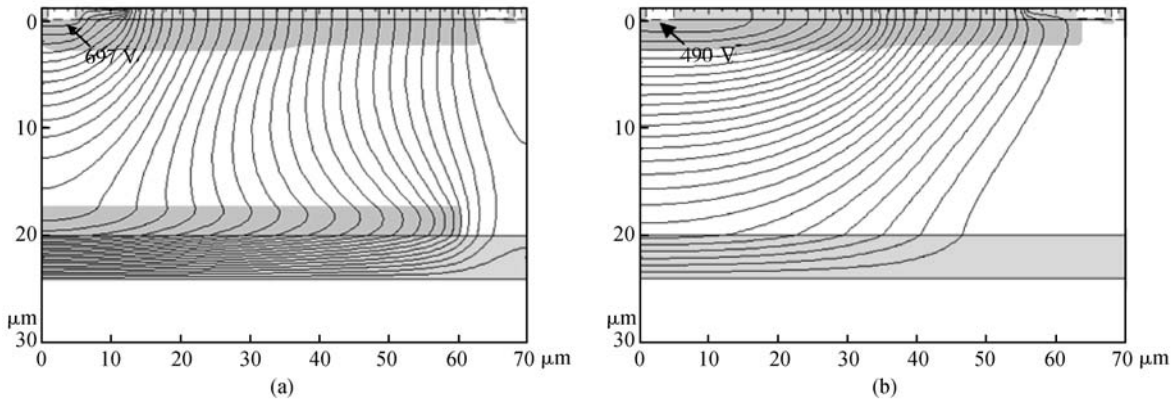


Fig. 5. Equi-potential contours of (a) BNI SOI LDMOS and (b) normal SOI LDMOS.

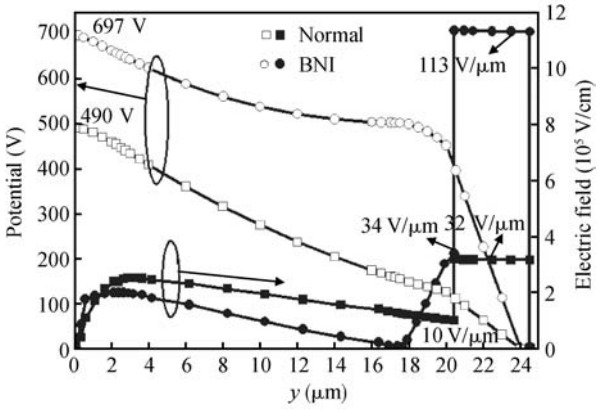


Fig. 6. Vertical electric field and potential distribution.

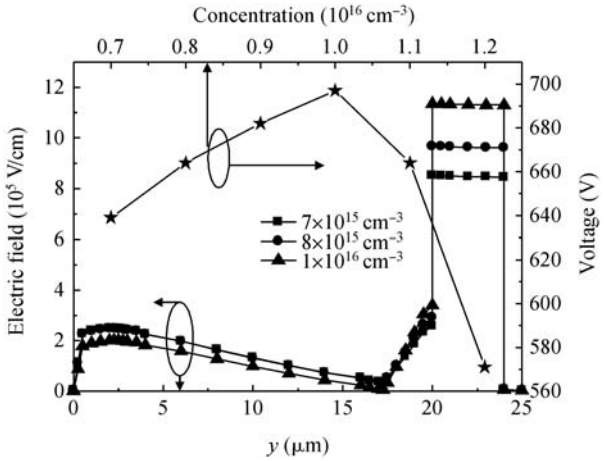


Fig. 7. Influence of concentration of n-islands on BV and vertical electric field.

current, resulting in a low BV and a large leakage current.

3.2. Analysis of breakdown characteristics

In order to make a fair baseline, all structure parameters of SOI LDMOS without n-islands are the same as the BNI SOI LDMOS. Figure 5 shows the potential contours for BNI SOI and the conventional p-SOI n-channel LDMOSFET. The n-islands helps to modulate the surface electric field distribution, thus the potential distribution becomes much more uniform, consequently the BV increases from 490 V for the normal SOI LDMOS to 697 V for the BNI SOI LDMOS.

Figure 6 shows the vertical electric field distribution and potential distribution for the two structures at breakdown. E_S increases from 10 V/μm for the conventional p-SOI LDMOS to 34 V/μm (at x = 2 μm) for the BNI SOI LDMOS, and thus the electric field in the BOX increases from 32 V/μm for the normal SOI LDMOS to 113 V/μm for the proposed structure, resulting in a larger BV of 697 V compared to 490 V for the normal structure.

Figure 7 shows the influence of doping concentration of the n-islands on BV and electric field in the y-direction. As is shown, the BV first increases and then drops with the increase of concentration of n-islands. This can be understood by analyzing the electric field in the y-direction. The slope of the electric field within the n-islands is low when doping concentration is relatively low, and so is the electric field in the BOX layer and BV, while BV and vertical electric field increase for a high concentration of n-islands. However, when the doping concentration exceeds a critical value, n-islands are not fully depleted, resulting in a decrease in BV.

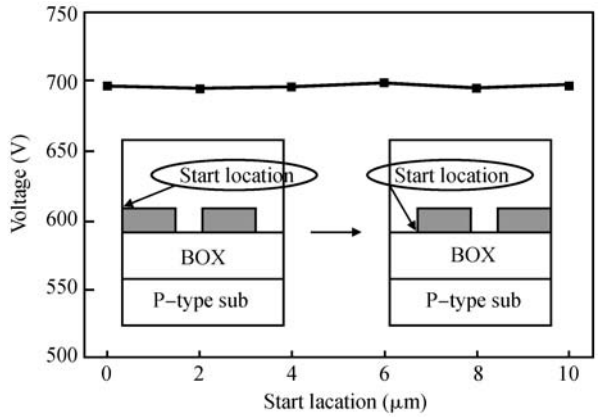
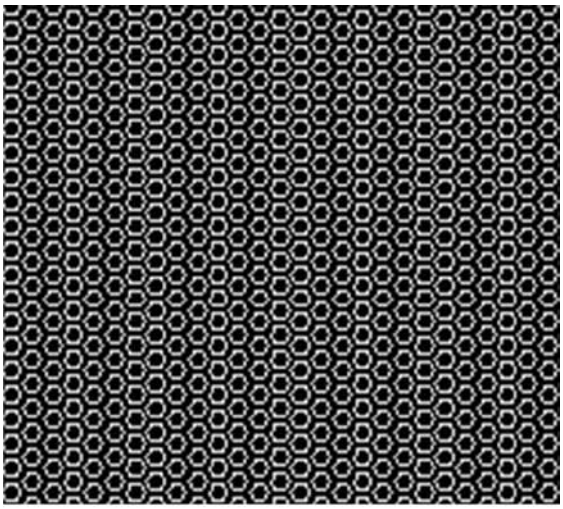
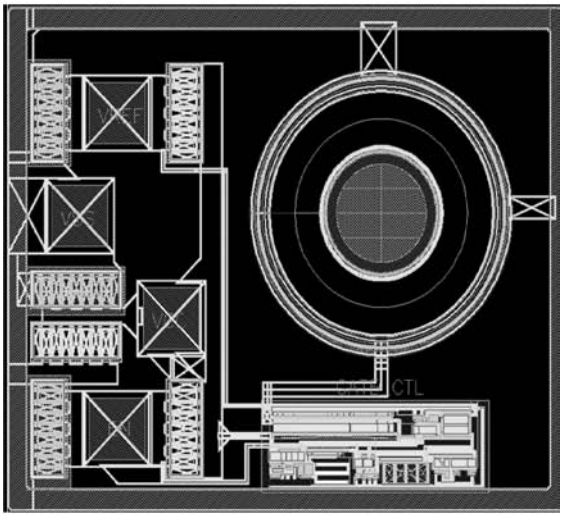


Fig. 8. Influence of start location on BV.

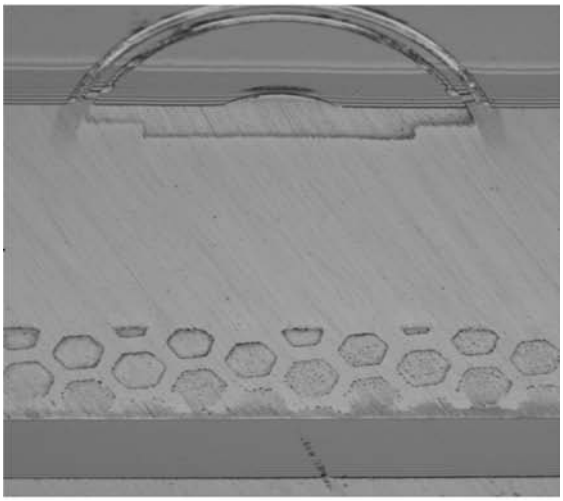
Figure 8 shows the relationship between BV and the start location of n-islands. As is shown, the BV of the BNI SOI LDMOS almost remains constant when the start location of



(a)



(b)



(c)

Fig. 9. (a) Layout of n-islands. (b) Layout of the whole system. (c) The section plane of a sample.

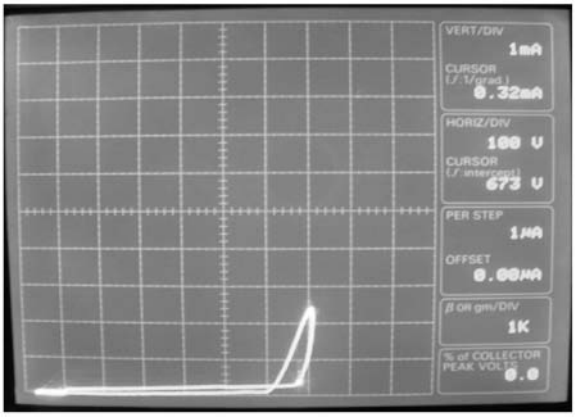


Fig. 10. Blocking characteristic.

n-islands changes, which supplies a great convenience to the adding process for BNI without taking account of its start location.

3.3. Experimental results

Since the start location of n-islands has no influence on the BV of the BNI SOI LDMOS, the pattern of n-islands is chosen to be regular hexagon arrays, as shown in Fig. 9(a). Figure 9(b) is the layout of the HVIC, in which the power device is designed to be circular in order to decrease the curvature effect, and the drain is placed right in the middle and the source in the outer region. This consideration has two advantages: one is to separate the leakage current of the high-voltage power device from the low-voltage control part; the other is to let the high electric field from the power device terminate fully in the source region, ensuring good isolation. Figure 9(c) shows a tilted-section view of an experimental sample. The snapshot was taken at a triangle of 2°52′ from the sample. A 673 V BNI SOI LDMOS is fabricated in Fig. 10, which is in accordance with simulation results. It is measured by SONY TEKTRONIX 371A (a piece of high-voltage measurement equipment).

4. Conclusion

This paper presents a novel high-voltage BNI SOI LDMOS for SOI HVIC application, in which isolation between the power device and the low-voltage control cell is realized by using self-isolation technology. Meanwhile, the positive charges in the n-islands modulate electrical field distribution in the drift region and increase the electric field in BOX, resulting in a high BV for the BNI SOI LDMOS. The fabrication is compatible with the standard CMOS process. This novel structure enlarges the application of thick film SOI devices, and provides a novel alternate structure in SOI HVICs.

References

[1] Udrea F, Garner D, Sheng K, et al. SOI power devices. J Electron Commun Eng, 2000, 12(1): 27

[2] Sorin C. Silicon on insulator technologies and devices: from present to future. Solid-State Electron, 2001, 45(8): 1403

[3] Elattari B, Bosch G V, Schoenmaker W, et al. Impact of charging on breakdown in deep trench isolation structures [parasitic MOSFET example]. European Solid-State Device Research, 2003: 513

[4] Ohno T, Matsumoto S, Izumi K. An intelligent power IC with double buried-oxide layers formed by SIMOX technology. IEEE Trans Electron Devices, 1993, 40(11): 2074
[5] Lerner R, Eckoldt U, Schottmann K, et al. Time dependent isolation capability of high voltage deep trench isolation. Proc ISPSD, 2008: 205
[6] Vogt F, Vogt H, Radecker M, et al. Smart power with 1200 V DMOS. Proc ISPSD, 1997: 317
[7] Luo X R, Li Z J, Zhang B, et al. A new high voltage (> 1200 V) MOSFET on partial SOI with the shielding charge trenches. IEEE Trans Electron Devices, 2008, 55(7): 1756
[8] Luo X R, Zhang B, Li Z J, et al. A novel 700-V SOI LDMOS with double-side trench. IEEE Electron Device Lett, 2007, 28(5): 422
[9] Yasuhara N, Nakagawa A, Furukawa K. SOI device structures implementing 650 V high voltage output devices on VLSIs. IEDM Tech Dig, 1991: 141
[10] Nakagawa A, Yasuhara N, Baba Y, et al. Breakdown voltage enhancement for devices on thin silicon layer/silicon dioxide film. IEEE Trans Electron Devices, 1991, 38(7): 1650
[11] Nakagawa A, Yamaguchi Y, Yasuhara N, et al. New high voltage SOI device structure eliminating substrate bias effects. IEDM Tech Dig, 1996: 477
[12] Luo X R, Lei T F, Wang Y G, et al. A high-voltage LDMOS compatible with high-voltage integrated circuits on p-type SOI layer. Electron Device Lett, 2009, 30(10): 1093
[13] Udrea F, Milne W, Popescu A. Lateral insulated gate bipolar transistor (LIGBT) structure based on partial isolation SO1 technology. Electron Lett, 1997, 33(10): 907
[14] Ratnam P. Novel silicon-on-insulator MOSFET for high voltage integrated circuit. Electron Lett, 1989, 25: 536
[15] Merchant S, Arnold E, Baumgart H, et al. Realization of high breakdown voltage (> 700 V) in thin SOI device. Proc ISPSD, 1991: 31
[16] Letavic T, Arnold E, Simpson M, et al. High performance 600 V smart power technology based on thin layer silicon-on-insulator. Proc ISPSD, 1997: 49
[17] Tadikonda R, Hardikar S, Narayanan E M S, et al. Realizing high breakdown voltages (> 600 V) in partial SOI technology. Solid State Electron, 2004, 48(9): 1655
[18] Sunkavalli R, Tamba A, Baliga B J, et al. Step drift doping profile for high voltage DI lateral power devices. Proceedings IEEE International SOI Conference, 1995: 139
[19] Kimura M, Okabe T, Shimizu I, et al. A flat-panel display control IC with 150-V drivers. Solid-State Circuits, 1986, 21(6): 971