An advanced monolithic digitalized random carrier frequency spread-spectrum clock generator for EMI suppression*

Guo Haiyan(郭海燕)[1,2,†], Chen Zao(陈早)[1], Zhang Bo(张波)[1], and Li Zhaoji(李肇基)[1]

(1 State Key Laboratory of Electronic Thin Films and Integrated devices, University of Electronic Science and Technology of China, Chengdu 610054, China)

(2 Information Engineering School, Southwest University of Science and Technology, Mianyang 621000, China)

Abstract: A novel monolithic digitalized random carrier frequency modulation spread-spectrum clock generator (RCF-SSCG) is proposed. In this design, the output frequency of the proposed RCF-SSCG changes with the intensity of the capacitive charge and discharge current. Its analytical model is induced and the effect of the modulation parameters on the spread spectrum is numerically simulated and discussed. Compared with other works, this design has the advantages of small size, low power consumption and good robustness. The circuit has been fabricated in a 0.5 μm CMOS process and applied to a class D amplifier in which the proposed RCF-SSCG occupies an area of 0.112 mm^2 and consumes 9 mW. The experimental results confirm the theoretical analyses.

Key words: Ransom carrier frequency modulation spread-spectrum clock generator; class D amplifier; electromagnetic interference

DOI: 10.1088/1674-4926/31/6/065010 **EEACC:** 1205; 1230B

1. Introduction

Electromagnetic interference emission is always of grave concern for power electronic circuit designers. The spread-spectrum clock technique has proven to be an efficient way to reduce peak electromagnetic interference (EMI)[1−12]. The harmonic power is spread out in this scheme so that peak EMI is significantly reduced. Compared with a periodic frequency modulation spread-spectrum clock generator (SSCG), a random carrier frequency modulation spread-spectrum clock generator (RCF-SSCG) has a better effect on the spread spectrum. A novel monolithic digitalized variable current RCF-SSCG is proposed in this paper.

In a low power consumption circuit, an amplifier without filter is widely adopted to save the cost and reduce the size, which results in increasingly outstanding EMI problems. An SSCG is usually used in these circuits even if in low power consumption to meet the related FCC standard. Conventional approaches to generate an SSCG are related to phase-locked loop (PLL) techniques[3−9]. Direct modulation of the voltage-controlled oscillator (VCO) in PLLs is used in these techniques[7−9]. But when the input frequency is low or the required bandwidth is small, large passive components in the loop filter will be required for stability consideration, and they will occupy a large silicon area which makes fully integrated PLLs difficult. In contrast, the proposed RCF-SSCG uses variable current direct modulation, which is based on the output frequency discretely changing along with the intensity of the capacitive charge/discharge current. A random signal generating circuit and a variable micro-current generating circuit are involved in the RCF-SSCG. In this design, the RCF-SSCG generates clocks of 300 kHz with maximal center spread ratios of 10%. The circuit has been fabricated in a 0.5 μm CMOS process and applied to a class D amplifier. The experimental results confirm the theoretical analyses.

2. Model and analyses of the proposed RCF-SSCG

2.1. Model of the proposed RCF-SSCG

As shown in Fig. 1, the RCF-SSCG circuit consists of a conventional oscillator circuit and a spread-spectrum circuit. VDDA and GNDA are power supply and ground respectively. Enable signals for two circuits are provided by EN. The random signal generating circuit generates random signals D_1−D_M to control whether the corresponding secondary current I_i is added into I_{main}, where I_{main} represents the capacitor charge/discharge current without frequency modulation and I_i is far less than I_{main}. In this design, when D_i is high, the switch is turned on to inject the corresponding secondary current I_i so that the variable micro-current generating circuit outputs variable current $\sum_{i=1}^{M} D_i I_i$ to OSC. The spread-spectrum circuit supplies variable charge current to the oscillator through ISP and supplies variable discharge current to the oscillator through ISN. Node voltages V_{ISP} and V_{ISN} from OSC supply bias voltages to the spread-spectrum circuit to generate the secondary micro-current I_i. V_{SAW} represents the voltage across the capacitor C. Let I_{sum} denote the sum current of I_{main} and $\sum_{i=1}^{M} D_i I_i$, which acts as the capacitive charge/discharge current. The relationship between the output frequency of the RCF-SSCG and the capacitive charge/discharge current can be expressed as $f = \rho(I_{sum})$ such that variable frequencies within a narrow range are obtained to reduce EMI noise by spreading the energy over a wider frequency range and an RCF-SSCG is

* Project supported by the National Natural Science Foundation of China (No. 60436030).

† Corresponding author. Email: guohy5@sina.com

Received 21 November 2009, revised manuscript received 23 February 2010

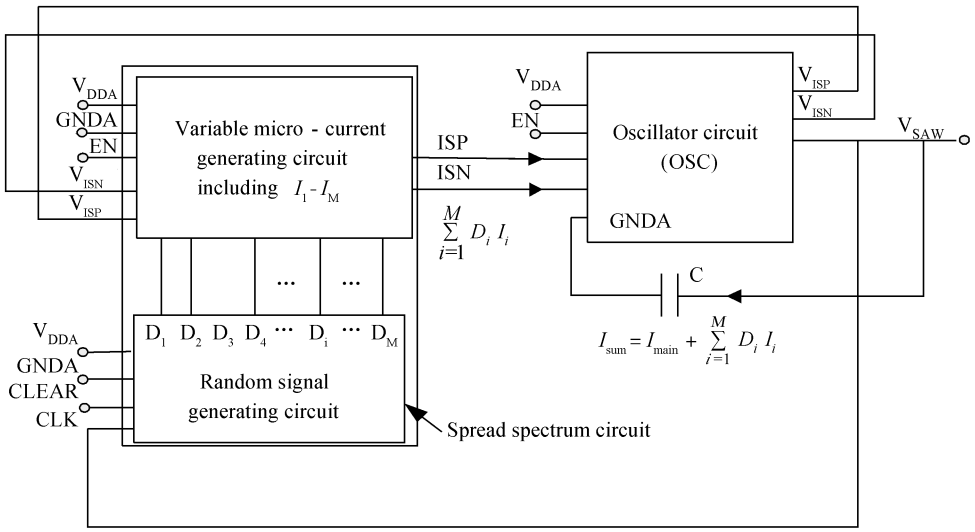

Fig. 1. Schematic diagram of the proposed RCF-SSCG.

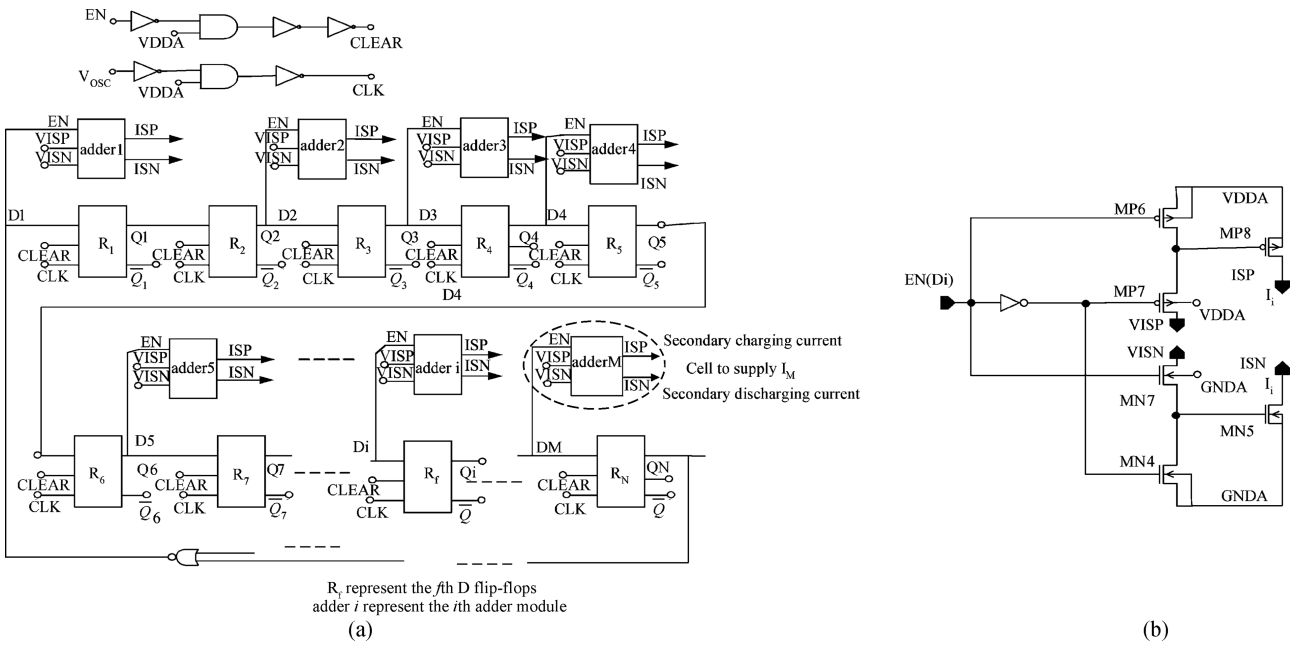

Fig. 2. Structure of the spread-spectrum circuit. (a) Block diagram of the spread-spectrum circuit. (b) Transistor-level realization of the adder module.

obtained.

2.2. Analyses of the proposed RCF-SSCG

In this circuit, the spread-spectrum circuit consists of a random signal generating circuit and a variable micro-current generating circuit which consists of M adder cells. The random signal generating circuit is realized by N serial D flip-flops whose terminals are connected as an m sequence, such that the output terminal of each D flip-flop is a random binary signal, which acts as an enable signal of the adder cell. The transistor-level realization of the adder cell is shown in Fig. 2(b). When enable signal D_i is high, MP7 and MN7 are turned on, so that the gate voltages of MP8 and MN5 are clamped to voltages $V_{\rm ISP}$ and $V_{\rm ISN}$ which are from the oscillator and are used to mirror a small proportion of the bias current I_i to nodes ISP and ISN of the oscillator. Each adder cell generates a micro-current I_i when enable signal D_i is high and M adder cells supply a variable current $\sum_{i=1}^{M} D_i I_i$ which is added into the primary current $I_{\rm main}$ to form $I_{\rm sum}$.

The transistor-level realization of the oscillator circuit is shown in Fig. 3. VDDA and GNDA are power supply and ground respectively. When the voltage of L_3 is low, MP5 is turned on while MN1 is turned off. In this case, capacity C is charged through MP5. Otherwise, capacity C is discharged through MN1.

In Fig. 3, the voltage across R_3 is clamped by OPA and equals the voltage across R_4; the current which flowing through R_4 is given as

$$I_4 = \frac{V_{\rm DDA} R_3}{(R_3 + R_2 + R_1) R_4}. \tag{1}$$

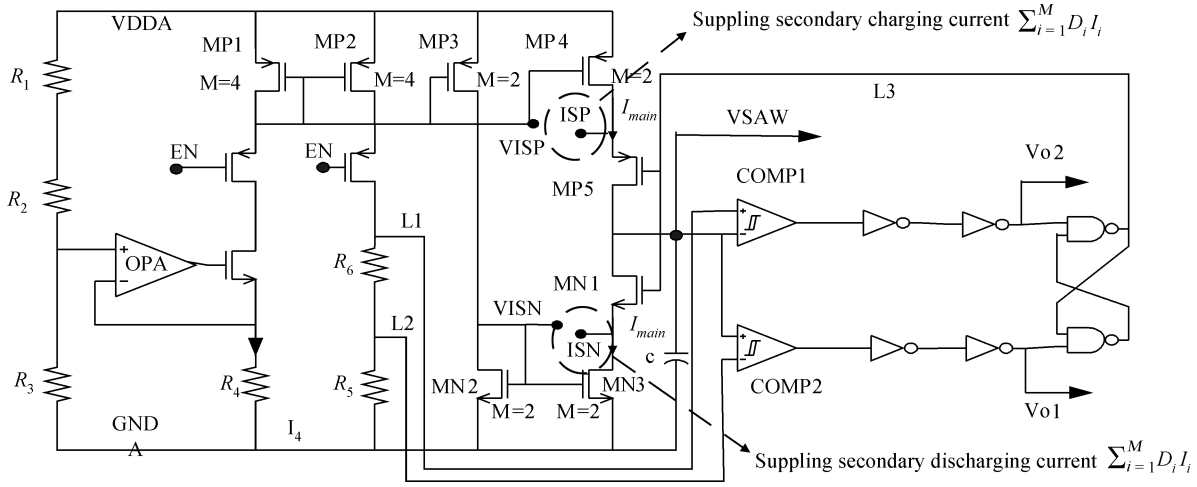

Fig. 3. Transistor-level realization of the oscillator circuit.

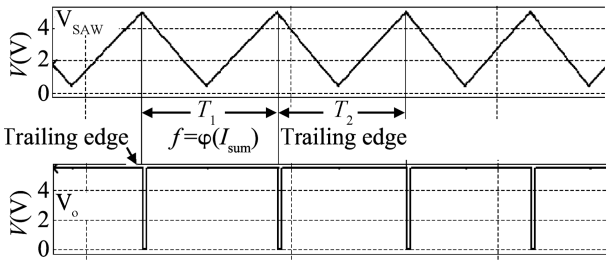

Fig. 4. Waveform of V_{SAW} and V_{o}.

From Fig. 3, I_{main} and I_{sum} are given as

$$I_{\mathrm{main}} = \frac{I_4}{2},$$

$$I_{\mathrm{sum}} = I_{\mathrm{main}} + \sum_{i=1}^{M} D_i I_i, \tag{2}$$

where M represents the number of secondary currents.

Because a D trigger is triggered at the trailing edge, triggers in the random signal generating circuit are triggered once in a period, where a period is denoted as the time quantum between two trailing edges as shown in Fig. 4. In a period, the charge/discharge currents are unchanged due to the status of D_1–D_{M} being constant. High gain and high speed comparators are chosen in this circuit to decrease the propagation delay from the logic path. If the transmission time consumed by digital circuits and comparators is ignored, the oscillator output frequency f is obtained as

$$f = \frac{I_{\mathrm{sum}}}{2C_{\mathrm{o}}(V_{\mathrm{L_1}} - V_{\mathrm{L_2}})}. \tag{3}$$

When D_1–D_{M} are all at a high level, $\sum_{i=1}^{M} D_i I_i$ reaches its peak and the oscillator output frequency reaches a maximum, and vice versa.

$$f_{\max} = \frac{I_{\mathrm{main}} + \sum_{i=1}^{M} I_i}{2C_{\mathrm{o}}(V_{\mathrm{L_1}} - V_{\mathrm{L_2}})}, \tag{4}$$

$$f_{\min} = \frac{I_{\mathrm{main}}}{2C_{\mathrm{o}}(V_{\mathrm{L_1}} - V_{\mathrm{L_2}})}. \tag{5}$$

So the carrier frequency f_{c} and the peak deviation of switching output frequency Δf_{c} are described by

$$f_{\mathrm{c}} = \frac{2I_{\mathrm{main}} + \sum_{i=1}^{M} I_i}{4C_{\mathrm{o}}(V_{\mathrm{L_1}} - V_{\mathrm{L_2}})}, \tag{6}$$

$$\Delta f_{\mathrm{c}} = \frac{\sum_{i=1}^{M} I_i}{4C_{\mathrm{o}}(V_{\mathrm{L_1}} - V_{\mathrm{L_2}})}. \tag{7}$$

As a result, the modulation index m_{f} can be expressed as

$$m_{\mathrm{f}} = \frac{\Delta f_{\mathrm{c}}}{f_{\mathrm{m}}} = \frac{(2^N - 1) \times \sum_{i=1}^{M} I_i}{2I_{\mathrm{main}} + \sum_{i=1}^{M} I_i} = \frac{2^N - 1}{2I_{\mathrm{main}} \Big/ \sum_{i=1}^{M} I_i + 1}. \tag{8}$$

f_{m} is the frequency of the modulating profile. In this circuit, f_{m} is given as

$$f_{\mathrm{m}} = \frac{f_{\mathrm{c}}}{2^N - 1}, \tag{9}$$

where N is the stage number of the serial D flip-flops.

According to basic modulation theory, the bigger m_{f} is, the better effect of the spread spectrum will be. Equation (8) indicates that larger N and smaller $I_{\mathrm{main}}/\sum_{i=1}^{M} I_i$ should be chosen in terms of EMI suppression. Because N is an exponential factor, it has a larger effect on EMI reduction. However, there is usually a limit to the switching frequency variation which may be accepted by a circuit, particularly on the selection of magnetic and capacitive components. So a balance point should be chosen in circuit design.

3. Simulation and measurement

In this design, the random signal generator consists of 17 stages of D triggers while the number of supplemental currents is 8. That is, $N = 17$, $M = 8$.

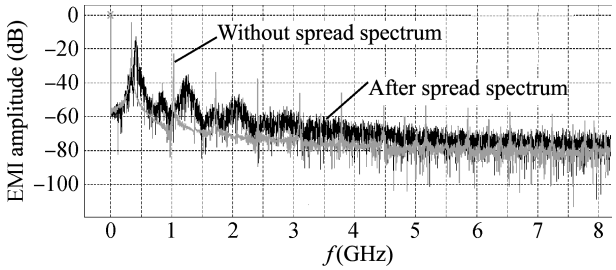

Fig. 5. Contrasted spectrum amplitudes with and without frequency jitter.

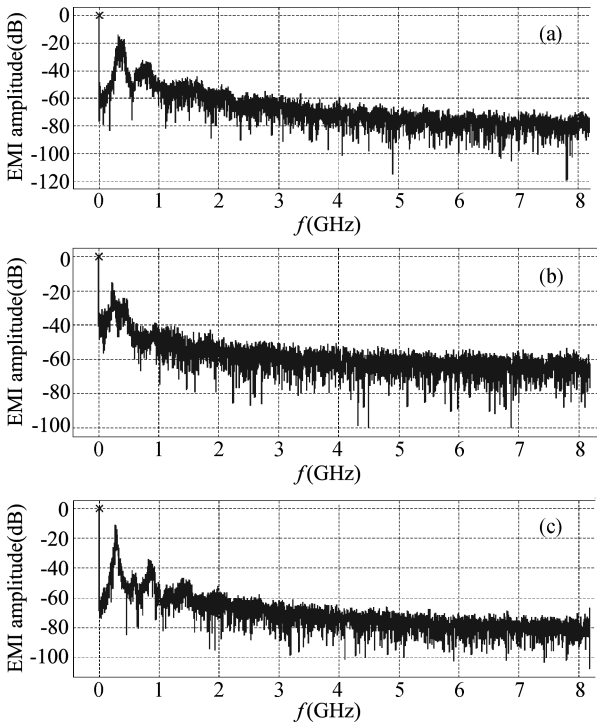

Fig. 6. Simulated spectra of 300 kHz output signal with spread-spectrum ratio 10% under different N. (a) N = 17. (b) N = 13. (c) N = 10. t = 25 °C, V_{DDA} = 3.6 V, M = 8.

The proposed RCF-SSCG can provide clock outputs of 300 kHz with center spread ratios of 10%. Spectrum amplitude comparisons of oscillator output waves with and without frequency jitter are simulated, which is shown in Fig. 5. It is shown that the EMI amplitude is reduced by about 12 dB after using the RCF-SSCG.

Modulation index m_f is a very important parameter to describe characteristics of the modulated signal in modulation theory. In this circuit, m_f is mainly related to the stage number of D flip-flops in the random signal generator. The effects of different N on EMI suppression are compared which is shown in Fig. 6. It indicates that when N = 17, EMI amplitude is close to that of N = 13, which is reduced by about 6 dB compared with N = 10. The relationship between peak power reduction (PPR) and the stage number N is somehow obvious: the greater N, the better PPR. However, it appears that when N reaches a certain level, PPR reaches a plateau. After that, greater N has little effect on the PPR. Meanwhile, adding the stage number of D flip-flops in the random signal generator will cause the circuit cost to increase. So a designer must trade off the relationship between the cost and EMI suppression to find a balance point.

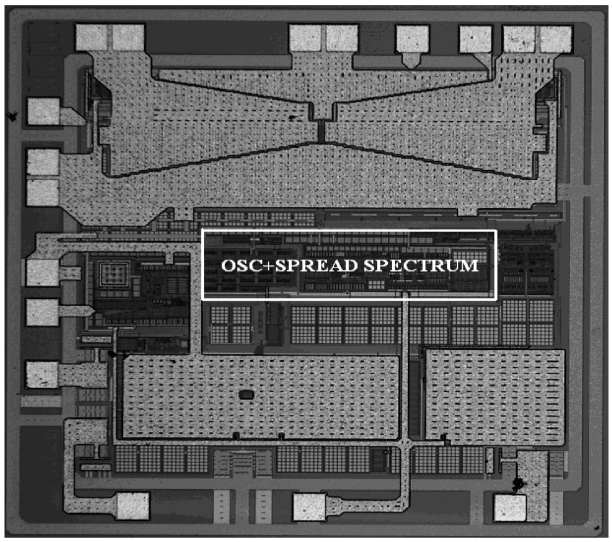

Fig. 7. Microphotograph of a class D amplifier where the RCF-SSCG is applied.

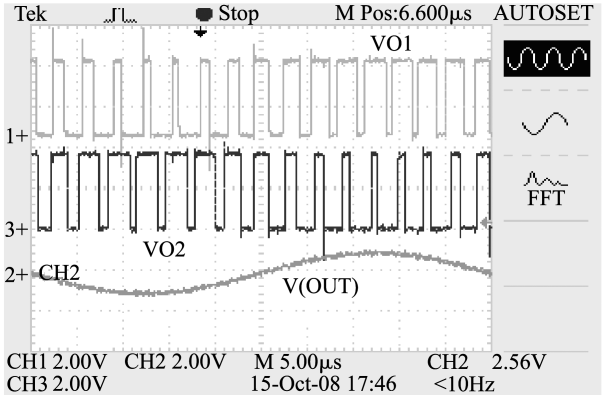

Fig. 8. Measured output wave of the oscillator and class D amplifier.

The proposed RCF-SSCG has been applied to a class D amplifier and fabricated in a 0.5 μm CMOS process. A microphotograph of the class D amplifier is shown in Fig. 7, in which the RCF-SSCG occupies an area of 0.112 mm^2. Figure 8 shows the output wave of the oscillator, which indicates the output frequency of the RCF-SSCG is variable and the RCF-SSCG works well. Figure 9 shows the radiated emissions of the class D amplifier with the RCF-SSCG from experiment, which indicates that the class D amplifier with the RCF-SSCG meets the FCC standard and this RCF-SSCG circuit works normally.

Table 1 summarizes the performance of the proposed RCF-SSCG and compares it with other works. The power consumption of the proposed RCF-SSCG is only 9 mW, much lower than that in the previous models in Refs. [7, 8, 10]. The total capacitor used here is only 4 pF while it is 352.47 nF in Ref. [7] and 78.959 nF in Ref. [8]. It occupies an area of 0.112 mm^2, which is more compact than that in other works. Hence, the advantage of the variable current controlled RCF-SSCG is clearly evident.

Table 1. Performance summary.

Parameter	Ref. [3]	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [8]	Ref. [9]	Ref. [10]	This work
Modulation method $\Sigma\Delta$		PI	PI	VCO	VCO	VCO	DCA	V-current
Modulation profile	triangle	triangle	Non-linear	triangle	triangle	triangle	N/A	RCF
EMI reduction (dB)	13.9	10.6	8.02	N/A	16	11.2	9	12*
Technology (μm)	0.2	0.6	0.15	0.35	0.35	0.3	0.35	0.5
Total capacitor (nF)	N/A	N/A	N/A	352.47	78.96	N/A	N/A	4×10^{-3}
Power (mW)	N/A	99#	N/A	300	150#	N/A	120	9*
Area (mm^2)	N/A	0.5625	N/A	2.012	0.77	2.18	0.306	0.112

Note: In this table, the data marked with * in this work represent simulated data, while the data marked with # are from either simulation or measurement, it not being clearly pointed out in the references. The unmarked data are measured data.

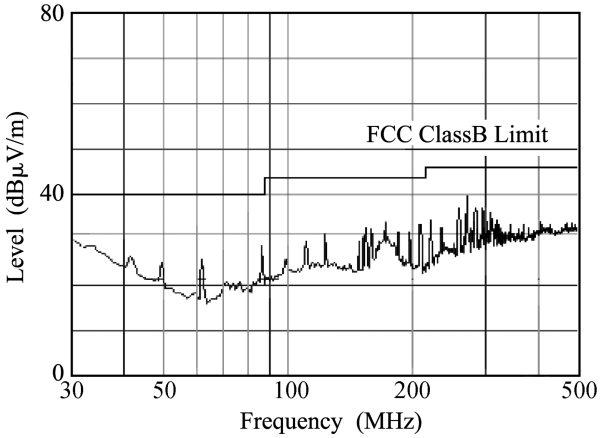

Fig. 9. Radiated emissions of the class D amplifier with the RCF-SSCG.

4. Conclusion

In this paper, a 300 kHz monolithic digitalized RCF-SSCG is presented. The clock uses no analog parts which makes it less sensitive to process variations and shows good robustness. An analytical model of the proposed RCF-SSCG is also introduced and discussed. This design has been fabricated using a 0.5 μm standard CMOS process and applied to a class D amplifier in which the circuit occupies an area of 0.112 mm^2 and consumes 9 mW. The proposed RCF-SSCG is advantageous for its good robustness, small size and low power consumption compared to PLL-based on-chip clocking methods. The measurement result shows that this architecture does achieve the spread-spectrum function as expected.

Acknowledgment

The authors would like to thank ADI for financial support.

References

[1] Gonzalez D, Balcells J, Santolaria A. Conducted EMI reduction in power converters by means of periodic switching frequency modulation. IEEE Trans Power Electron, 2007, 22: 2271

[2] Moon Y, Jeong D K, Kim G. Clock dithering for electromagnetic compliance using spread-spectrum phase modulation. Proc IEEE Int Solid-State Circuits Conf, 1999: 186

[3] Michel J Y, Neron C. A frequency modulated PLL for EMI reduction in embedded application. Proc IEEE Int ASIC/SOC Conf, 1999: 362

[4] Lee H R, Kim O, Ahn G, et al. A low-jitter 5000 ppm spread-spectrum clock generator for multi-channel SATA transceiver in 0.18-μm CMOS. Proc IEEE Int Solid-State Circuits Conf, 2005: 162

[5] Chen H W, Wu J C. A spread-spectrum clock generator for EMI reduction. IEICE Trans Electron, 2001, E84-C(12): 1959

[6] Yoshikawa T, Educhi T, Arima Y, et al. A spread-spectrum clock generator using digital tracking scheme. IEICE Trans Electron, 2005, E88-C(6): 1288

[7] Chang H H, Hua I H, Liu S I. A spread-spectrum clock generator with triangular modulation. IEEE J Solid-State Circuits, 2003, 38(4): 673

[8] Chen C C, Lee S C, Liu S I. A spread-spectrum clock generator using a capacitor multiplication technique. Proc Emerg Inf Technol Conf, 2005: 43

[9] Li H S, Cheng Y C, Puar D. Dual-loop spread-spectrum clock generator. Proc IEEE Int Solid-State Circuits Conf, 1999: 184

[10] Kim J, Kam D G, Kim J. Spread spectrum clock generator with delay cell array to reduce the EMI from a high-speed digital system. Proc International Symposium on Electromagnetic Compatibility, 2004, 3: 820

[11] Guo H Y, Li Z J, Zhang B. The effect of duty cycle on suppressing EMI level in random carrier frequency modulation of PWM. Proc ICACIA Conf, 2008: 164

[12] Mihali F, Kos D. Reduced conductive EMI in switched-mode DC–DC power converters without EMI filters: PWM versus randomized PWM. IEEE Trans Power Electron, 2006, 21: 1783