A 0.8 V low power low phase-noise PLL

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Abstract: A low power and low phase noise phase-locked loop (PLL) design for low voltage (0.8 V) applications is presented. The voltage controlled oscillator (VCO) operates from a 0.5 V voltage supply, while the other blocks operate from a 0.8 V supply. A differential NMOS-only topology is adopted for the oscillator, a modified precharge topology is applied in the phase-frequency detector (PFD), and a new feedback structure is utilized in the charge pump (CP) for ultra-low voltage applications. The divider adopts the extended true single phase clock DFF in order to operate in the high frequency region and save circuit area and power. In addition, several novel design techniques, such as removing the tail current source, are demonstrated to cut down the phase noise. Implemented in the SMIC 0.13 μm RF CMOS process and operated at 0.8 V supply voltage, the PLL measures a phase noise of –112.4 dBc/Hz at an offset frequency of 1 MHz from the carrier and a frequency range of 3.166–3.383 GHz. The improved PFD and the novel CP dissipate 0.39 mW power from a 0.8 V supply. The occupied chip area of the PFD and CP is 100 × 100 μm^2. The chip occupies 0.63 mm^2, and draws less than 6.54 mW from a 0.8 V supply.

Key words: phase-locked loop; voltage control oscillator; low voltage; low power; low phase noise
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1. Introduction

Integrated circuit technology has maintained an exponential scaling of the line-width of CMOS technologies deeper into nanoscale dimensions for the next two decades. This will increase the functionality density, the intrinsic speed of the devices and thus the signal processing capability of the circuits. However, in order to maintain the reliability, reduce the power density, and avoid breakdown as well as thermal problems, the maximum supply voltage has to be scaled down appropriately. All these features mentioned above have allowed the realization of systems with very high levels of integration on a monolithic silicon die at very low cost[1]. Compared with the reduction of the supply voltage, the transistor's threshold voltage is not reduced as aggressively. The low power supply voltages and the relatively large device threshold voltages are an obstacle for high performance analog circuit design. Recently, there have been several papers reporting that PLLs can operate at low-voltage supplies such as 0.65 V[1] or 1 V[2]. At supply voltages below 1 V, the design of analog circuits becomes very challenging since the traditional circuit techniques do not have sufficient voltage headroom. This is especially true for VCOs in wired and wireless communication systems for which high carrier power is necessary to lower the phase noise.

In this paper, a low power, low phase noise PLL that operates from an aggressively downscaled supply voltage implemented in the 0.13 μm RF CMOS process is presented. It demonstrates several design techniques overcoming the obstacles raised by voltage scaling and realizing low power dissipation. The detailed circuit design of the PLL is described, including the designs of the VCO, CP, PFD and divider.

2. Architecture of the PLL

A block diagram of the proposed PLL is depicted in Fig.1. The architecture of the system illustrated in Fig. 1 is simple and traditional. It comprises a PFD, CP, VCO, a dual-modulus prescaler, and an external third-order passive loop filter, which is designed for saving the core area. The detailed design techniques that are utilized for the low-voltage application of the PLL will be described in the following sections.

3. Circuit design

3.1. VCO design

In the PLL design, the most challenging task is to realize a high performance VCO with a reduced supply voltage and power consumption. While there are several VCO topologies, the complementary cross-coupled VCO topology is widely used due to its ability to suppress the $1/f$ noise. Unfortunately,

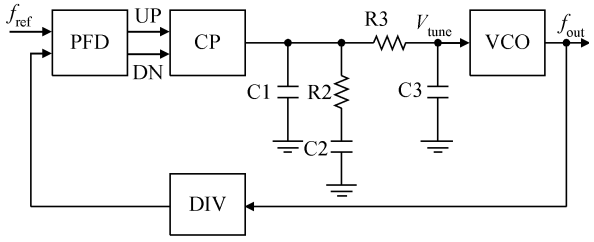

Fig. 1. Block diagram of the phase-locked loop.

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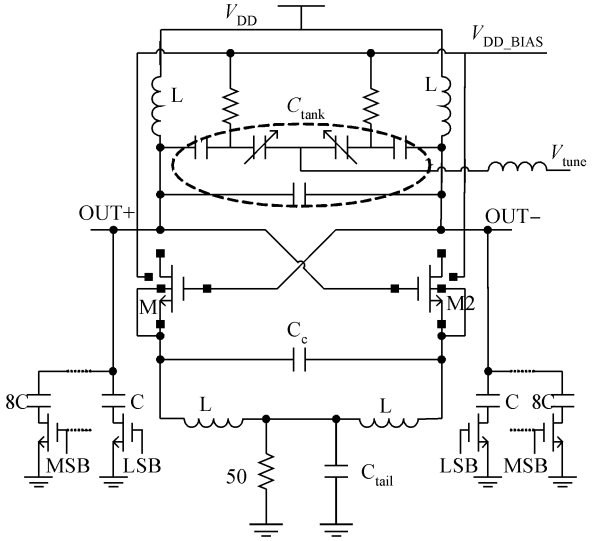

Fig. 2. Circuit diagram of the prototype VCO.

this topology is not suitable for a low supply voltage because of the voltage headroom cut down by the CMOS and the current source. So a transformer-feedback VCO topology is usually adopted for low voltage applications[2−4]. But the drawback is that the topology and calculation are enormously complicated as it introduces mutual inductors.

In this work, a differential NMOS-only topology is considered to realize the ultra-low voltage supply application for a VCO as shown in Fig. 2. As the NMOS-only VCO does not have PMOS cross-coupled pairs and current source, it reduces the voltage headroom, provides higher output swing for a low supply voltage and reduces the phase noise.

From the mechanistic physical model[5] mentioned, the noise factor F for the differential LC CMOS oscillator is given by:

$$F = 1 + \frac{4\gamma RI}{\pi V_0} + \gamma \frac{4}{9} g_{\text{mbias}} R, \tag{1}$$

where I is the bias current, γ is the channel noise coefficient of the FET, and g_{mbias} is the transconductance of the current source FET. Equation (1) indicates that the noise is derived from the tank resistance, the differential pair FETs, and the current source. In typical oscillators operating at high current levels, the current source contribution dominates other sources of phase noise[5]. Adopting the proposed VCO, the current source is omitted, so the third term is removed from Eq. (1). Unfortunately, removing the tail current source has its drawbacks. That is, the impedance at the common-mode point S is reduced and the loaded factor when the oscillation forces M1 and M2 into the triode region is loaded[6]. So two tail inductors are introduced in place of the tail current source raising the tail impedance at the oscillation frequency and its harmonics at the output node as well as lowering the voltage headroom.

The control voltage V_{tune} shown in Fig. 2 is connected to the output of the loop filter. If the output signal has high frequency harmonics, it will flow through the varactors to AC ground, degrading the Q factor and increasing the phase noise at the output. In order to suppress the high frequency signal but have no effect on DC voltage[7], an inductor and varactors in series

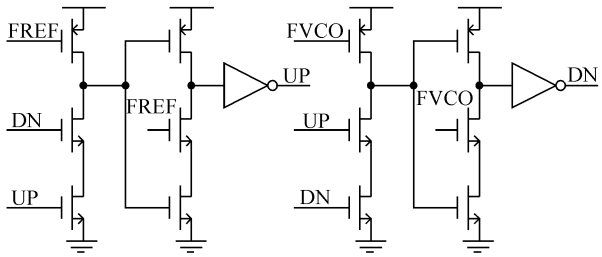

Fig. 3. Schematic of precharge type PFD.

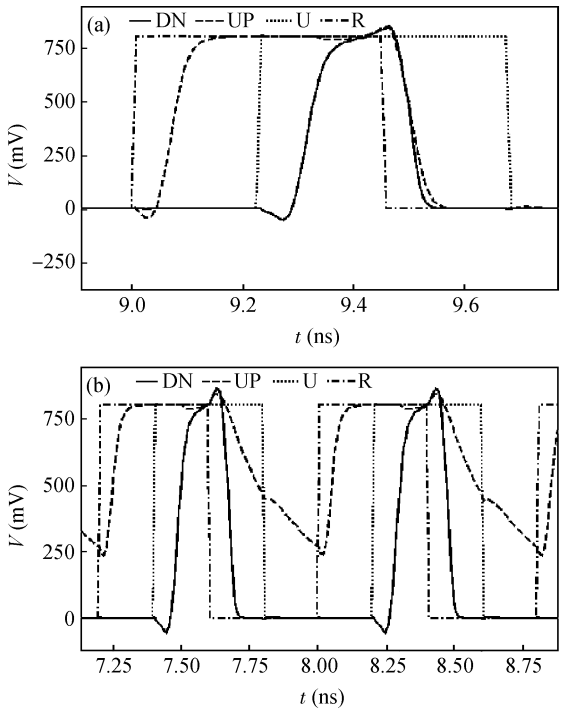

Fig. 4. Output of the PFD. (a) $f_{\text{in}} = 1.11$ GHz. (b) $f_{\text{in}} = 1.25$ GHz.

with passive metal–isolator–metal capacitors are used to make a clean control voltage.

Flicker noise in M1, M2 is modeled as a fluctuating offset voltage that unbalances the differential pair. After commutation, the fluctuation modulates the oscillation frequency and ultimately results in output phase noise. By eliminating the common mode capacitance, the flicker noise conversion is nulled[8]. The capacitor C_s is sized to appear as low impedance for the fundamental tone that circulates differentially in the cross coupled pair and very high impedance to flicker noise in the switching pair. With proper choice of the capacitance value, the fundamental oscillation is hardly disturbed and flicker noise is prevented from modulating the oscillation frequency.

3.2. PFD and CP

The PFD is implemented by modified precharge[9] topology since it can operate from a 0.8 V supply (Fig. 3). The modified precharge PFD (MPTPFD) has better speed performance than a conventional PFD. However, till now, all the papers concerning it said that it had a dead zone around zero phase error. Through careful analysis of the construct of the pt-PFD, it is found that the dead zone can be removed by suitably designing

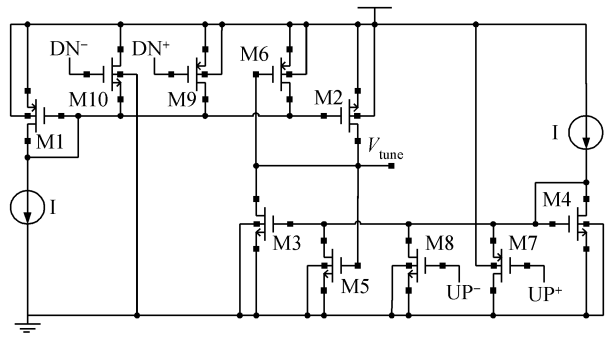

Fig. 5. Proposed charge pump topology.

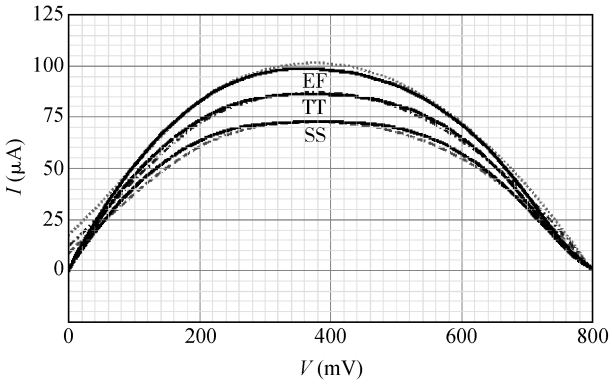

Fig. 6. Charge pump current matching characteristic under different process corners.

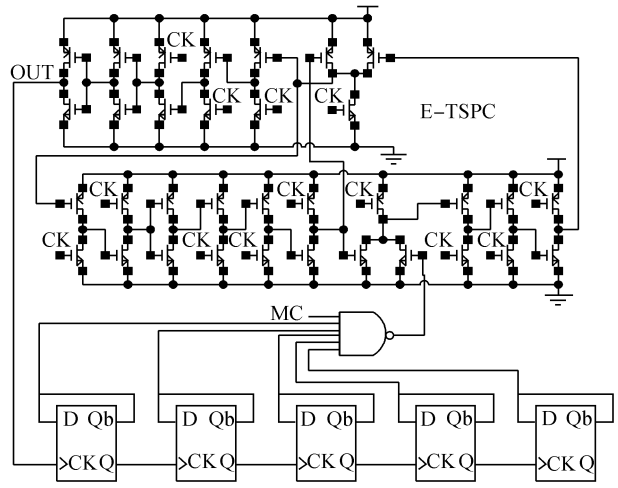

Fig. 7. Schematic of the divide-by 128/129 dual-modulus prescaler.

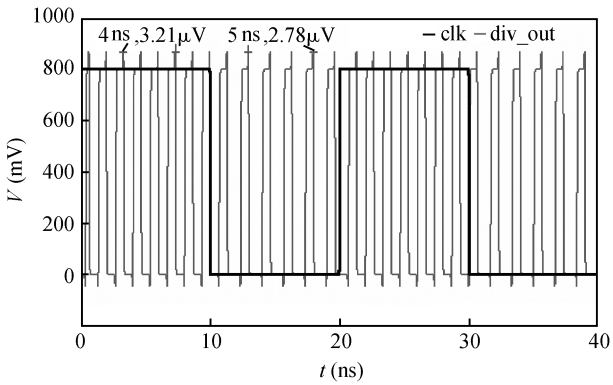

Fig. 8. Simulation results of the prescaler.

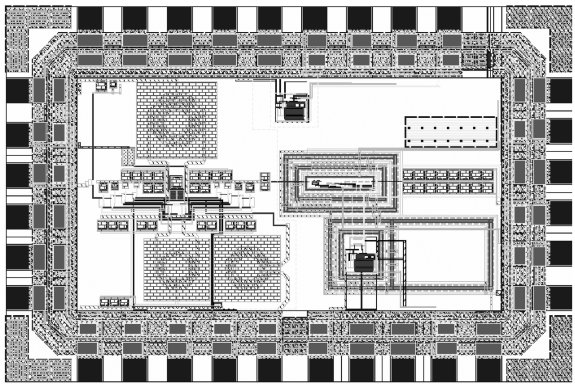

Fig. 9. Die micrograph of the proposed PLL.

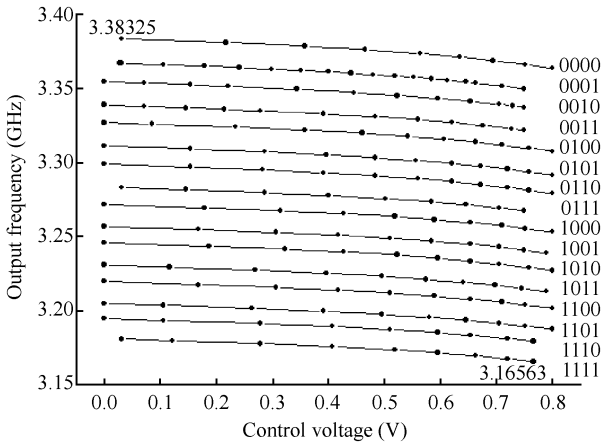

Fig. 10. Tuning characteristics of the proposed VCO.

the size of the transistors. The maximum operation frequency is defined as the shortest period with the correct UP and DN signals together with the inputs having the same frequency plus 90° phase difference[10]. Using this comparison criterion, the operation frequency for the proposed PFD is obtained greater than 1.11 GHz. The simulation result is shown in Fig. 4.

The proposed charge pump is shown in Fig. 5. In the 0.13 μm 1P8M CMOS process, the threshold voltage for NMOS and PMOS is about 0.3 V, which leads the output voltage range for a conventional charge pump to be reduced as low as 0.2 V. So with the reduced supply voltage, traditional stacking transistor stages should be prevented. Thus, the switches at the gate terminals of M2 and M3 are utilized to control the functionality of charging or discharging the loop filter. It is also noted that when the controlled voltage approaches the supply voltage or the ground potential, the mismatch between the up and down currents becomes large enough to greatly degrade the performance of the PLL. So the controlled voltage is connected to the gate terminals of M5 and M6 establishing a negative feedback to suppress the mismatch over a large voltage range[11]. Figure 6 shows the simulated systematic mismatch between the

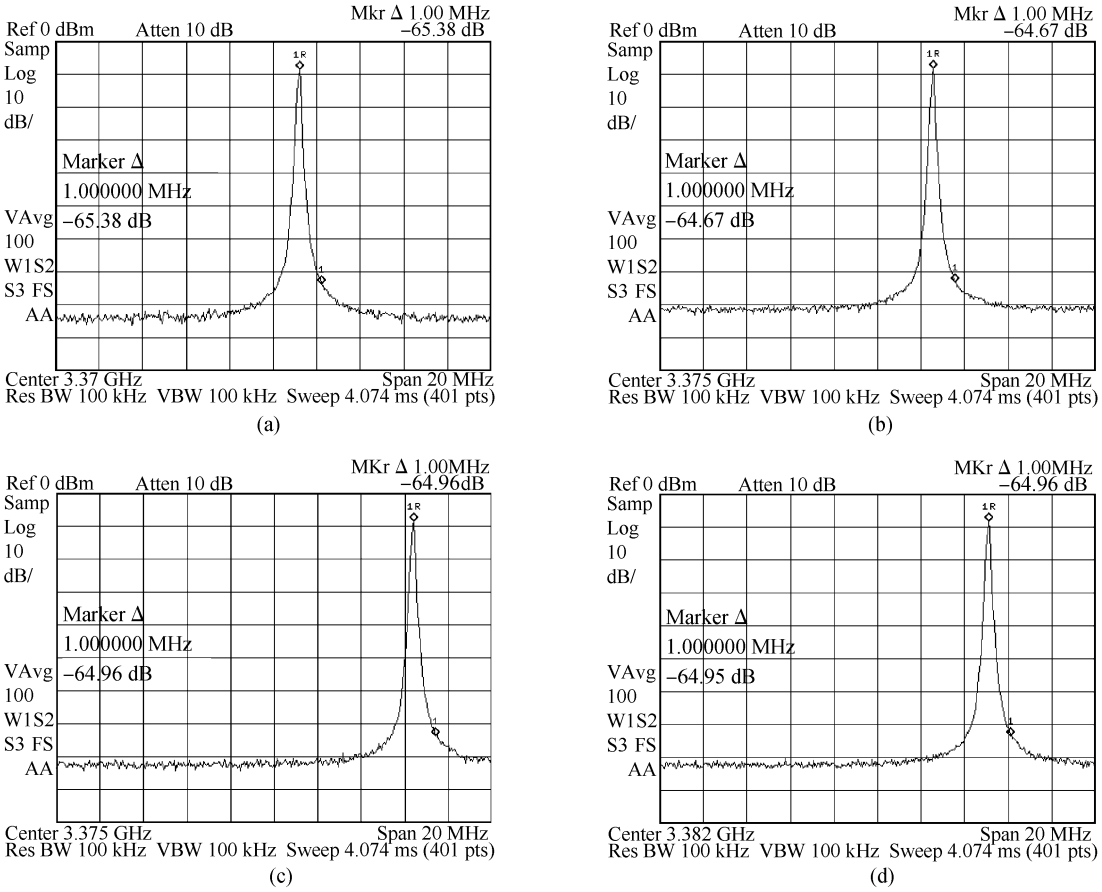

Fig. 11. Frequency spectrum of the output signal from the PLL. (a) $f_{\rm in} = 26.35$ MHz, $f_{\rm out} = 3.3728$ GHz. (b) $f_{\rm in} = 26.40$ MHz, $f_{\rm out} = 3.3793$ GHz. (c) $f_{\rm in} = 26.43$ MHz, $f_{\rm out} = 3.3830$ GHz. (d) $f_{\rm in} = 26.48$ MHz, $f_{\rm out} = 3.3895$ GHz.

up and down currents as a function of the output voltage for the proposed charge pump.

3.3. Divider design

A divide-by 128/129 dual-modulus prescaler circuitry using the traditional transmission gate flip-flop (TGFF) is shown in Fig. 7. Note that the speed of the divider is limited by a divide-by 4/5 prescaler circuit, so the extended true-single-phase-clock CMOS circuit technique (E-TSPC)[12] is introduced, which enhances the technique for high-speed operations. Based on 0.13 μm CMOS technology with a supply voltage of 0.8 V, the prescaler circuit in the gray area of Fig. 7 can run at 4 GHz with 0.71 mW power consumption. The asynchronous divide-by N, where N is 32 in this divide-by 128/129 prescaler, consists of one true-single-phase-clock (TSPC) FF[13]. It is simple and can work well at high frequencies.

4. Experimental results

The circuit was fabricated in a standard 0.13 μm CMOS process. The die photo is shown in Fig. 9, and its area is 1.2×1.1 mm^2, including the pads, while the loop filter is realized by off-chip components. Each building block is encircled by double guardrings to minimize substrate noise interference. Empty areas are filled with poly and metal layers to meet the requirement for the minimum density of these layers. Open-drain NMOS buffers are used for VCO output measurement[14].

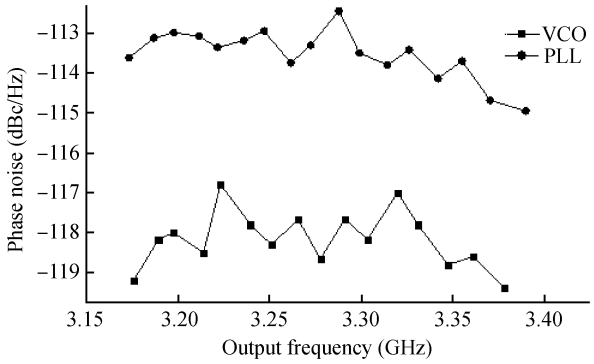

Fig. 12. Phase noise for the VCO and PLL at 1 MHz offset frequency.

By a combining discrete and continuous tuning[15], a family of overlapping tuning curves which guarantee continuous frequency coverage over the tuning range are measured and shown in Fig. 10. This VCO is tunable over 220 MHz with a sensitivity of about 30 MHz/V. In Fig. 11 the frequency spectrum of the output signal from the PLL with different reference frequencies is shown, while Figure 12 shows the phase noise of the VCO and PLL at 1 MHz offset along the whole frequency tuning range. It also shows that the phase noise displays little dependence on the frequency tuning. For example, in the whole frequency tuning range, the output phase noise reaches its worst value of −112.45 dBc/Hz at 1 MHz offset 3.2877 GHz,

Table 1. Comparison of PLL performance.

Reference	V_{DD}(V)	CMOS process (μm)	Frequency (GHz)	Phase noise @ 1 MHz (dBc/Hz)	Settling time (μs)	Power (mW)	Divider	FOM
Ref. [1]	0.65	0.09	2.4–2.6	–113	–	6	Integer-*N*	–173.5
Ref. [2]	1	0.18	4.112–4.352	–114	86	9.68	Integer-*N*	–176.6
Ref. [3]	0.8	0.18	1.06–1.4	–121	200	4.92	Fractional-*N*	–176.4
Ref. [16]	1.1	0.18	5.06–6.08	–114	40	31	Integer-*N*	–173.9
Ref. [17]	1.2	0.13	2.4–2.48	–125	70	15	Fractional-*N*	–180.8
This work	0.8	0.13	3.17–3.38	–112.4	37.2	6.542	Integer-*N*	–174.8

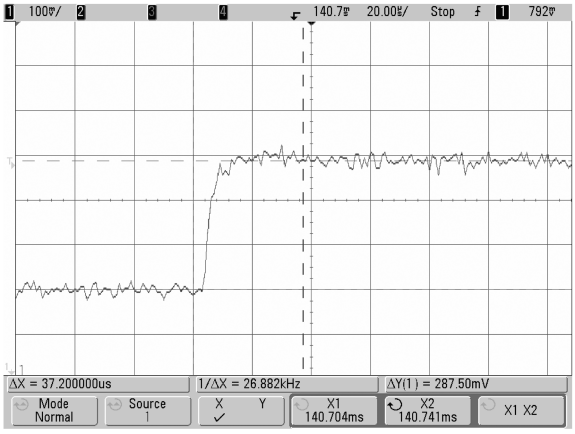

Fig. 13. Measured acquisition of the voltage controlled signal.

which results in the worst FOM of –174.630 dBc, while the output phase noise reaches the best value of –114.95 dBc/Hz at 1 MHz offset 3.3895GHz, and the optimum FOM is –177.396 dBc. Figure 13 shows the control voltage signal of the VCO, it also shows that the settling time of the proposed PLL is less than 50 μs. The total power consumption of this PLL chip was measured to be 6.542 mW, and the power consumption for the VCO is 1.3 mW. The performance of the proposed PLL is summarized in Table 1, compared with the performance of recently published PLLs with low supply voltages in the CMOS process. In order to compare the proposed PLL performance to other published work, it is useful to employ a FOM that captures three important performance parameters for oscillators: frequency, phase noise and power consumption.

5. Conclusions

In this paper, a low phase noise, low power PLL is presented. The circuit is implemented in a standard 0.13 μm CMOS process. With the improved PFD and novel CP structure, their dissipation is cut down to 0.39 mW from a 0.8 V supply. In addition, a differential NMOS-only topology that removes the tail current source is adopted for the VCO to ensure ultra-low voltage operation and reduce the phase noise. With a 0.8 V supply, the PLL measures a phase noise of –114.95 dBc/Hz at an offset of 1 MHz with a center frequency of 3.3895 GHz and a frequency tuning range from 3.17 to 3.38 GHz. The proposed PLL occupies a chip area of 1.32 mm^2 and dissipates only 6.54 mW.

Acknowledgement

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