A novel CMOS charge-pump circuit with current mode control 110 mA at 2.7 V for telecommunication systems

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Abstract: This paper presents a novel organization of switch capacitor charge pump circuits based on voltage doubler structures. Each voltage doubler takes a DC input and outputs a doubled DC voltage. By cascading voltage doublers the output voltage increases up to 2 times. A two-phase voltage doubler and a multiphase voltage doubler structures are discussed and design considerations are presented. A simulator working in the Q–V realm was used for simplified circuit level simulation. In order to evaluate the power delivered by a charge pump, a resistive load is attached to the output of the charge pump and an equivalent capacitance is evaluated. To avoid the short circuit during switching, a clock pair generator is used to achieve multi-phase non-overlapping clock pairs.

This paper also identifies optimum loading conditions for different configurations of the charge pumps. The proposed charge-pump circuit is designed and simulated by SPICE with TSMC 0.35-μm CMOS technology and operates with a 2.7 to 3.6 V supply voltage. It has an area of 0.4 mm^2; it was designed with a frequency regulation of 1 MHz and internal current mode to reduce power consumption.

Key words: switch capacitor charge pump; voltage doubler; power consumption
DOI: 10.1088/1674-4926/31/4/045001 **EEACC:** 2570

1. Introduction

A DC–DC charge pump circuit provides a DC voltage that is higher than the DC voltage of the power supply or provides a voltage of a reverse polarity. In many applications such as power IC and continuous time filter, 5 V flash memory programmer and EEPROM, voltages higher than the power supplies are frequently required. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load and do not involve amplifiers or transformers. For that reason, a charge pump is a device of choice in semiconductor technology where normal range of operating voltages is limited.

Existing charge pumps such as Dickson[1] and Makowski[3] charge pumps require a two-phase clock to control the charge transferring between capacitors. The voltage gain of a charge pump is a function of the number of stages in the pump. An n-stage Dickson pump has a voltage gain equaling to $n + 1$. In Ref. [3], Makowski established a theoretical limit on the voltage gain in a two-phase multiplier and related it to Fibonacci numbers.

An n-stage Makowski charge pump has a voltage gain equaling to the $2n$th Fibonacci number. Makowski's charge pumps have the highest voltage gains, which need the least number of capacitors among two-phase charge pumps. To improve the power efficiency[6], especially in the light load condition, a current mode control discussed in detail in section 3 is used to control the output current. The power efficiency[7], driving ability and clock generator regulation are discussed.

2. Theoretical consideration

A switched-capacitor organization of a two-phase DC–DC voltage doubler is shown in Fig. 1. It contains two clock-controlled switches and two capacitors. $V_{\rm IN}$ is the power supply; V_+ is the voltage output and $C_{\rm L}$ is the output capacitor. For a simple explanation of the voltage doubler operation, let us assume that the switches and the capacitors are all ideal. That is, we assume that there is no leakage current in the capacitors, and that the electric charge transferring is instantaneous. Let us assume that the voltage doubler starts in phase I (the two switches are connected to nodes I as shown in Fig. 1). The capacitor C_1 is initially charged by the power source to a voltage $V_{\rm IN}$, and C_2 is assumed to have no initial charge. In phase II, the lower voltage terminal C_{1-} of C_1 is connected to the power supply.

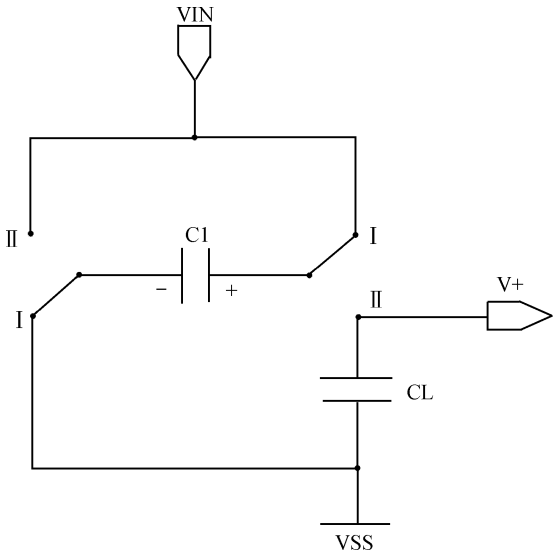

Fig. 1. Voltage doubler.

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Received 25 November 2009, revised manuscript received 29 December 2009

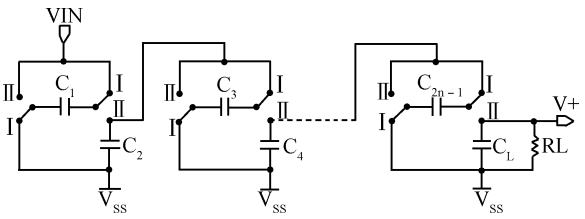

Fig. 2. Two-phase voltage doublers (simply cascaded).

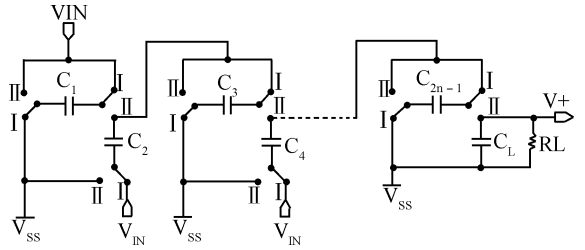

Fig. 3. Two-phase voltage doublers (Makowski charge pump).

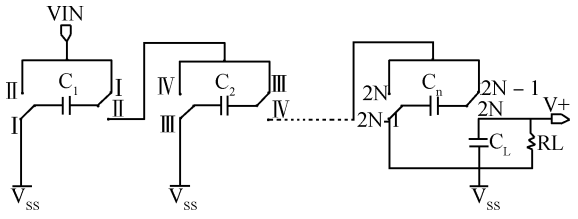

Fig. 4. Multi-phase voltage doublers (MPVD).

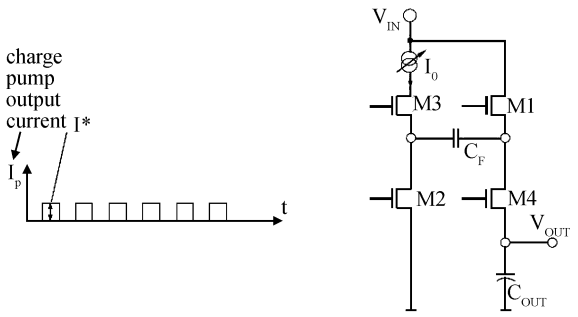

Fig. 5. Current mode voltage doubler.

If there were no C_2 connected to the higher voltage terminal C_{1+}, C_{1+} would have a voltage of value $2V_{\rm IN}$. As the C_{1+} is connected to C_2, the charge stored in C_1 is shared with C_2. The final output voltage V_+ is fixed by the $V_{\rm IN}$ plus a voltage due to the final charge in the capacitor C_1. This charge is less than the initial one in phase I. The charge redistribution allows V_+ to grow. Subsequently, the voltage doubler goes back to phase I, C_1 is recharged to hold a voltage $V_{\rm IN}$, and C_2 keeps the previous charge. Then the circuit is switched to phase II again. We obtain a final output voltage V_+ value greater than the previous one due to the charge stored in C_2. By repeating these operations many times, the output voltage V_+ keeps growing to the final voltage $2V_{\rm IN}$.

To achieve a voltage gain higher than 2, we can cascade the voltage doublers as shown in Fig. 2. The resistor RL represents the circuit load. The output voltage of previous voltage doubler is the power supply of the next voltage doubler. If there was no load (RL is infinite), the final output voltage is $2n$ times the voltage supply in ideal condition (no leakage current), where n is the number of stages of the charge pump. It needs $2n$ capacitors and $2n$ switches. Makowski proposed a two-phase charge pump in Ref. [3]; the basic diagram of this circuit is shown in Fig. 3. An n-stage Makowski charge pump has a voltage gain equal to the $2n$-th Fibonacci number that is higher than the voltage gain of simply cascaded voltage doublers, and needs $2n$ capacitors and $3n - 1$ switches. Starzyk[4] proposed a new multi-phase charge pump shown in Fig. 4. An n-stage Starzyk charge pump has a voltage gain 2n and it uses $n + 1$ capacitors and 2n switches. It requires n clock pairs to control these switches. Among these three charge pumps, MPVD have the highest voltage gain if the same number of capacitors is used. Hence a desired gain can be implemented with the least design area.

3. Current mode control for charge pumps

When we regulate the output voltage without observing the voltage drop on any of the switches by means of a two-limits or "skip" regulator we find the operating voltage levels on the "flying" capacitors being undefined. (For a "skip"-regulated voltage doubler this voltage can have any value between $V_{\rm OUT}/2 - V_{\rm IN}$ and $V_{\rm IN}$.) This comes from the fact that the ratio between the losses in charge- and discharge phase is undefined.

Therefore we have the big risk when we change the conversion ratio that the operating voltage level on the "flying" capacitor may change as well since the size, number, effective gate drive, etc. of the individual switches in charge and discharge states of the converter are different between the different conversion modes. The effect will be that additional charge is transferred to or from the input and output capacitors. This will cause an output voltage over- or undershoot at conversion ratio change. In extreme situations (large "flying" capacitors) a stable operation of the converter may be impossible. To minimize the glitch currents and keep the output voltage stable the operating voltage level on the "flying" capacitors is not allowed to change when switching from one conversion ratio to another.

Current-mode now is a regulation scheme for a charge pump in which one transistor in the output stage is operated as a controlled current source $I_{\rm O}$ (see Fig. 5).

$$I^* = \frac{2V_{\rm IN} - V_{\rm OUT}}{R^*_{{\rm M}i}} = f(V_{\rm IN}) \Rightarrow I^* = I_{\rm O}. \qquad (1)$$

The charge transferred per cycle is $I_{\rm CONT}\Delta t$ and therefore independent on $V_{\rm IN}$ and the sum of the resistances $\Sigma R_{{\rm M}i}$, where $R_{{\rm M}i}$ = on-resistance of switch Mi. With concentrating the conversion losses in the current regulated transistor (M3) we have the opportunity to stabilize the operating voltage level on the "flying" capacitor. When the current controlled transistor is in the discharge path (see circuit in Fig. 5) which means more losses in discharge phase than in charge phase, the voltage on $C_{\rm F}$ stabilizes to its maximum value ($V_{\rm IN}$). With the current controlled transistor being in the charge path, the voltage on $C_{\rm F}$ is minimized to a value of $V_{\rm OUT} - V_{\rm IN}$. Apart from the effect of stabilizing the operating voltage on the "flying" capacitors, current mode has additional advantages.

The output voltage ripple is minimized independent on the

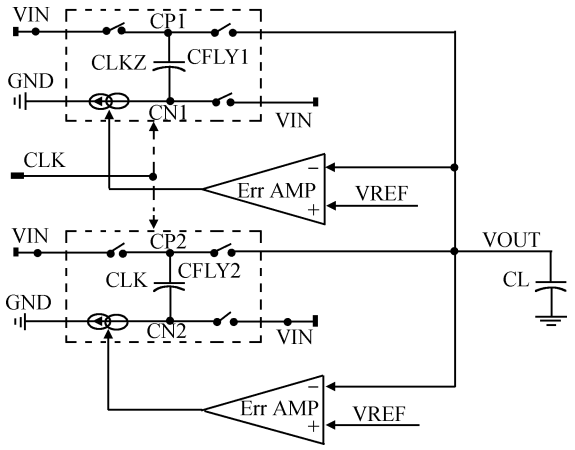

Fig. 6. 2-stage charging circuit.

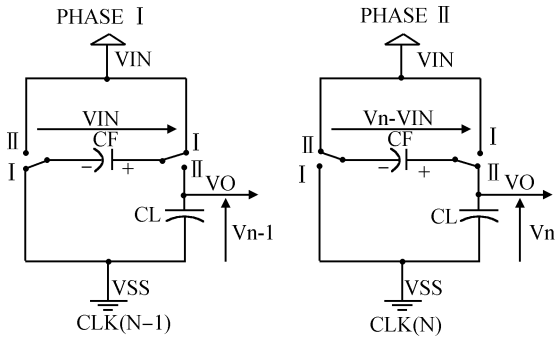

Fig. 7. Equivalent circuits of 2-stage voltage doubler.

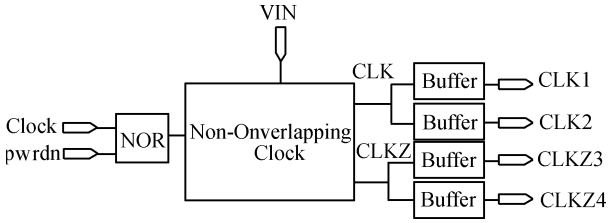

Fig. 8. Clock pairs generator.

supply voltage $V_{\rm IN}$ and the internal resistance $R_{{\rm M}i}$. When $I_{\rm O}$ is generated from a current mirror, the small signal gain of the controlled system "charge pump" is well defined; it is the ratio of the current mirror defining $I_{\rm O}$ divided by two (since the converter delivers energy only during the discharge phase). When the current source is placed in the discharge path of the charge pump, $C_{\rm F}$ always gets charged to the maximum possible voltage. With a "fully" charged $C_{\rm F}$, the charge pump achieves the best possible load transient response. As long as the current source $I_{\rm O}$ is kept out of saturation, the current waveform produced from the charge pump is independent on $C_{\rm F}$. The dominant pole of the system is defined by the load capacitor $C_{\rm LOAD}$ and the output impedance of the current source $I_{\rm O}$.

4. The proposed charge pump

The schematic diagram of the designed 2-stage charging circuit is shown in Fig. 6. The basic idea is to connect the two charge pump in parallel with the same output capacitor $C_{\rm L}$; four large MOS transistors are designed to control the connection and disconnection of the three capacitors C_1, C_2 and $C_{\rm L}$. The clock pairs CLK and CLKZ work at 1 MHz; they are used to switch these transistors on and off. The error amplifier is to vary the duty cycle of the switches reference to control the on-resistance which compares the output voltage with a of one of the switches this new architecture is working and deliver 110 mA at $V_{\rm IN}$ of 2.7 V.

Let us assume that for these large transistors, the turned-off resistors are infinite and the turned-on resistors are zero. For 2-stage MPVD, there are two phases; the equivalent circuit for each phase is shown in Fig. 7.

In an ideal condition, by assuming $C_1 = C_2 = C$ and the periods CLK and CLKZ equal to T, the average output voltage $V_{\rm out}$ is given by:

Assume that:

In phase I, the switches and capacitors are ideal, the voltage doubler starts in phase I, $C_{\rm F}$ is initially charged to $V_{\rm IN}$, and $C_{\rm L}$ is assumed to have no initial charge.

In phase II, $Q = CV$, the law of conservation of charge states that if two capacitors are connected together, the total charge on the combination is equal to the sum of the original charges on the capacitors.

$$C_{\rm F-} = V_{\rm IN},$$

$$C_{\rm F+} = 2V_{\rm IN}. \tag{2}$$

$C_{\rm F}$ is connected to $C_{\rm L}$. The charge stored in $C_{\rm F}$ is shared with $C_{\rm L}$, and $V_{\rm O}$ is fixed by $V_{\rm IN}$ plus a voltage due to the charge redistribution, after N period $V_{\rm O} = 2V_{\rm IN}$.

$$C_{\rm F}V_{\rm IN} + C_{\rm L}V_{N-1} = C_{\rm F}(V_N - V_{\rm IN}) + C_{\rm L}V_N$$

$$\Rightarrow V_N = \alpha V_{N-1} + \beta V_{\rm IN}, \tag{3}$$

where $\alpha = \dfrac{C_{\rm L}}{C_{\rm F} + C_{\rm L}}, \beta = \dfrac{2C_{\rm F}}{C_{\rm F} + C_{\rm L}}$.

By assuming the initial value of $V_{\rm O} = 0$, after N period:

$$V_N = \frac{1-\alpha^{N+1}}{1-\alpha}\beta V_{\rm IN} = 2\left(1-\alpha^{N+1}\right)V_{\rm IN}, \tag{4}$$

when $N \to \infty$, since $\alpha < 1 \Rightarrow V_N = 2V_{\rm IN}$.

5. Clock pairs generator

Figure 8 shows a block diagram of the clock pair generator. It contains a power down (pwrdn), a no overlapping clock pair converter, and buffer circuits. The pwrdn is used to control starting/stopping of the charging process.

As shown in Fig. 6, the CLK and CLKZ control the switches of the large transistors. Ideally, if the CLK is exactly the inverse of CLKZ, and there is no delay in switching the transistors, the M1 and M2 are not turned on at the same time. Since the W/L ratios of the transistors are very large, the transistors' rise and fall times are very large. Subsequently, it takes a long time to turn these large transistors on and off. To avoid the situation in which both M1 and M2 enter the transition state,

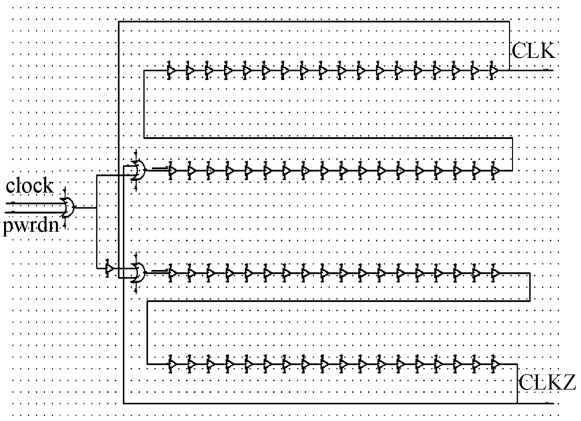

Fig. 9. Non-overlapping clock pairs converter.

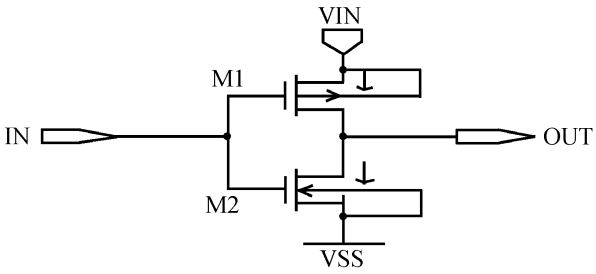

Fig. 10. Inverter CMOS.

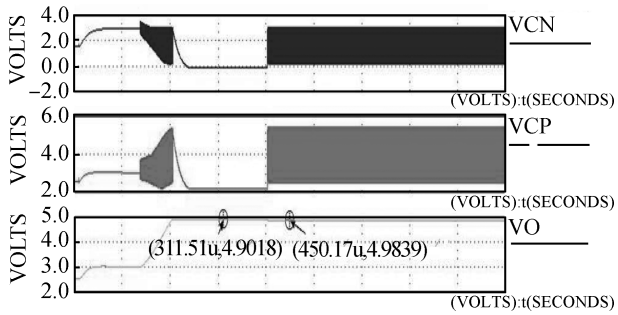

Fig. 11. Simulation result of clock generator and the output voltage.

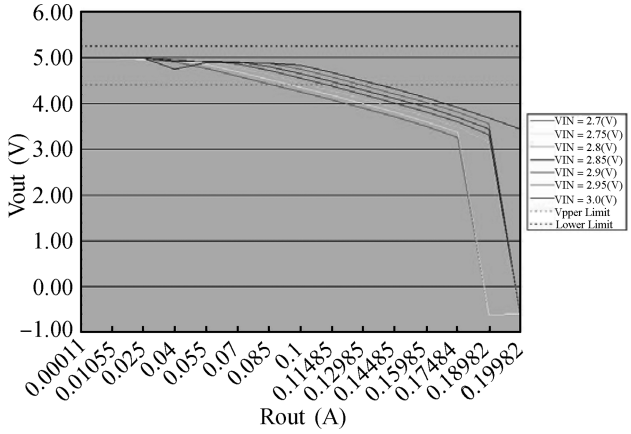

Fig. 12. Input voltage versus output.

the clock pair CLK and CLKZ must be designed to guarantee that before M1 is turned on, M2 must be turned off completely, and vice versa. To make sure that there is no short circuit current, and considering that a mismatch may occur during fabrication, the off-time (both CLK and CLKZ are turned off) should be several times larger than the rise time plus the fall time of the large transistors, the substrates of all PMOS transistors are connected to V_{out} to turn these MOS transistors on and off properly. The schematic of the non-overlapping clock generator is shown in Fig. 9. The generated clock pair CLK with their inverse clock pair CLKZ are non-overlapping.

The inverter shown in Fig. 10 is used to achieve the required delay. The rise time and the fall time of these 8 large transistors are very large. It will take a long time if the clock pair drives these transistors directly, and there is a risk of a short current during switching, even for 600 ns off time for the non-overlapping clock pair. To reduce the time spent in turning these transistors on and off, the driving buffers are designed.

6. Comparison with other regulated switched capacitor voltage converter

The most straightforward is to follow the switched capacitor Inverter/Doubler with a low dropout (LDO) linear regulator (architecture investigated).

The LDO provides the regulated output and also reduces the ripple of the switched capacitor converter.

This approach, however:

(1) Adds complexity.

(2) Reduces the available output voltage by the dropout voltage of the LDO.

(3) May require an external pin for the stability.

(4) Another approach to regulation is to vary the duty cycle of the switch control signal with the output of an error amplifier which compares the output voltage with a reference.

(5) This technique is similar to that used in inductor-based switching regulators and requires the addition of a PWM and appropriate control circuitry.

However, this approach is highly nonlinear and requires long time constants

The simplest and most effective method for achieving regulation in a switched capacitor voltage converter is:

(1) To use an error amplifier to control the on-resistance of one of the switches.

(2) Needs for stability reasons a fixed dominant pole 3× lower than the minimum external pole.

(3) For high load current the output resistor gets smaller and the pole moves to higher frequency.

$F_{\text{p}} \approx 1/R_{\text{o}}C_{\text{out}}$ is the non dominant pole at heavy and light loads.

(4) To use an error amplifier to control the current of one of the switches (architecture used).

(5) Replacement of the R_{on} control with current source control (high impedance) improves system stability.

7. Simulation results and conclusion

In order to evaluate the proposed charge pump and compare it to the conventional charge pump, circuit simulations are performed using 0.35 μm CMOS process parameters. All the simulations are carried out at 1 MHz. The values of pumping capacitors and output capacitors in all the charge pumps are

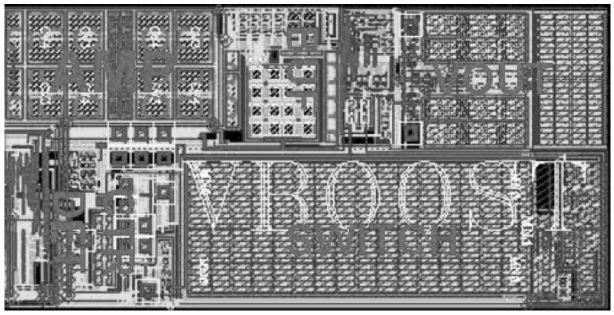

Fig. 13. Layout of the proposed charge pump.

CFLY1 = CFLY2 = C = 2.2 μF and C_{L} = 4.7 μF respectively. Figure 11 shows SPICE simulation results for the proposed charge pump. The output load current is 100 mA in all cases and the power efficiency is 79%.

As shown in Fig. 12, for the proposed charge pump with V_{in} of 2.7 to 3.6 V, we can see that the output voltages achieve 4.7 and 5.2 V respectively, and chip area could be reduced for the applications of high output voltage and low power supply by the proposed charge pump. Figure 13 shows the layout of the proposed charge pump this structure is realized and verified with caliber. In conclusion, our proposed circuit is still optimal.

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