A low power Gm–C filter with on-chip automatic tuning for a WLAN transceiver

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Abstract: A sixth-order Butterworth Gm–C low-pass filter (LPF) with a continuous tuning architecture has been implemented for a wireless LAN (WLAN) transceiver in 0.35 μm CMOS technology. An interior node scaling technique has been applied directly to the LPF to improve the dynamic range and the structure of the LPF has been optimized to reduce both the die size and the current consumption. Measurement results show that the filter has 77.5 dB dynamic range, 16.3 ns group delay variation, better than 3% cutoff frequency accuracy, and 0 dBm passband IIP3. The whole LPF with the tuning circuit dissipates only 1.42 mA (5 MHz cutoff frequency) or 2.81 mA (10 MHz cutoff frequency) from 2.85 V supply voltage, and only occupies 0.175 mm^2 die size.

Key words: Gm–C filter; interior node scaling; frequency automatic tuning
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1. Introduction

Increasing demand for higher capacity in the growing wireless LAN (WLAN) market and the different standards for 5-GHz WLANs—such as IEEE802.11a, HiperLAN/2, and HiSWANa—has led to more demand for wideband high-frequency operations. To support high user density, we will need multiple-channel-bandwidth systems (such as the latest Japanese standard with channel bandwidths of 5 MHz and 10 MHz) with widely tunable channel selection. A conventional channel-selection filter based on an array configuration, however, occupies a large chip area and cannot provide a continuous range of frequency tuning.

Besides widely tunable channel-selection, the filter for 4.9–5.95 GHz multi-standard WLAN systems with 5–20 MHz channel bandwidths has to meet other strict specifications from the system requirements: (a) accurate calibration system is needed to maintain precision cutoff frequency against process variation, temperature drift and aging; (b) the filter should have good linear performance and keep stable in high frequency; (c) temperature independent characteristic over wide dynamic range which is critical to achieve simple and accurate RSSI estimation; (d) small passband ripple to improve frequency dependent I/Q mismatch; (e) the filter should occupy a small chip area to be easily integrated.

This paper discusses the architecture design of the filter to find a suitable filter prototype, and discusses the circuit implementation of the filter and frequency automatic tuning circuit.

2. Basic design consideration

For the main filter, a sixth-order Butterworth leapfrog Gm–C filter topology is selected based on the following observations:

(1) Among the filter topologies, the prototype of the Butterworth filter has modest Q and requires low transconductor bandwidth which saves power consumption. Besides, the Butterworth filter has small group delay variation and can satisfy the band attention of the WLAN system specification. So the Butterworth topology is selected for our design.

(2) High order filters based on the integrators could be constructed using different methods. Different constructed methods would result in different dynamic ranges and accuracies. Among these methods, the leapfrog structure could achieve the lowest sensitivity and the best dynamic range[1], so it is adopted in this design.

(3) The Gm–C topology is usually preferred at high frequency for its lower power consumption relative to active-RC or MOSFET-C structures.

(4) Automatic tuning circuitry is necessary to maintain a precise filtering characteristic against process variations, temperature drift, aging, etc. Such a circuit is conveniently implemented by means of a phase-locked loop (PLL) using either a voltage-controlled filter (VCF) or a voltage-controlled oscillator (VCO). The first configuration has two main disadvantages. One is that it has stringent requirements on the phase comparator accuracy and speed performance, and the other is that it has additional tuning errors introduced by harmonic distortion[2]. So we choose a PLL with VCO to implement the frequency automatic tuning circuit.

3. Circuit design

3.1. Main filter

The structure and the component values of the leapfrog Gm–C filter are derived from the double terminated LC ladder filter prototype by signal flow graph transformation or with the help of filter synthesis software. The state equations of the LC ladder filter can be listed using the current through the inductors and the voltage at the grounded capacitance as the state variables. After some conversions, a group of new state equations, which use only voltage variables and have on differential operations, can be listed. When the Gm–C integrators are used to realize the integration operations of the new state equations, a leapfrog filter with the same transfer function can be obtained. The sixth-order Gm–C leapfrog filter topology is

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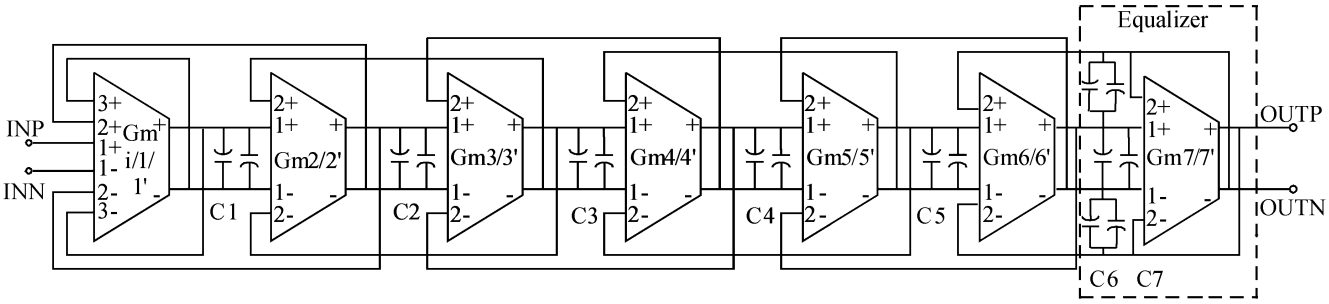

Fig. 1. Sixth order Gm–C leapfrog filter topology with an equalizer.

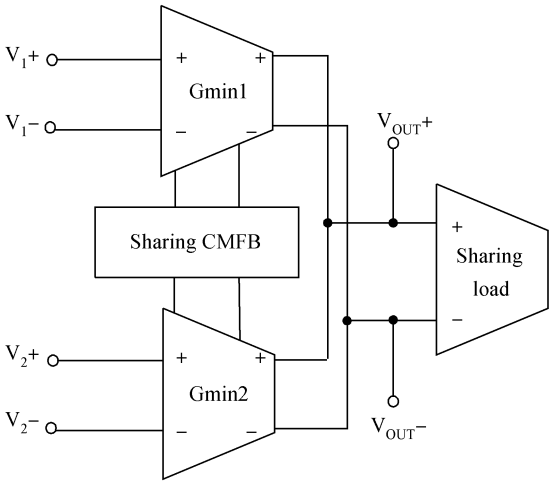

Fig. 2. Gm*i*/*i*' (i = 1, 2, 3, 4, 5, 6) with sharing load and CMFB.

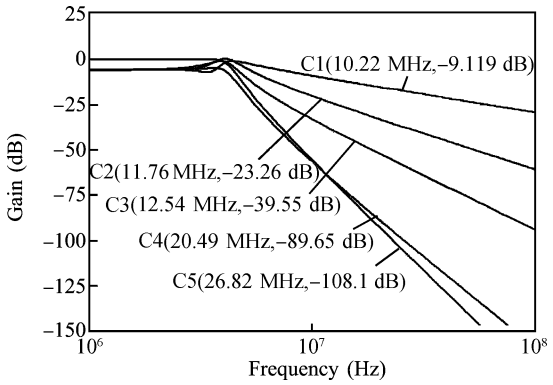

Fig. 3. Amplitude response of the LPF's interior nodes.

drawn in Fig. 1. The integrating capacitors are split as anti-parallel ones to keep the back-plate parasitic capacitances balanced to the n/p signal lines. The values of the actual capacitors and the parasitic capacitances are modified by deducing those of common mode feedback (CMFB) compensating capacitors C_C (which contributes a lot to reducing the die size and will be shown in Section 3.2) and the capacitances contributed by the linear transconductor circuit (Gm cell). In cases where the output currents of several Gm cells are combined, we need only one set of load and CMFB circuitry. In practice we used sharing loads and CMFB circuits, as shown in Fig. 2, to reduce the need for half as many load and CMFB circuits as the Gm cell input signal. So both the chip area and consumption current are reduced in this design.

An interior node scaling technique is applied to the prototype active ladder to achieve the maximum dynamic range (DR) with limited linear input range. When the topological structure of the filter was synthesized through function simulation, we found that although the passband gain of the filter was about unity the interior node voltage gains were greater than unity around the cutoff frequency. This meant that the signal amplitude at the interior nodes were greater than the amplitude of the input signal, which was to say that the linear input range of the filter was less than that of the transconductors, so part of the linear input range of the transconductors was not used. Thus, the interior node scaling technique is applied to make maximum use of the limited available voltage range in low-voltage operation.

The interior node scaling is carried out by varying the transconductance and capacitor values appropriately so that all the transconductors have unity voltage gain near the cutoff frequency[3]. We scaled the gains of the nodes C1, C2, C3 and C4. Specifically, the transconductance of Gm1, 1', 2, 2' and the node integral capacitance of C1 and C2 were doubled, and the transconductance of Gm3' and Gm4 was reduced by half. Figure 3 shows the simulation result of the gain of the LPF's interior nodes after being scaled. After we scaled the gains of the nodes C1, C2, C3 and C4, the passband gains were about –5.9 dB. Before being scaled, the gain of node Ci (i = 1, 2, 3, 4) around the cutoff frequency was greater than unity. After being scaled, each of them was reduced to be about unity relative to the input, which means that the voltage swing near cutoff frequency is reduced to be nearly equal to the input swing. So the linear input range of the LPF is increased around the cutoff frequency. Through this scaling the dynamic range is increased about 3 dB. In addition, the total signal-to-noise ratio (SNR) of the filter is improved by 3 dB because the total noise increased by 3 dB and the total voltage gain became doubled.

3.2. The linear transconductor circuit

The linear transconductor circuit (Gm cell) is the most critical building block of the whole filter and tuning system. The main characteristics of a Gm cell are: (1) enough linear input voltage range, (2) finite and wide bandwidth, (3) finite signal-to-noise ratio (SIN), and (4) finite output impedance. The SIN is a function of the Gm cell architecture among other factors. The output impedance can be increased using cascode structures at the expense of reduced output signal swing. Their programmability is caused by the transconductance bias depen-

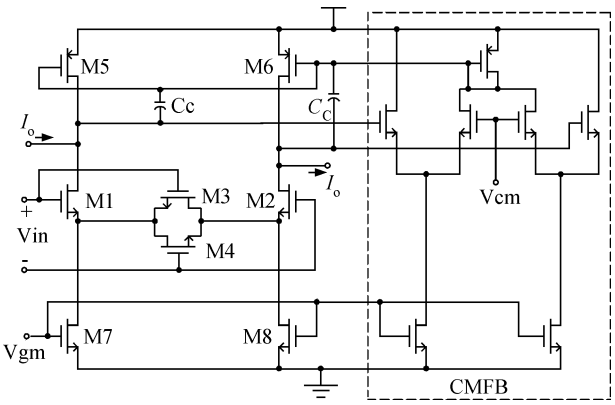

Fig. 4. One linearized active-source-degeneration Gmin cell with sharing capacitor C_C.

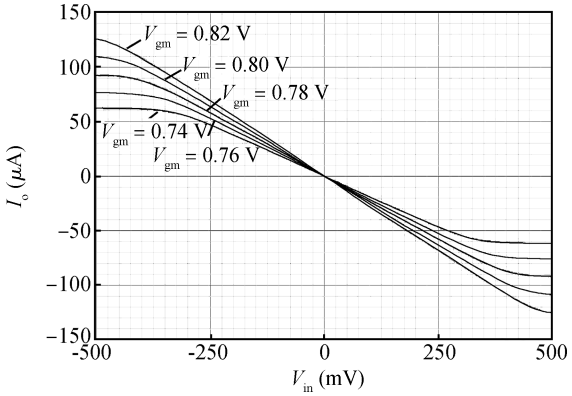

Fig. 5. Simulation results of I_o with different V_{gm}.

dence; this dependence allows several decades of tuning for transconductance with CMOS transistors operating in weak inversion and about two octaves for CMOS transistors operating in strong inversion.

Figure 4 shows the active-source-degeneration Gm cell used in this design. It uses source degeneration as the main linearization technique[2]. In this design, sharing capacitors are used to reduce the chip area. Capacitor C_C is used as the Miller compensating capacitor to ensure the stability of the CMFB circuit in every transconductor, while it is also part of the integrating capacitors of the main Gm–C filter. Capacitors can occupy a large area in layout. So using sharing capacitors can save a lot of chip area, which will be shown in the measurement result.

After optimizing the bias current and the transistor size, the unit transconductor achieves less than 1% total harmonic distortion (THD) when V_{pp} = 700 mV. The I_o simulated for different values of V_{gm} are plotted in Fig. 5. In Fig. 6, the simulated small-signal transconductance is plotted as a function of the input voltage for different V_{gm}. With the nominal bias conditions, the transconductance does not vary by more than ±0.8%. For higher bias currents, the "hump" in the middle of the G_m curve is enhanced, suggesting that for the transistors operating more deeply in strong inversion, the optimum ratio β_1/β_3 is larger. In contrast, that "hump" tends to disappear at lower current densities where the optimum β_1/β_3 is smaller. In the two latter cases the ripple in the transconductance characteristic has

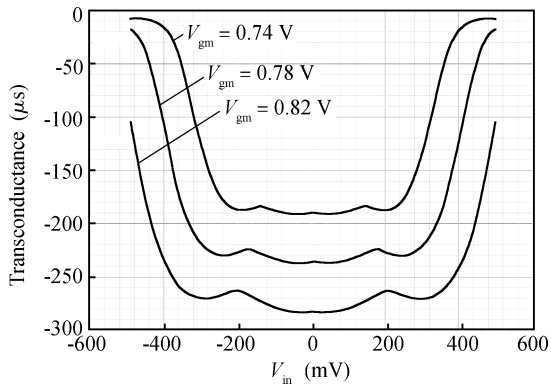

Fig. 6. Simulation results of the transconductance with different V_{gm}.

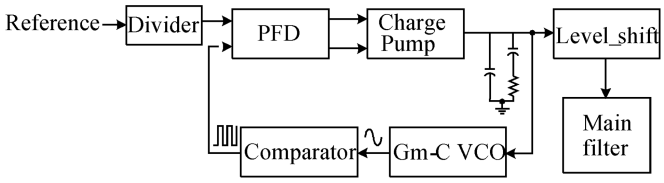

Fig. 7. Frequency tuning loop based on the PLL.

increased up to ±1.6%.

In this implementation, input transistors M1–M4 are in a common p-well connected to ground. Consequently, the transconductance is slightly dependent on the DC input common-mode voltage. This dependence may reduce the supply rejection capability but it does not degrade the linearity performance.

$$I_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + \cdots . \quad (1)$$

If the input common-mode voltage is not constant with respect to the bulk potential, even-order terms will appear in the i/v transfer characteristic, as shown in Eq. (1). These distortions may be minimized by increasing the bulk reverse voltage to reduce the body effect. For a purely differential mode input signal, the remaining even-order distortions would result from device mismatch, which has to be minimized by appropriate layout disposition.

In spite of its linear range being limited to $V_{in} < V_{DSAT1}$, this Gm cell shows low sensitivity to common-mode input signals and offers an attractive combination of good high-frequency behavior, linearity, and low power dissipation for a reduced circuit complexity.

3.3. Frequency automatic tuning

Automatic tuning is of critical importance to control the frequency response of continuous-time filters. Many conventional approaches reveal the use of a PLL. The PLL tunes the center or cutoff frequency of the filter indirectly by tuning on its own the oscillation frequency. So when the PLL has wide bandwidth, it will provide the filter wide channel-selected performance. The automatic tuning circuit should be as simple as possible to consider additional power consumption, chip area and noise. The PLL can achieve these requirements. The PLL configuration used in this design is shown in Fig. 7.

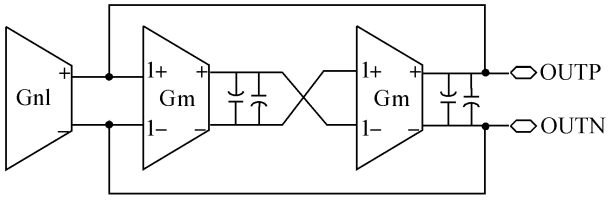

Fig. 8. VCO based on the Gm–C integrator.

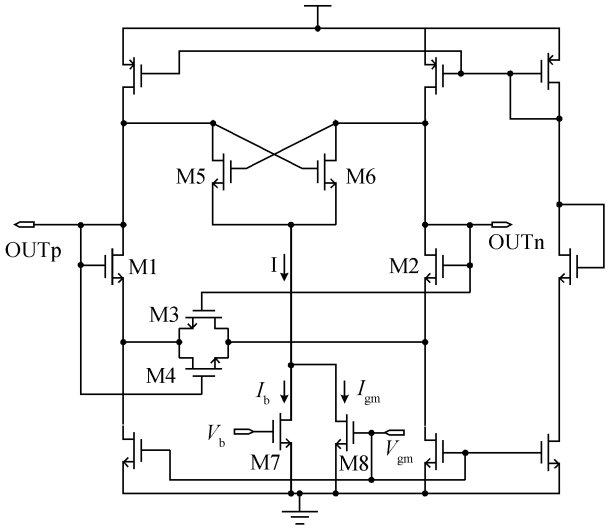

Fig. 9. Implementation of the nonlinear transconductor Gnl cell.

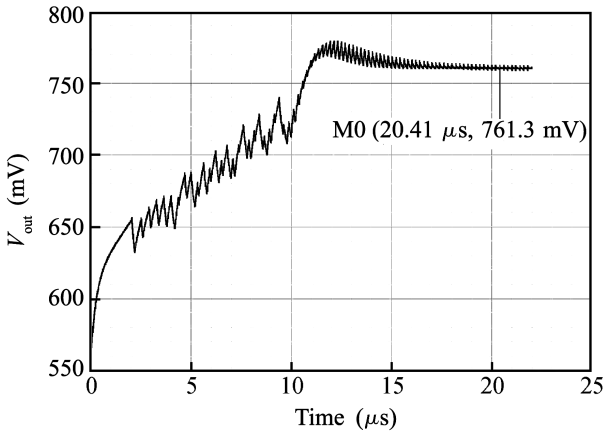

Fig. 10. Simulation result of the control signal generated by the PLL.

As opposed to the preceding PLL, absolute phase accuracy is not necessary since only the relative phase variations of one signal with respect to the other must be detected. The requirements on the PFD are thus relaxed. The main problem then is the implementation of the VCO that is well-matched to the filter to be tuned. The best candidate is usually a second-order harmonic oscillator[4], the amplitude regulation of which must be carefully considered since harmonic distortion and nonlinearities in the transconductors would shift the effective oscillation frequency, thus introducing a tuning error. For a Gm–C topology, with identical Gm cell, the parasitics are nearly the same from integrator to integrator. As good matching properties between the filter and the VCO are required, the VCO is built around a specific two-integrator loop which is implemented by the same Gm cell and with approximately the same parasitic-to-functional capacitor ratio and layout disposition. In addition, an amplitude regulation circuit is needed in the VCO based on a Gm–C integrator, as shown in Fig. 8. This is because, if the amplitude of the VCO is beyond the input linear range of the Gm cell, the transconductance G_m for a small signal will have errors and the VCO will not match to the main filter.

The implementation of nonlinear transconductor (Gnl cell) used for the amplitude regulation is shown in Fig. 9. A cross-coupled differential pair (M5 and M6), which provides negative transconductance, is added to the linearized transconductance stage (M1 to M4) connected in unity gain and provides positive transconductance. In the traditional design, there is only a tunable bias current source I_{gm}. Then when V_{gm} changes the bias current has a large changing range which would cause the negative transconductance to be too big or too small and lead to poor action and distortion of the VCO. The bias current source for the negative transconductance has been improved with a simple but effective method in this design. As shown in Fig. 8, a stable bias current source I_b (produced by M7 under fixed bias voltage V_b) is added with tunable current I_{gm} (controlled by the tunable voltage V_{gm}) to form the bias current I together. Because of the added stable current source, I can only change over a reasonable range. So the variation range of the negative transconductance is limited to be suitable, and the amplitude of the VCO is prevented from being too small or too big, which finally prevents distortion. To achieve the same linearity performance, transistors (M1 to M4) must operate at the same gate overdrive voltage as the input stage (transistors M1 to M4 in Fig. 4) of the other linearized Gm cell used in the VCO and in the main filter. For small signals, the Gnl cell is equivalent to a negative conductance; this will therefore ensure that oscillations build up when connected to a passive LC resonant circuit. The amplitude of the VCO will increase until the current I flowing through the Gnl cell has no more components at the resonant frequency f_0 of the two-integrator loop. In order to keep good control of the oscillation amplitude, the bias current and device sizes of the auxiliary cross-coupled pair M5 and M6 must be chosen in such a way that $\int_0^{T_0} VI\,\mathrm{d}t$ presents a maximum slope around zero. Considering our application, the Gnl cell can ensure a well-controlled oscillation amplitude (within the linear range of the Gm cell used in the two-integrator loop) while keeping the harmonic distortion at an acceptable level.

To avoid the VCO disturbing the filter while keeping good matching properties, the oscillation frequency is set to 10 MHz, which is the first zero of the filter. To minimize the error between the pole frequency of the PLL and the reference frequency (tuning error), the PFD should have low offsets. The loop filter is combined by discrete devices. The simulation result of the control signal generated by the PLL is shown in Fig. 10.

The unit Gm cell and capacitor is the basic unit cell in the core filter. Hence, the frequency response of the filter is automatically tuned by the frequency tuning loop. However, the practical tuning accuracy will be limited by the device matching. Proper layout, routing and placement of the device are critical to limit the device mismatches.

Table 1. Measurement results of the filter and comparison with other works.

	This work	Yao[6]	Yang[7]	Tea[8]
Technology	0.35 μm CMOS	0.25 μm CMOS	0.35 μm nwell CMOS	0.18 μm CMOS
Supply voltage (V)	2.85	3.3	3.3	1.8
Filter type	6th Butterworth	5th elliptic	9th Bessel	5th Bessel–Chebyshev
Cutoff frequency f_0 (MHz)	5 , 10.19	4	8	20
Die size (mm^2)	0.175	2	0.4	0.72
Current consumption (mA)	1.4 (f_0 = 5 MHz)	13	19.7	7.5
	2.81 (f_0 = 10 MHz)	13	19.7	7.5
Passband IIP3 (dBm)	0	–	–	–7.0
Bandwidth accuracy	3%	< 1%	–	–
Stopband attenuation (dB)	−33 @ 20 MHz (f_0 = 10 MHz)	−40	−95	−18
THD	1% @ V_{pp} = 750 mV	0.7% @ V_{pp} = 632 mV	< −60 dB	–
DR (dB)	77.5 @ 1% THD	54 @ 0.7% THD	–	–

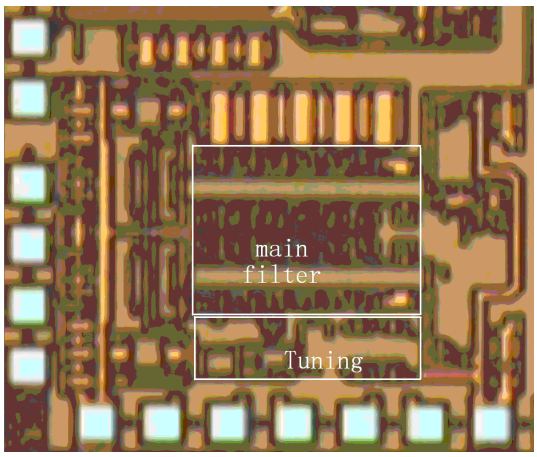

Fig. 11. Die photo of the filter system.

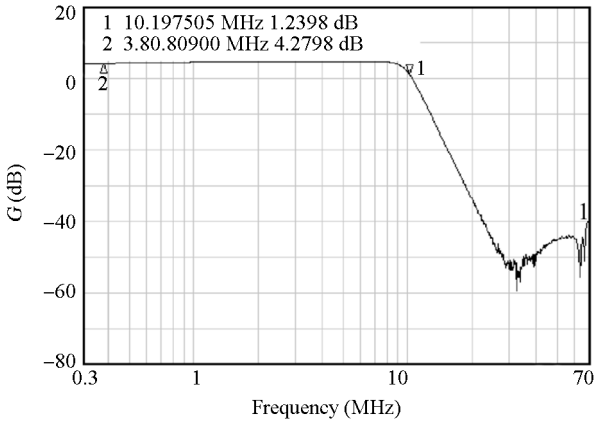

Fig. 12. Measured filter frequency AC response.

4. Measurement results

Figure 11 shows a die photograph of the sixth-order continuous-time leapfrog Gm–C filter, which has been implemented in IBM 0.35 μm CMOS technology. The frequency automatic tuning system occupies 0.045 mm^2 die size, while the main filter occupies 0.13 mm^2. The layout of the Gm cells and the capacitor array in the VCO are put near to the layout of the Gm cells and the capacitor array in the main filter, to make sure that the Gm cells match and the capacitors match[5].

The measured frequency AC characteristics of the filter are illustrated in Fig. 12. The filter shows a cutoff frequency of 10.19 MHz at 25 ℃. Figure 13 shows the measured in-band OIP3. The experimental result is measured with a VGA gain of 6 dB. The input power is −18 dBm, therefore the in-band IIP3 is 0 dBm according to Eq. (2). The measured output noise is about 100 μV, so the DR is 77.5 dB.

$$\mathrm{IIP_3}|_{\mathrm{dBm}} = \frac{\Delta P|_{\mathrm{dBm}}}{2} + P_{\mathrm{in}}|_{\mathrm{dBm}}. \quad (2)$$

The group delay ripple of the novel Butterworth filter is larger than the ripples of other filter types. So a first-order delay equalizer is added into the sixth-order Butterworth LPF to flatten the passband group delay variation, as shown in Fig. 1. The measurement result of the group delay variation is given in Fig. 14 and we can see that the group delay variation is only 16.3 ns, which is a successful improvement.

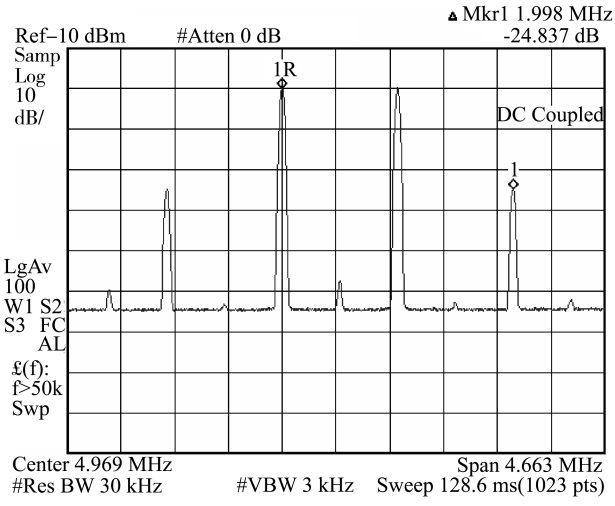

Fig. 13. Measured in-band OIP3 of the filter.

Table 1 summarizes the measurement results of the sixth-order continuous-time leapfrog Gm–C filter.

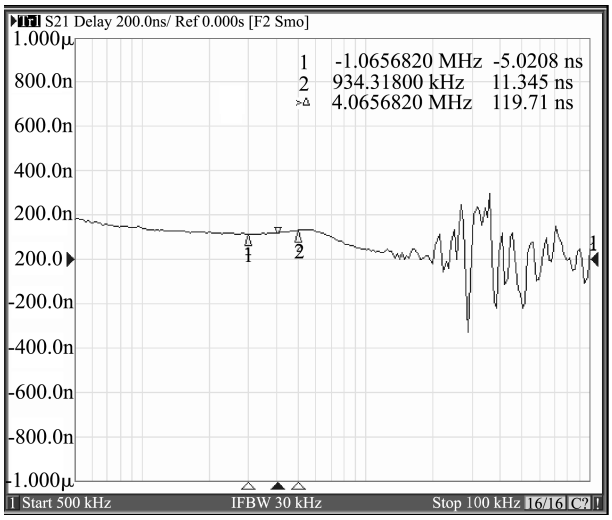

Fig. 14. Measured group delay variation of the filter.

5. Conclusion

This paper presents a sixth-order Butterworth leapfrog Gm–C filter for WLAN transceiver applications. It was realized in IBM 0.35 μm CMOS technology. The DR has been improved, while the chip size and current consumption have been successfully reduced. The measurement results show that the continuous-time Gm–C filter satisfies the WLAN transceiver specification well.

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