Design and application of a depletion-mode NJFET in a high-voltage BiCMOS process

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Abstract: A novel depletion-mode NJFET compatible high-voltage BiCMOS process is proposed and experimentally demonstrated with a four-branch 12-bit DAC (digital-to-analog converter). With this process, an NJFET with a pinch-off voltage of about –1.5 V and a breakdown voltage of about 16 V, an NLDDMOS (N-type lightly-dosed-drain in MOS) with a turn-on voltage of about 1.0 V and a breakdown voltage of about 35 V, and a Zener diode with a reverse voltage of about 5.6 V were obtained. Measurement results showed that the converter had a reference temperature coefficient of less than ±25 ppm/℃, a differential coefficient error of less than ±0.3 LSB, and a linear error of less than ±0.5 LSB. The depletion-mode NJFET and its compatible process can also be widely used for high-voltage ADCs or DACs.

Key words: depletion-mode NJFET; high-voltage BiCMOS process; ADC; DAC; temperature coefficient
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1. Introduction

With the rapid development of information technology, requirements for ADC (analog-to-digital converter) and DAC (digital-to-analog converter) design in high-voltage BiCMOS processes are becoming more and more stringent[1,2]. To meet the demand, it is necessary to develop a new process that enables ADCs and DACs to operate at ±15 V supply voltage.

Generally speaking, a JFET has the advantages of high input-impedance, low $1/f$ noise (channel in bulk), low temperature drift, and so on[3–6]. In particular, there is a very low offset voltage; when a depletion-mode NJFET is used in the input stage of an amplifier for an ADC or DAC, it can commendably ensure conversion accuracy[1,4]. Also, an NJFET can be directly used to design startup circuits of reference voltage for converters. Therefore, the depletion-mode NJFET is one of the key devices in the high-voltage BiCMOS process.

In this paper, a new depletion-mode NJFET compatible high-voltage BiCMOS process is proposed. The difficulty in designing the NJFET is that the breakdown voltage will decline, while the pinch-off voltage will rise, if the N-type impurity in the channel is high enough; otherwise, the device will be an enhanced-mode NJFET. So, a tradeoff should be made between breakdown voltage and pinch-off voltage. Figure 1 shows cross sections of the NJFET compatible CMOS and bipolar devices merged in this process.

2. Design and optimization

To make a depletion-mode NJFET for ADC and DAC working at ±15 V, whose V_{TH} (pinch-off voltage) is –1.5 ± 0.5 V, the BV_{DSS} (drain to source breakdown voltage) must exceed 15 V, and the typical value is 16 V. In particular, the process for the JFET has to be compatible with the high-voltage BiCMOS process.

2.1. Device structure

As shown in Fig. 1, there are several PN junctions in the high-voltage BiCMOS process, such as P-WELL to N-SUB (N-substrate), LDD to P-WELL or N-SUB, P^+ (PRING) to N-SUB and drain/source to P-WELL or N-SUB. The depth of P-WELL is about 7 μm, and P^+ is about 1 μm, so P^+ is chosen to form the top-gate of the NJFET, in which NRES (the resistor is fabricated by lightly doping implantation of PHOS (phosphorus)) is used for the channel of the NJFET, as shown in Fig. 2.

2.2. Parameter optimization

In fabrication of an NJFET using a high-voltage BiCMOS process, the difficulty is to find the tradeoff between the pinch-off voltage and breakdown voltage. Figure 3 shows simulated transfer characteristics of the NJFET with NRES doping varying from 2.2×10^{17} to 8.2×10^{17} cm^{-3} in steps of 1.0×10^{17} cm^{-3}.

As shown in Fig. 3, when channel doping changed from 4.2×10^{17} to 8.2×10^{17} cm^{-3}, the pinch-off voltage dropped to –1 and –2 V and the breakdown voltage changed from 23 to 15 V, as shown in Fig. 4.

From Fig. 4, it can be seen that, as doping varies from 4.2×10^{17} to 8.2×10^{17} cm^{-3}, the breakdown voltage of the NJFET falls. It can also be seen that, as the channel doping varies between 6.2×10^{17} and 8.2×10^{17} cm^{-3}, the breakdown voltage and pinch-off voltage change from 19 and –1 to 16 V and –2 V, respectively.

In order to optimize the breakdown voltage, the drain of the PMOS combined with RESURF is used to fabricate the top-gate of the NJFET, and the channel doping is changed to 3.2×10^{17} cm^{-3}. Simulation results show that the breakdown voltage of the NJFET reaches 35 V, as shown in Fig. 5.

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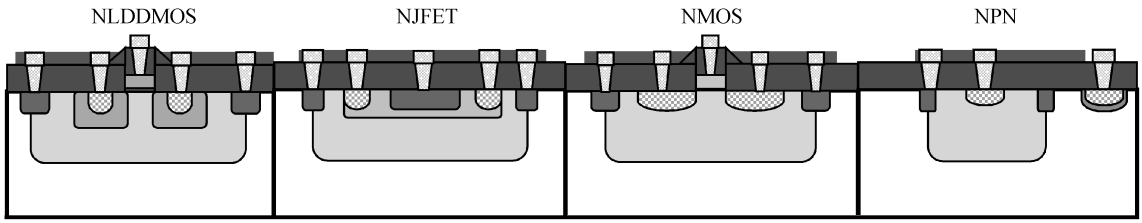

Fig. 1. Cross section of depletion-mode NJFET, CMOS and bipolar devices.

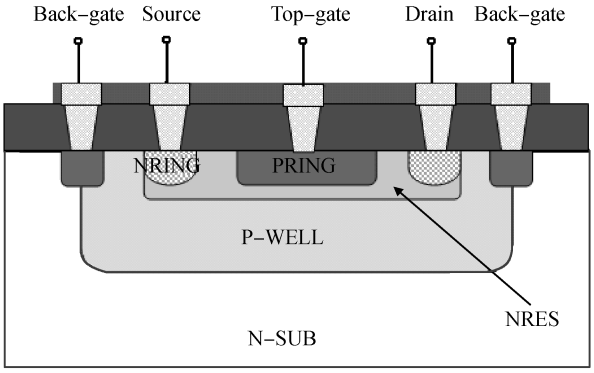

Fig. 2. Cross section of the proposed NJFET.

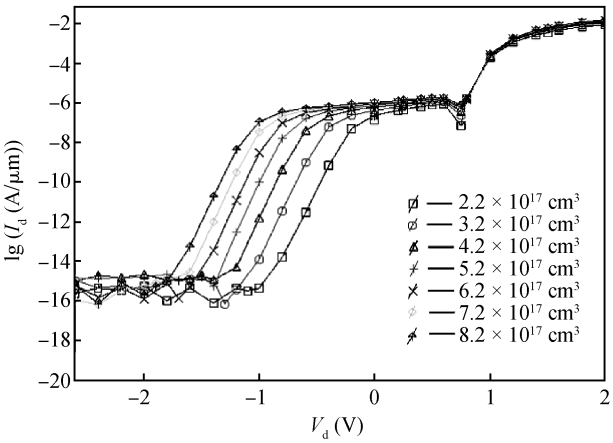

Fig. 3. Simulated transfer characteristics of the NJFET.

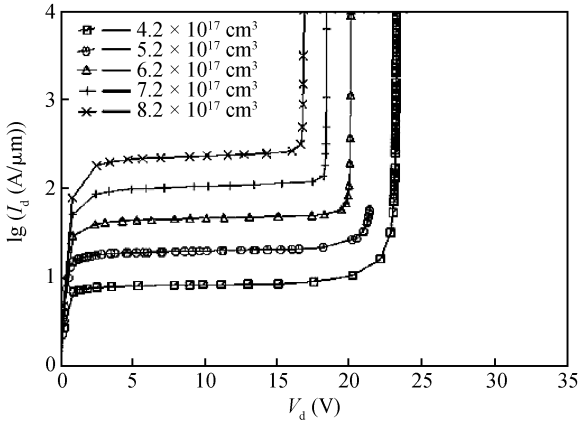

Fig. 4. Simulated breakdown voltage of the NJFET with doping changed from 4.2×10^{17} to 8.2×10^{17} cm^{-3} in 1.0×10^{17} cm^{-3} steps.

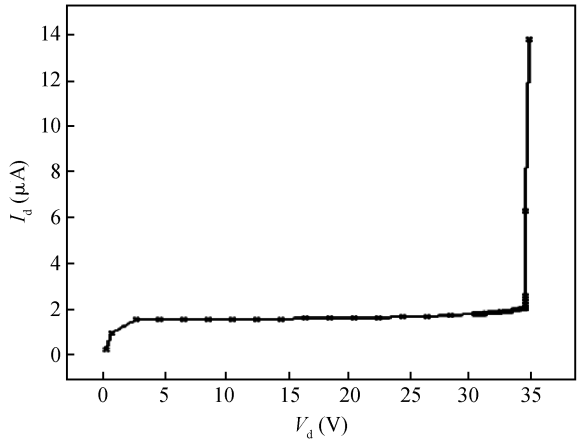

Fig. 5. Simulated breakdown voltage of the NJFET.

2.3. Device realization

The depletion-mode NJFET compatible high-voltage BiCMOS process is as follows:

Initial oxide → P-WELL photo/etch → thin oxide → boron implant → P-WELL drive → thin oxide → PLDD photo → PLDD boron implant → NLDD photo → NLDD PHOS implant → NBASE photo → PHOS implant → NRES photo → PHOS implant → annealing → PENH photo → boron implant → drive → remove all oxide → thin oxide → P + photo → high boron implant → N+(NRING) photo → high PHOS implant → deposit SiO_2 → annealing → ACTIVE photo/etch → light boron implant → low boron implant → gate oxide → deposit POLY (Poly-Silicon) → POLY doping → POLY photo/etch → PSD (drain and source of PMOS) photo → high boron implant → NSD (drain and source of NMOS) photo → high PHOS implant → deposit SiO_2 → annealing → LCONT photo/etch → Metallization.

For the NJFET, no additional step is needed. NRES photo and PHOS implant are used to obtain both the phosphorous implanted resistor and the NJFET channel. In particular, P+ photo and heavy boron implant are used to form the top-gate and PN junction isolation.

3. Results and application

Using the process steps described above, high-performance NJFETs are implemented, and based on the device, a 12-bit digital-to-analog converter is fabricated. Test results show that

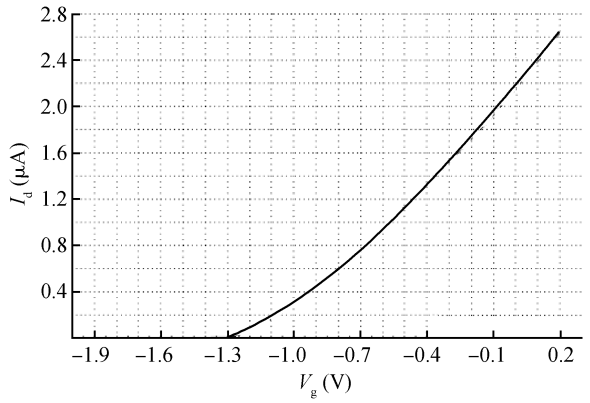

Fig. 6. Measured transfer characteristics of the NJFET.

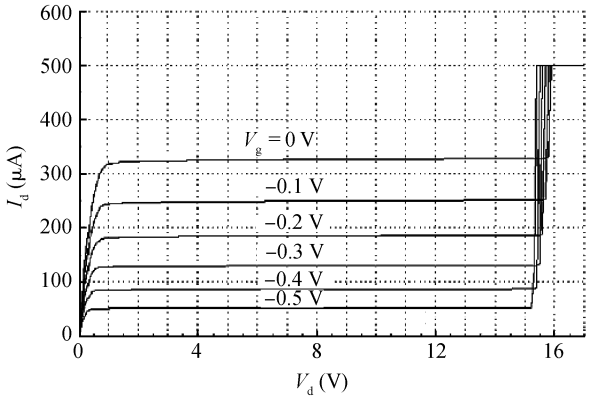

Fig. 7. Measured output characteristics of the NJFET.

Table 1. Performance of devices using the high-voltage BiCMOS process.

Device	Performance	Performance
NLDDMOS	BV_{DSS}> 35 V	0.8–1.2 V
PLDDMOS	BV_{DSS} < –35 V	–0.8 to –1.2 V
NMOS	BV_{DSS} > 18 V	0.8–1.2 V
PMOS	BV_{DSS} < –18 V	–0.8 to –1.2 V
VNPN	BV_{CEO} > 35 V	β = 200–300
VPNP	BV_{CEO} < –35 V	β = 20–40
NJFET	BV_{DSS} = 16 V	–1 to –2 V
Zener diode	V_F = 5.4–5.6 V	—

the NJFET has a pinch-off voltage of about –1.5 V and a breakdown voltage of about 16 V, as shown in Figs. 6 and 7, respectively. Some other devices are also fabricated in the high-voltage BiCMOS process. Table 1 is a summary of the measured parameters of devices fabricated in the process.

Figures 8–10 show a block diagram of the 12-bit DAC, its reference voltage curve (the temperature varies from –60 to 125 °C in 25 ℃ steps) and a microphotograph of the chip, respectively. Some parameters of the circuit are listed in Table 2.

Figure 9 shows that reference voltage of the DAC has an excellent temperature performance. The reason for this is that one of the two SiCr resistors in the reference will be trimmed with a laser to compensate for the variation if the temperature coefficient is positive, and the other resistor will be trimmed if the coefficient is negative. It can be seen from Table 2 that the

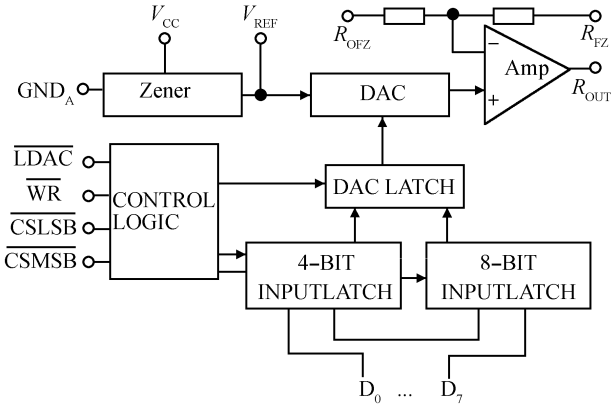

Fig. 8. Block diagram of the 12-bit DAC.

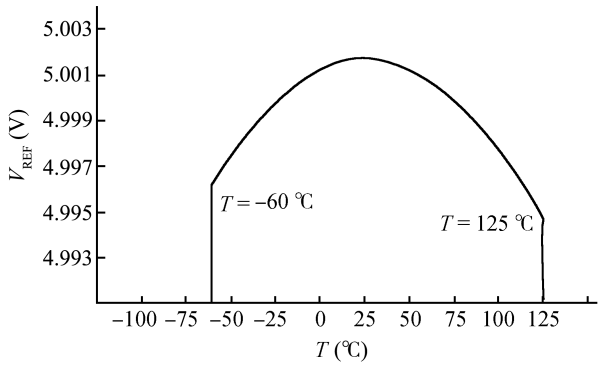

Fig. 9. Reference voltage curve of the DAC with temperature varying from –60 to 125 °C in 25 °C steps.

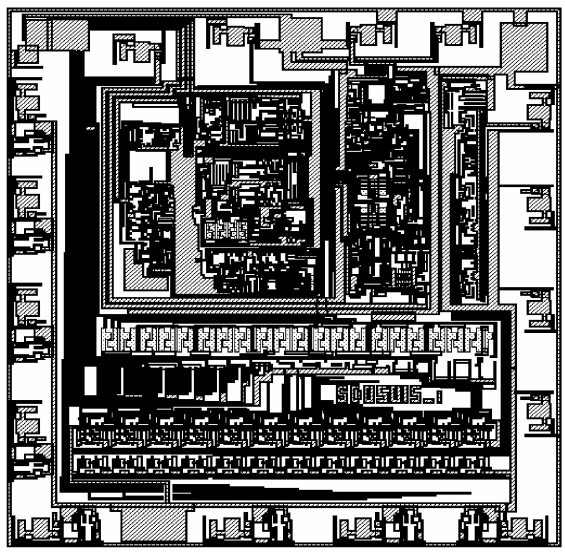

Fig. 10. Chip photo of the fabricated DAC.

DAC has a reference temperature coefficient of less than ±25 ppm/℃, a differential coefficient error below ±0.3 LSB, and a linear error of less than ±0.5 LSB.

Table 2. Some parameters of the 12-bit D/A converter.

Parameter	Symbol	Value
Resolution	R_{ES}	12 bits
Positive supply current	I_{DD}	8.5 mA
Negative supply current	I_{SS}	3 mA
Differential error	E_{DL}	±0.3 LSB
Unipolar offset error	E_{OU}	±1 LSB
Full range error	E_G	±3 LSB
Linear error	E_L	±0.5 LSB
Reference output	$V_{REF(OUT)}$	4.99–5.01 V
Reference temperature coefficient	αV_{REF}	±25 ppm/°C
Settling time	t_s	4 μs

4. Conclusion

A novel high-voltage BiCMOS process compatible with a depletion-mode NJFET is developed. Based on the NJFET and its compatible process, a four-channel 12-bit DAC is implemented, which, operating at +15 V and ±15 V, has a reference temperature coefficient of less than ±25 ppm/℃, a differential coefficient error of less than ±0.3 LSB, and a linear error below ±0.5 LSB. The proposed device and compatible process are applicable for other high voltage ADCs/DACs.

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