A process simplification scheme for fabricating CMOS polycrystalline-Si thin film transistors*

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Abstract: A process simplification scheme for fabricating CMOS poly-Si thin-film transistors (TFTs) has been proposed, which employs large-angle-tilt-implantation of dopant through a gate sidewall spacer (LATITS). By this LATITS scheme, a lightly doped drain region under the oxide spacer is formed by low-dose tilt implantation of phosphorus (or boron) dopant through the spacer, and then the n^+-source/drain (n^+-S/D) (or p^+-S/D) region is formed via using the same photo-mask layer during CMOS integration. For both n-TFT and p-TFT devices, as compared to the sample with conventional single n^+-S/D (or p^+-S/D) structure, the LATITS scheme can cause an obviously smaller leakage current, due to more gradual dopant distribution and thus smaller electric field. In addition, the resultant on-state currents only show slight degradation for the LATITS scheme. As a result, by the LATITS scheme, CMOS poly-Si TFT devices with an on/off current ratio well above 8 orders may be achieved without needing extra photo-mask layers during CMOS integration.

Key words: polycrystalline-Si thin-film transistor; process simplification; large-angle-tilt-implantation
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1. Introduction

In recent years, polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) have been extensively studied for their potential use in static random-access memory and in the integration of peripheral driving circuits in high-resolution active matrix liquid crystal displays (AMLCDs) due to their large mobility[1, 2]. However, due to the presence of defects in poly-Si TFTs, some issues have to be resolved in comparison with single crystalline transistors. A leakage current is increased with increasing gate and drain voltage due to the field emission via trap states in the depletion region near the drain. This is one of the bias-dependent issues caused by defects in poly-Si TFTs, which yields poor switching characteristics such as low on/off current ratio[3−6]. TFT devices with lower on/off current ratio, used as pixel switching in AMLCD, represent a limiting factor for operation and can degrade the performance of the display.

By a conventional scheme, single n^+-S/D (or p^+-S/D) implantation is carried out after the gate delineation. Hence, large leakage current would be caused, due to the large electric field intensity in the depletion region near the drain region. It has been reported that a lightly-doped-drain (LDD) structure can effectively decrease the leakage current and the kink current in polysilicon TFTs due to reduction of electric field intensity near the drain region[7−11]. However, the above device fabrication processes would need more process steps. In particular, for CMOS integration, two extra photo-masking layers have to be employed for carrying out the n-LDD and the p-LDD implantation process.

In this study, a process simplification scheme for forming CMOS poly-Si TFT devices has been proposed. The scheme is implemented by using large-angle-tilt implantation (LATI) of dopant through an oxide sidewall spacer to form the n- (or p-) lightly doped drain (LDD) region below the oxide spacer and then performing n^+-S/D (or p^+-S/D) implantation in the same photo-mask layer. Hence, by the above process-simplification scheme, an LDD region may be formed without needing an extra photo-mask layer during CMOS process integration. In addition, the resultant CMOS poly-Si TFT devices can cause lower off-state leakage current and kink current than those formed by the conventional single-n^+-S/D (or p^+-S/D) implantation scheme.

2. Device scheme

A 100-nm-thick amorphous silicon (a-Si) film was firstly deposited on standard glass substrate by low-pressure-chemical-vapor-deposition (LPCVD) at 580 ℃. Then, the a-Si thin film was crystallized by 308-nm XeCl excimer-laser annealing. After defining the active device layer, an 80-nm-thick tetra-ethyl-ortho-silane (TEOS) gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD), as a gate dielectric, at 400 ℃. A 300-nm-thick poly-Si film was then deposited, and delineated as a gate electrode of 4-μm channel length and 10-μm channel width. Figure 1(a) shows the schematic structure of the TFT fabrication during gate formation. Some of the samples were then phosphorus-implanted with n^+-S/D implantation at an energy of 80 keV to a dose of 4×10^{15} cm^{-2}, namely, the conventional scheme. Figure 1(b) shows the schematic structure of the conventional n-TFT

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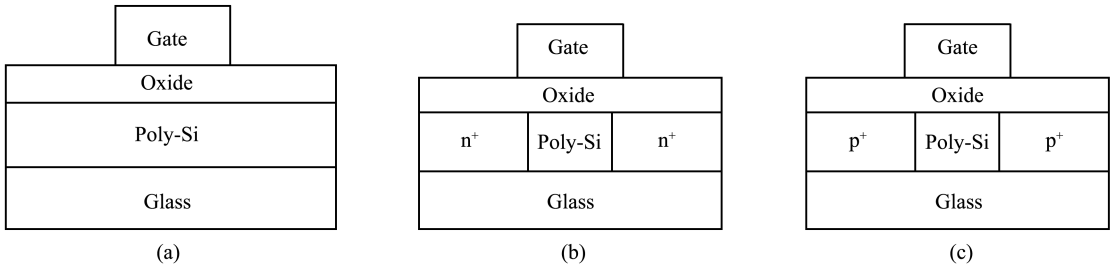

Fig. 1. (a) Schematic structure of TFT fabrication during gate formation. (b) Schematic structure of n-TFT fabrication during n^+-S/D formation. (c) Schematic structure of p-TFT fabrication during p^+-S/D formation.

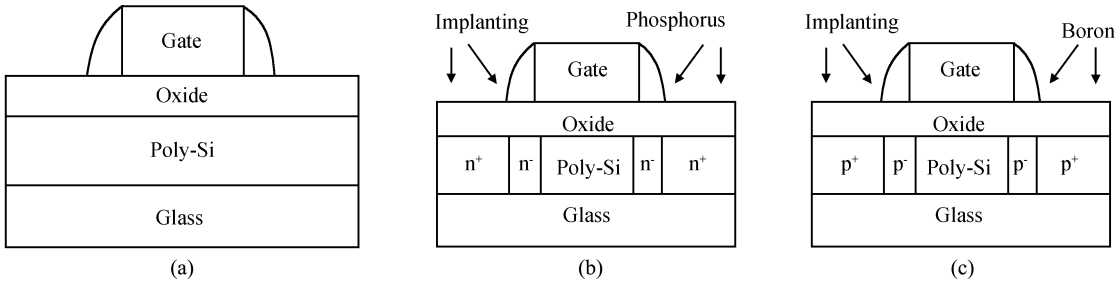

Fig. 2. (a) Schematic structure of TFT fabrication during spacer formation. (b) Schematic structure of n-TFT fabrication with the scheme that uses large-angle-tilt-implantation of phosphorus dopant through a spacer. (c) Schematic structure of p-TFT fabrication with the scheme that uses large-angle-tilt-implantation of boron dopant through a spacer.

fabrication during n^+-S/D formation. In addition, some of the post-gate-delineated samples were then boron-implanted with p^+-S/D implantation at an energy of 25 keV to a dose of 2×10^{15} cm^{-2}. Figure 1(c) shows the schematic structure of the conventional p-TFT fabrication during p^+-S/D formation. It is noted that, for CMOS process integration, only two photo-mask layers were required for implementing the p^+-S/D and n^+-S/D implantation.

On the other hand, other post-gate-delineated samples were directly deposited with a 250-nm-thick low-temperature-oxide (LTO) film and anisotropically etched. An oxide spacer of about 0.25 μm width was formed. Figure 2(a) shows the schematic structure of the TFT fabrication while the spacer formation. Subsequently, some of the samples were large-angle-tilt implanted with phosphorus dopant through the oxide spacer at an energy of 100 keV to a dose of 6×10^{13} cm^{-2} and a tilt angle of 45°, to form a lightly doped n^--region below the oxide spacer. The LATI process was carried out with rotation of the wafer to avoid the implantation gate-shadow effect. Then, without removing the photo-resist mask layer, the samples were further implanted with phosphorus dopant at 80 keV to a dose of 4×10^{15} cm^{-2} to form the n^+-S/D region. It is noted that, for CMOS process integration, by this scheme only one photo-masking step is required for the n^+-S/D implantation and the formation of the lightly doped n^--region. Figure 2(b) shows the schematic structure of the n-TFT fabrication that employs the scheme of large-angle-tilt-implantation of dopant through a spacer (LATITS).

In addition, some of the post-spacer-formed samples were large-angle-tilt implanted with boron dopant through the oxide spacer at an energy of 40 keV to a dose of 6×10^{13} cm^{-2} and a tilt angle of 45°, to form a lightly doped p^--region below the oxide spacer. Then, without removing the photo-resist mask layer, the samples were further implanted with boron dopant at 20 keV to a dose of 2×10^{15} cm^{-2} to form the p^+-S/D region. It is noted that, for CMOS process integration, by this scheme only one photo-masking step is required for the p^+-S/D implantation and the formation of the lightly doped p^--region. Figure 2(c) shows the schematic structure of the p-TFT fabrication that employs the LATITS scheme.

For all the samples, the implanted dopant was activated by furnace annealing at 600 °C for 90 min. Then, an 800-nm-thick TEOS oxide was deposited by PECVD as a passivation layer. Contact holes were formed, and a 1200-nm-thick Al film was subsequently deposited and patterned. Finally, all the samples were sintered at 300 °C for 45 min in a forming gas ambient.

3. Results and discussion

For n-channel poly-Si TFT devices, by the LATITS scheme, the resultant off-state current is about one order lower than that by the conventional scheme. Figure 3 shows the drain current as a function of gate voltage for n-channel poly-Si TFT devices formed by the conventional scheme and the LATITS scheme, respectively, biased at V_{DS} of 5 V. In addition, no considerable degradation of the on-state characteristics is found by using this process simplification scheme. Hence, this LATITS scheme can provide sufficient dopant to form a lightly doped n^--region under the oxide spacer.

By using the LATITS scheme, the suppressed leakage current is attributed to a smaller electric field intensity in the depletion region near the drain region, as compared to the conventional scheme. Figures 4(a) and 4(b) show the phosphorus dopant distribution profiles for n-channel poly-Si TFT devices formed by the conventional and LATITS schemes, correspondingly, from the TSUPREM-4 simulation[12]. In addition,

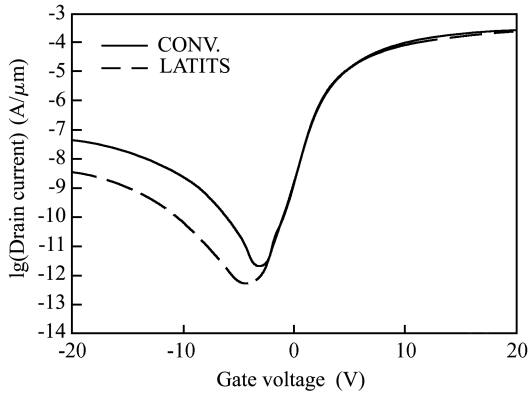

Fig. 3. I_{DS}–V_{GS} characteristic at V_{DS} of 5 V for n-TFT devices formed by the conventional single n^+-S/D scheme and the LATITS scheme, respectively.

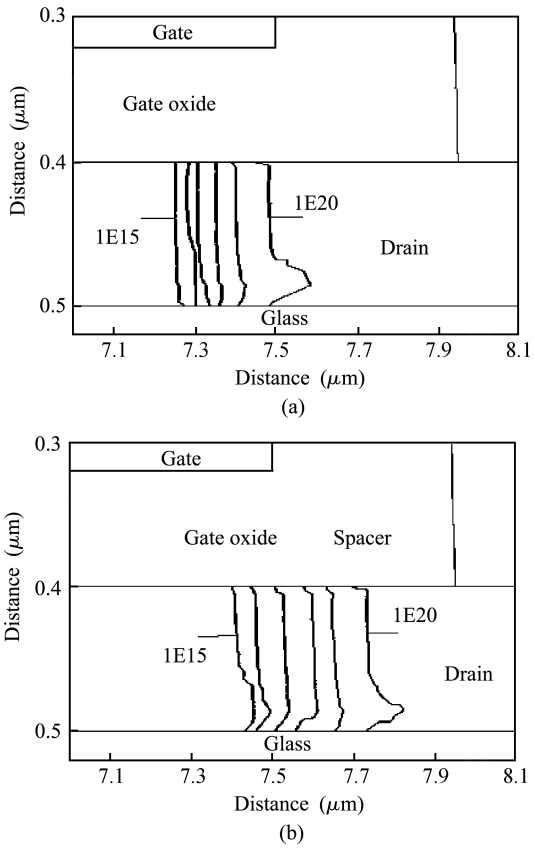

Fig. 4. Phosphorus dopant distribution profiles for n-TFT devices formed by (a) the conventional single n^+-S/D and (b) the LATITS schemes, correspondingly, from the TSUPREM-4 simulation.

Figure 5 shows the profiles of phosphorus dopant distribution along the channel surface for the n-TFT devices formed by the conventional single n^+-S/D and LATITS schemes, correspondingly. It is found that the LATITS scheme results in a wider dopant distribution and thus a more gradual dopant distribution than the conventional scheme, due to high-energy/low-dose tilt implantation. Hence, by this LATITS scheme, lower electrical field intensity near the drain is caused, and thus the leakage current due to carrier field emission via trap states can be suppressed.

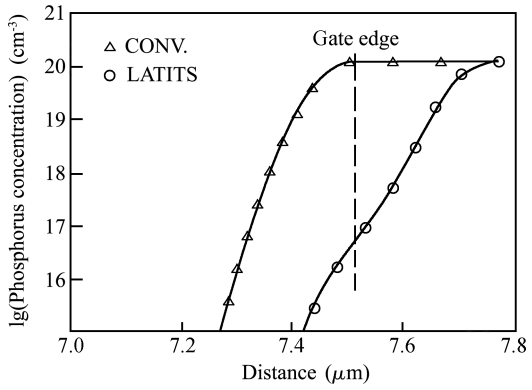

Fig. 5. Profiles of phosphorus dopant distribution along the channel surface for n-TFT devices formed by the conventional single n^+-S/D and LATITS schemes, correspondingly, from the TSUPREM-4 simulation.

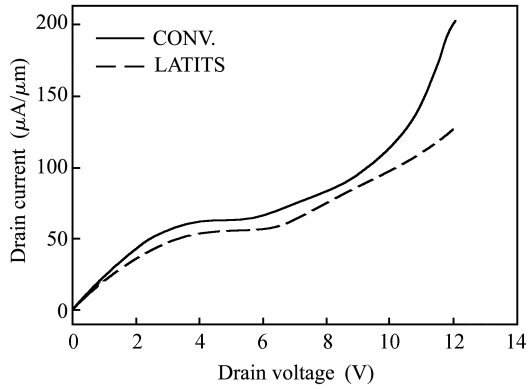

Fig. 6. Drain current as a function of drain voltage for the conventional single n^+-S/D scheme and the LATITS scheme, respectively, biased at a gate voltage of 8 V.

In addition, the oxide spacer would retard both the phosphorus dopant tilt-implanted into the substrate and the encroachment of n^+-S/D-implanted dopant into the channel region. Hence, also from Figs. 4(a) and 4(b), the conventional scheme leads to a shorter effective channel length than the LATITS scheme. As a result, LATITS would cause a slightly smaller on-state current than the conventional scheme. Figure 6 shows the drain current as a function of drain voltage for n-channel poly-Si TFT devices formed by the conventional scheme and the LATITS scheme, respectively, biased at a gate voltage of 8 V. In addition, the LATITS sample may cause less kink current than the conventional sample, primarily due to the lower electric field near the drain region. Furthermore, in terms of the device reproducibility and uniformity, Figures 7(a) and 7(b) illustrate the number of samples distributed at different leakage currents for the LATITS and conventional samples, correspondingly, biased at V_{GS} of –10 V and V_{DS} of 5 V. No considerable difference is found for the samples among three different process substrates, which reflects the good reproducibility. In addition, no significant difference between the uniformity of the conventional and LATITS schemes is found, which reflects that the device uniformity is not degraded by using the LATITS scheme.

On the other hand, for p-channel poly-Si TFT devices, by

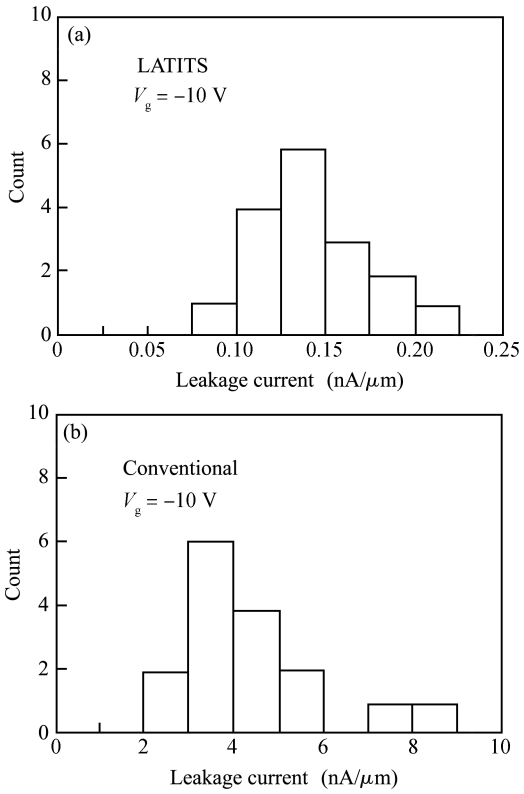

Fig. 7. Number of samples distributed at different leakage currents for (a) the LATITS and (b) the conventional samples, correspondingly, biased at V_{GS} of –10 V and V_{DS} of 5 V.

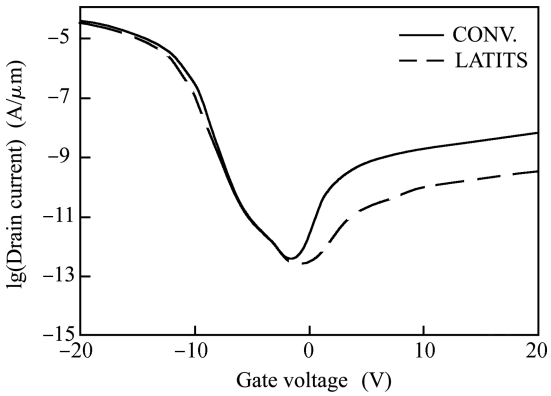

Fig. 8. I_{DS}–V_{GS} characteristic at V_{DS} of −5 V for p-TFT devices formed by the conventional single p^+-S/D scheme and the LATITS scheme, respectively.

the LATITS scheme, the resultant off-state current is lower than that by the conventional scheme. Figure 8 shows the drain current as a function of gate voltage for p-channel poly-Si TFT devices formed by the conventional scheme and the LATITS scheme, respectively, biased at V_{DS} of −5 V. In addition, no considerable degradation of the on-state characteristics is found by using this process simplification scheme. Hence, this LATITS scheme can provide sufficient boron dopant to form a lightly doped p^--region under the oxide spacer.

By using the LATITS scheme for p-TFT devices, the suppressed leakage current is primarily attributed to the smaller electric field intensity in the depletion region near the drain

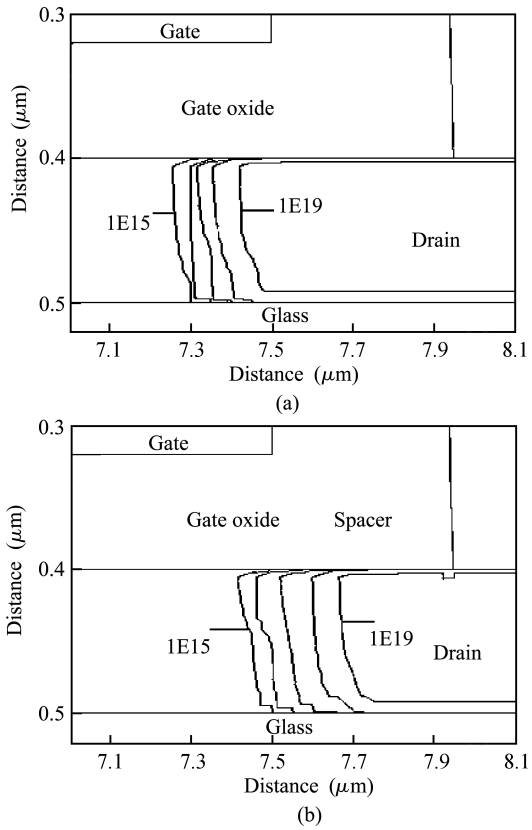

Fig. 9. Boron dopant distribution profiles for p-TFT devices formed by (a) the conventional single p^+-S/D and (b) the LATITS schemes, correspondingly, from the TSUPREM-4 simulation.

region, as compared to the conventional scheme. Figures 9(a) and 9(b) show the boron dopant distribution profiles for the p-channel poly-Si TFT devices formed by the conventional and LATITS schemes, correspondingly, from the TSUPREM-4 simulation[12]. It is found that the LATITS scheme results in a wider dopant distribution than the conventional scheme, due to high-energy/low-dose tilt implantation. Hence, by this LATITS scheme, lower electrical field intensity near the drain is caused, and thus the leakage current due to carrier field emission via trap states can be suppressed. In addition, the oxide spacer would retard both the boron dopant tilt-implanted into the substrate and the encroachment of p^+-S/D-implanted dopant into the channel region. Hence, also from Figs. 9(a) and 9(b), the conventional scheme leads to a shorter effective channel length than the LATITS scheme. As a result, LATITS would cause a slightly smaller on-state current than the conventional scheme. Figure 10 shows the drain current as a function of drain voltage for p-channel poly-Si TFT devices formed by the conventional scheme and the LATITS scheme, respectively, biased at a gate voltage of –12 V. In addition, for p-TFT, the LATITS sample may cause less kink current than the conventional sample, primarily due to the lower electric field near the drain region.

4. Conclusions

The formation of CMOS poly-Si TFT devices by the LATITS scheme has been studied for process simplification. By this LATITS scheme, a lightly doped drain region under a gate sidewall oxide spacer is formed by low-dose tilt implan-

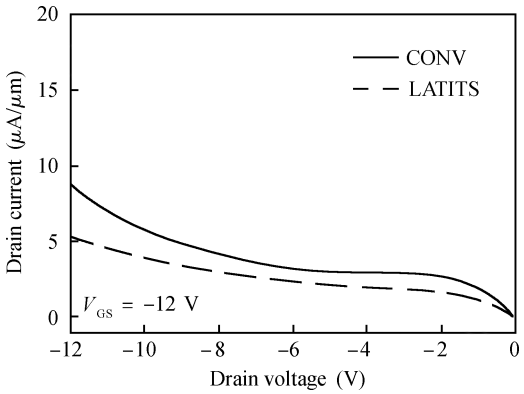

Fig. 10. Drain current as a function of drain voltage for the conventional single p^+-S/D scheme and the LATITS scheme, respectively, biased at a gate voltage of –12 V.

tation of phosphorus (or boron) dopant through the spacer, and then the n^+-S/D (or p^+-S/D) region is formed via using the same photo-mask layer during CMOS integration. For both n-TFT and p-TFT devices, as compared to the sample with conventional single n^+-S/D (or p^+-S/D) structure, the LATITS scheme can cause an obviously smaller leakage current, due to more gradual dopant distribution and thus smaller electric field. In addition, the resultant on-state current only shows slight degradation for the LATITS scheme, primarily due to the larger effective channel length. As a result, by the LATITS scheme, CMOS poly-Si TFT devices with on/off current ratios well above 8 orders may be achieved without needing extra photo-mask layers during CMOS integration.

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