A novel wideband low phase noise 2 : 1 frequency divider

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Abstract: This paper describes a novel low-power wideband low-phase noise divide-by-two frequency divider. Hereby, a new D-latch topology is introduced. By means of conventional dynamic source-coupled logic techniques, the divider demonstrates a wideband with low phase noise by adding a switch transistor between the clock port and the couple node of the input NMOS pair in the D latch. The chip was fabricated in the 90-nm CMOS process of IBM. The measurement results show that the frequency divider has an input frequency range from 0.05 to 10 GHz and the phase noise is –159.8 dBc/Hz at 1 MHz offset from the carrier. Working at 10 GHz, the frequency divider dissipates a total power of 9.12 mW from a 1.2 V supply while occupying only 0.008 mm^2 of the core die area.

Key words: frequency divider; wideband; low phase noise
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1. Introduction

Frequency dividers are required for many applications, such as frequency synthesis in high speed wireless communication systems, quadrature signal generators, and clock recovery circuits. The commonly used architectures of high speed frequency dividers are source-coupled logic (SCL) dividers, regenerative dividers, and injection locked dividers. Although the latter two architectures can achieve a high speed with low power consumption, they are inherently narrow band[1], so this is not suitable for wideband systems. In comparison with them, SCL is a configuration with high speed, wideband, and appropriate power consumption. So the SCL architecture is widely applied in high speed wideband wireless communications. However, when the supply voltage drops below 1 V, the performance of SCL degrades significantly, and some of them even fail to function[2]. So Razavi's structure[3] is widely applied in the low supply voltage. The disadvantage of the structure is that the bandwidth is not wide enough to work at low frequency. On the other hand, a high spectrum purity divider with wideband is more and more important for many applications, such as software radio. So the traditional SCL structure should be improved to fit the demands of low supply voltage, high spectrum purity, and wideband.

In this paper, a 1.2 V, 0.05–10 GHz low phase noise divide-by-two frequency divider is designed with a novel D-latch topology and designed in a 90-nm CMOSLP process. The circuit of the designed divider principle is briefly explained. A theoretical analysis of the bandwidth and phase noise is described.

2. Principle of the designed frequency divider

Figure 1(a) shows a block diagram of the divide-by-two frequency divider. It consists of two D latches which are cross-coupled with each other. It is based on master and slave latches connected in series. All the latch data signals are differential and the clock signals are pseudo differential. Each D latch is triggered by one clock signal, CLK or $\overline{\text{CLK}}$. These two D latches always operate periodically and alternately between the sampling mode and holding mode. So the cross connection between the output of the slave latch and the input of the master latch causes the clock frequency to be divided by two. Figure 1(b) shows the schematic of the designed D latch. The cross-coupled NMOS pair (M1, M2) is used as a positive feedback to hold the output signals in the holding mode. The input NMOS pair (M3, M4) is implemented to sample the input signals in the sampling mode. The pair of PMOS transistors (M6, M7) is implemented to the dynamic loading and an NMOS transistor (M5) is used as a switch in order to expand the bandwidth.

The operating principle of the design is based on the dynamic sampling and alternating operations of the D latches. In the sampling mode, the PMOS loading transistors are operated in a linear region and the switching transistor (M5) turns on. The turn-on resistance of the load is very small, thus achieving a small RC time constant at the output node. Then, the charge up or charge down current is very large. Such a small RC time constant and large current make the NMOS pair (M3, M4) sample the D input and charge-discharge the output nodes at the maximum speed. In the holding mode, the PMOS loading transistor and switching transistors (M5) are turned off and achieve a large RC output time constant in the output node. At the same time, the charge-discharge down current is very small. Such a large RC time constant and small current make the cross-coupled NMOS pair (M1, M2) hold the output state of the D latch at the maximum time. Thus, the dynamic load technique and switching transistor greatly increases the range of the frequency divider's operating frequency.

3. Bandwidth analysis

The operating frequency of the designed frequency divider is determined by the sampling and holding time. To predict the operating frequency, simplified schematics of the two modes are shown in Fig. 2, respectively.

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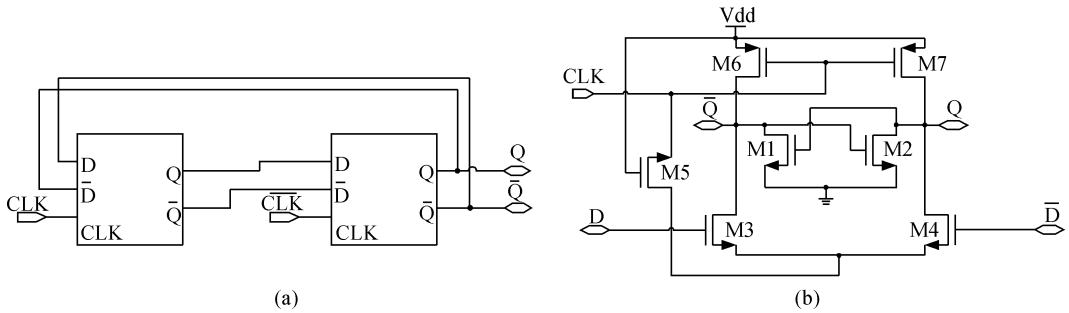


Fig. 1. (a) Block schematic of the divide-by-two SCL frequency divider. (b) Schematic of the designed D latch.

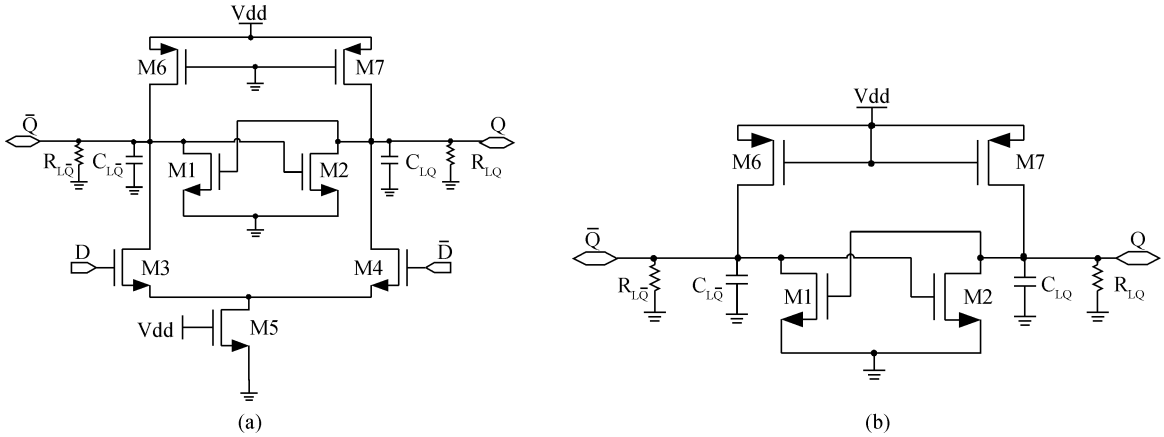


Fig. 2. Simplified schematic of the D latch. (a) In sampling mode. (b) In holdling mode.

Figure 2(a) shows a simplified schematic of the D latch in sampling mode. The speed of sampling is limited by the RC time constant and the charge-discharge current. If CLK is at the low level, the D latch is in sampling state. It is supposed that at the beginning, D and $\overline{Q}$ ports are at the high level, then $\overline{D}$ and Q ports are at the low level. Thus, M3 is turned on, and M4 is turned off. The charge-down time constant ($\tau_{s\overline{Q}}$) is given by

$$\tau_{s\overline{Q}} \approx (C_{GDM6} + C_{GSM2} + C_{GDM2} + C_{L\overline{Q}}) \times \left[r_{on6} || (r_{on3} + r_{on5}) || R_{L\overline{Q}}\right], \quad (1)$$

and the charge-up time constant (τ_{sQ}) is given by

$$\tau_{sQ} \approx \left(C_{GDM7} + C_{GSM1} + C_{LQ}\right)\left(r_{on7} || r_{on2} || R_{LQ}\right), \quad (2)$$

where r_{on2} is the on-resistance of M2, r_{on3} is the on-resistance of M3, r_{on5} is the on-resistance of M5, r_{on6} is the on-resistance of M6 and r_{on7} is the on-resistance of M7; $L_{L\overline{Q}}$ and R_{LQ} include parasitic and load resistance; $C_{L\overline{Q}}$ and C_{LQ} include load and parasitic capacitance.

According to the characteristics of the RC charge-up or charge-down circuit, the rise and fall times are determined by the time constant and charge-up or charge-down current. In the sampling mode, the current charge-up is supplied by M6 or M7, which are approximately equal; at the same time, the current of the charge-down is equal to $i_{M5} - i_{M6}$ or $i_{M5} - i_{M7}$. The two time constants and the current are different, so the rise and the fall time are not equal. Finally, the sampling time is determined by the maximum of the rise time and fall time.

Figure 2(b) shows the schematic and equivalent circuit of the D latch in holding mode. The holding time is limited by the RC time constant and the leakage current. When CLK is at the high level, the D latch is in holding mode. It is supposed that at first time D and $\overline{Q}$ ports are at the high level, $\overline{D}$ and Q ports are at the low level. At the holding mode, the time constant ($\tau_{h\overline{Q}}$) is given by

$$\tau_{h\overline{Q}} \approx (C_{GDM6} + C_{GDM1} + C_{GSM2} + C_{GDM2} + C_{L\overline{Q}})R_{L\overline{Q}}, \quad (3)$$

and the time constant (τ_{hQ}) is given by

$$\tau_{hQ} \approx (C_{GDM7} + C_{GDM1} + C_{GSM1} + C_{GDM2} + C_{LQ})R_{LQ}. \quad (4)$$

At the holding mode, the current only contains the small leakage current, it does not vary with the level of D and the time constant of the two ports is same, so the holding current is determined by the technology.

Compared to the divider which was designed by Razavi in Ref. [3], the holding time of the novel frequency divider is larger while sharing the same sampling time at the same condition. So the designed divider has a wider bandwidth.

4. Phase noise analysis

In Fig. 1(a), the jitter at the output of this divider is not affected by the noise of the first latch, since the output signals is not controlled by the latch. Thus, only the noise sources of the second latch need to be considered in the output jitter assessment. The time jitter can be computed from the variance of

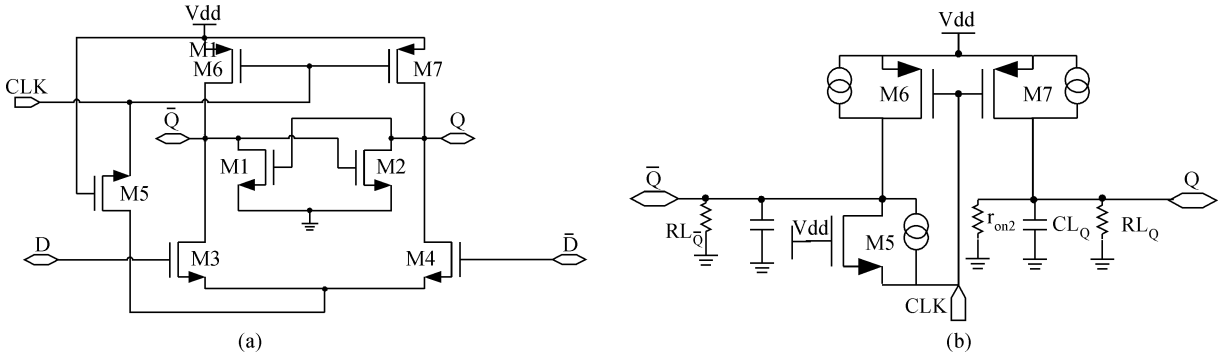


Fig. 3. (a) Schematic of the designed D latch. (b) Simplified schematic of the same circuit with a noise source.

output voltage $\hat{V}_{\mathrm{o}}^2$ as in Ref. [4]:

$$\sigma_{t_0}^2 = \frac{\hat{V}_{\mathrm{o}}^2}{S_{\mathrm{L}}^2}, \tag{5}$$

where S_{L} is the slope of the output voltage at the zero crossings. The period jitter ($\sigma_{T\mathrm{out}}^2$) is computed as

$$\sigma_{T_{\mathrm{out}}}^2 = \sigma_{t_{\mathrm{H0}}}^2 + \sigma_{t_{\mathrm{L0}}}^2. \tag{6}$$

According to the expression $\phi = 2\pi f_{\mathrm{out}} t_0$, the phase of the output signal is sampled at $f_{\mathrm{out}} = 1/T_{\mathrm{out}}$ and it is proportional to the switching instant. The sampling process folds back any noise component at frequency higher than $f_{\mathrm{out}}/2$ and the phase spectrum is defined in the Nyquist band 0–$f_{\mathrm{out}}/2$. Then, the time jitter can be written in terms of the integral of the single-sided power spectral density (PSD) of the phase within the Nyquist band[5]:

$$\sigma_{t_0}^2 = \frac{1}{4\pi^2 f_{\mathrm{out}}^2} \int_0^{f_{\mathrm{out}}/2} S_\phi(f)\mathrm{d}f. \tag{7}$$

For proper operation of the divider, the D signals of the second latch have already switched completely before the CLK signal starts to switch. Therefore, M3 is off and M4 is in the triode region. The same happens to the transistors M1 and M2. Thus, the circuit in Fig. 3(a) can be further simplified as shown in Fig. 3(b).

From the schematic in Fig. 3(b), we can simply estimate the time delay between the input clock switching and the zero-crossing instant of the output signals Q and $\overline{\mathrm{Q}}$. Both of the transient signals Q and $\overline{\mathrm{Q}}$ have an approximately exponential waveform with the different time constant $\left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right) C_{\mathrm{LQ}}$ and $\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right) C_{\mathrm{L}\overline{\mathrm{Q}}}$. The noise sources affecting the output zero crossing are also represented in Fig. 3(b). Therefore, the noise sources are a pair of PMOS transistors (M6, M7) and NMOS switching transistor (M5).

4.1. White phase noise

For white noise, $S_\phi(f) = W$ is constant and Equation (6) gives the link between the jitter and the phase spectrum. The single-side-band-to-carrier ratio (SSCR or L) is

$$l_{\mathrm{w}} = \frac{W}{2} = 4\pi^2 f_{\mathrm{out}} \sigma_{t_{0,\,\mathrm{total}}}^2. \tag{8}$$

The linear dependence of l_{w} on the output frequency is in accordance with the model designed by Kroupa[4, 6].

4.1.1. Dynamic load transistors

In practice, the level of the CLK signal is low and the transistors of M6 and M7 work in the linear region when the CLK signal starts to switch. So the output noise currents of M6 and M7 are

$$\begin{aligned}\hat{i}_{\mathrm{o6}}^2 &= 4kT\left[\alpha\gamma\left(g_{\mathrm{m6}}|_{V_{\mathrm{ds6}}=0}\right)\right]\cdot \mathrm{BW} \\ &= kT\left[\alpha\gamma\mu_{\mathrm{n}}C_{\mathrm{ox}}\frac{W_6}{L_6}\left(V_{\mathrm{GS6}}-V_{\mathrm{TH}}\right)\right]\frac{1}{\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on6}}||r_{\mathrm{on5}}\right)C_{\mathrm{L}\overline{\mathrm{Q}}}},\end{aligned} \tag{9}$$

$$\begin{aligned}\hat{i}_{\mathrm{o7}}^2 &= 4kT\left[\alpha\gamma\left(g_{\mathrm{m7}}|_{V_{\mathrm{ds7}}=0}\right)\right]\cdot \mathrm{BW} \\ &= kT\left[\alpha\gamma\mu_{\mathrm{n}}C_{\mathrm{ox}}\frac{W_7}{L_7}\left(V_{\mathrm{GS7}}-V_{\mathrm{TH}}\right)\right]\frac{1}{\left(L_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)C_{\mathrm{LQ}}},\end{aligned} \tag{10}$$

where γ and α are the noise factor and the constant relating to technology, respectively. Their current noise is alternatively injected into nodes Q and $\overline{\mathrm{Q}}$. From the schematic in Fig. 3(b), the variance voltage of Q port and $\overline{\mathrm{Q}}$ port are

$$\hat{V}_{\mathrm{Q}}^2(t) = \left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)^2 \hat{i}_{\mathrm{o7}}^2 \mathrm{e}^{-\frac{2t}{\left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)C_{\mathrm{LQ}}}}, \tag{11}$$

$$\hat{V}_{\overline{\mathrm{Q}}}^2(t) = \left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right)^2 \hat{i}_{\mathrm{o6}}^2 \mathrm{e}^{-\frac{2t}{\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right)C_{\mathrm{L}\overline{\mathrm{Q}}}}}. \tag{12}$$

Without considering the noise effect, we assume that Q is at low level and $\overline{\mathrm{Q}}$ is at high level. The transient voltages of Q and $\overline{\mathrm{Q}}$ are

$$\begin{aligned}V_{\mathrm{Q}}(t) = {} & \frac{V_{\mathrm{DD}}}{r_{\mathrm{on7}}}\left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)\left(1-\mathrm{e}^{-\frac{t}{\left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)C_{\mathrm{LQ}}}}\right) \\ & + V_{\mathrm{Q}}(0_-),\end{aligned} \tag{13}$$

$$\begin{aligned}V_{\overline{\mathrm{Q}}}(t) = {} & \left(\frac{V_{\mathrm{DD}}}{r_{\mathrm{on6}}}-\frac{V_{\mathrm{DD}}}{r_{\mathrm{on5}}}\right)\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right) \\ & \times \mathrm{e}^{-\frac{t}{\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right)C_{\mathrm{L}\overline{\mathrm{Q}}}}} + V_{\overline{\mathrm{Q}}}(0_-).\end{aligned} \tag{14}$$

Thus, at the zero crossings, the slopes of Q port voltage and $\overline{\mathrm{Q}}$ port voltage are equal to

$$S_{\mathrm{LQ}} = \frac{V_{\mathrm{DD}}}{C_{\mathrm{LQ}} r_{\mathrm{on7}}}, \tag{15}$$

$$S_{\mathrm{L}\overline{\mathrm{Q}}} = \left(\frac{V_{\mathrm{DD}}}{r_{\mathrm{on5}}} - \frac{V_{\mathrm{DD}}}{r_{\mathrm{on6}}}\right)\frac{1}{C_{\mathrm{L}\overline{\mathrm{Q}}}}. \tag{16}$$

Taking Eq. (5) into account, at the moment of $t = 0$, the jitter due to the dynamic load transistor noise can be written as:

$$\sigma^2_{t_0,\mathrm{Q}} = \frac{\left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)^2 \hat{i}^2_{\mathrm{o7}}}{\left(S_{\mathrm{LQ}}\right)^2} = \left(\frac{C_{\mathrm{LQ}} r_{\mathrm{on7}}}{V_{\mathrm{DD}}}\right)^2 \left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)^2 \hat{i}^2_{\mathrm{o7}}, \tag{17}$$

$$\sigma^2_{t_0,\overline{\mathrm{Q}}} = \frac{\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on6}}||r_{\mathrm{on5}}\right)^2 \hat{i}^2_{\mathrm{o6}}}{\left(S_{\mathrm{L}\overline{\mathrm{Q}}}\right)^2} = \left(\frac{C_{\mathrm{L}\overline{\mathrm{Q}}} r_{\mathrm{on6}} r_{\mathrm{on5}}}{V_{\mathrm{DD}}(r_{\mathrm{on6}} - r_{\mathrm{on5}})}\right)^2 \left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on6}}||r_{\mathrm{on5}}\right)^2 \hat{i}^2_{\mathrm{o6}}. \tag{18}$$

The two random processes described by Eqs. (8) and (9) are uncorrelated, so Equations (16) and (17) are uncorrelated. We can get

$$\sigma^2_{t_0,\mathrm{total}} = \sigma^2_{t_0,\mathrm{Q}} + \sigma^2_{t_0,\overline{\mathrm{Q}}}. \tag{19}$$

4.1.2. Switching transistors

M5 works in the linear region when the CLK signal starts to switch. Thus, the output noise current of M5 is

$$\hat{i}^2_{\mathrm{o5}} = 4kT\left[\alpha\gamma\left(g_{\mathrm{m5}}|_{V_{\mathrm{ds5}}=0}\right)\right]\cdot \mathrm{BW} = kT\left[\alpha\gamma\mu_{\mathrm{n}} C_{\mathrm{ox}}\frac{W_5}{L_5}\left(V_{\mathrm{GS5}} - V_{\mathrm{TH}}\right)\right]\frac{1}{\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on6}}||r_{\mathrm{on5}}\right)C_{\mathrm{L}\overline{\mathrm{Q}}}}. \tag{20}$$

The current noise is injected into node $\overline{\mathrm{Q}}$. So the variance voltage across $\overline{\mathrm{Q}}$ port is

$$\hat{V}^2_{\overline{\mathrm{Q}}}(t) = \left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right)^2 \hat{i}^2_{\mathrm{o5}}\left(1 - \mathrm{e}^{-\frac{2t}{\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on5}}||r_{\mathrm{on6}}\right)C_{\mathrm{L}\overline{\mathrm{Q}}}}}\right). \tag{21}$$

At the moment of $t = 0$, $\hat{V}^2_{\overline{\mathrm{Q}}}(0) = 0$. So the switching transistor noise has no effect on the port $\overline{\mathrm{Q}}$.

4.1.3. Total white phase noise

The total jitter is obtained from the three noise contributions of Eqs. (17) and (18). The correspondent phase noise level follows from Eqs. (8) and (19), and it is

$$l_{\mathrm{total},W} = 2\pi\alpha\gamma\mu_{\mathrm{n}} C_{\mathrm{ox}}\frac{W_6}{L_6}\left(V_{\mathrm{GS6}} - V_{\mathrm{TH}}\right)\frac{r^2_{\mathrm{on7}} C_{\mathrm{LQ}}}{V^2_{\mathrm{DD}}} \times\left[R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}} + \left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on6}}||r_{\mathrm{on5}}\right)\left(\frac{r_{\mathrm{on5}}}{r_{\mathrm{on6}} - r_{\mathrm{on5}}}\right)^2\right] f_{\mathrm{out}}. \tag{22}$$

Notes: $V_{\mathrm{GS6}} = V_{\mathrm{GS7}}, r_{\mathrm{on6}} \approx r_{\mathrm{on7}}, C_{\mathrm{LQ}} \approx C_{\mathrm{L}\overline{\mathrm{Q}}}$ and $R_{\mathrm{LQ}} \approx R_{\mathrm{L}\overline{\mathrm{Q}}}$.

4.2. Flicker phase noise

Because of the sampling effect, the flicker noise is convenient to analyze in the frequency domain. The output voltage noise at frequency ($kf_{\mathrm{out}} \pm f_{\mathrm{m}}$) (with $k = 0, 1, \ldots$ and $f_{\mathrm{m}} < f_{\mathrm{out}}/2$) can be represented as a signal with amplitude V_{m} and random phase. Because of sampling, this voltage signal causes a phase variance ϕ_{m} at f_{m}, it can be calculated as

$$\phi_{\mathrm{m}} = 2\pi f_{\mathrm{out}}\frac{V_{\mathrm{m}}}{S_{\mathrm{L}}}. \tag{23}$$

Hence, the phase noise spectrum can be written as

$$\ell_{\mathrm{w}} = \frac{2\pi^2 f^2_{\mathrm{out}}}{{S_L}^2} S^{\mathrm{folded}}_{\mathrm{V}}(f_{\mathrm{m}}), \tag{24}$$

where $S^{\mathrm{folded}}_{\mathrm{V}}(f_{\mathrm{m}})$ is the PSD of the output voltage noise folded in the Nyquist band from 0 to $f_{\mathrm{out}}/2$.

If the corner frequency of the voltage spectrum is lower than $f_{\mathrm{out}}/2$, the flicker component undergoes no folding and $S^{\mathrm{folded}}_{\mathrm{V}}(f_{\mathrm{m}})$ in Eq. (24) can be substituted by the unfolded spectrum $S_{\mathrm{V}}(f_{\mathrm{m}})$. As a result, the phase noise in the flicker region is proportional to the square of the output frequency f_{out}. This dependence has been experimentally verified in Ref. [6].

Once the PSD of the output voltage $S_{\mathrm{V}}(f_{\mathrm{m}})$ has been expressed in the terms of the noise source, Equation (24) can be used to estimate the phase noise of a frequency divider in the flicker region.

4.2.1. Dynamic load transistors

In practice, the level of the CLK signal is low and the transistors begin to work on the triode region when the CLK signal starts to switch. So the output noise currents of M6 and M7 respectively are

$$\hat{i}^2_{\mathrm{o6,f}} = \frac{K_{\mathrm{f}}\left(g_{\mathrm{m6}}|_{V_{\mathrm{ds6}}=0}\right)^2}{W_6 L_6 C_{\mathrm{ox}}}\frac{\mathrm{BW}}{f} = \frac{K_{\mathrm{f}} W_6 C_{\mathrm{ox}}\left[kT\alpha\gamma\mu_{\mathrm{n}}\left(V_{\mathrm{GS6}} - V_{\mathrm{TH}}\right)\right]^2}{L^3_6} \times\frac{1}{f}\frac{1}{4\left(R_{\mathrm{L}\overline{\mathrm{Q}}}||r_{\mathrm{on6}}||r_{\mathrm{on5}}\right)C_{\mathrm{L}\overline{\mathrm{Q}}}}, \tag{25}$$

$$\hat{i}^2_{\mathrm{o7,f}} = \frac{K_{\mathrm{f}}\left(g_{\mathrm{m7}}|_{V_{\mathrm{ds7}}=0}\right)^2}{W_7 L_7 C_{\mathrm{ox}}}\frac{\mathrm{BW}}{f} = \frac{K_{\mathrm{f}} W_7 C_{\mathrm{ox}}\left[kT\alpha\gamma\mu_{\mathrm{n}}\left(V_{\mathrm{GS7}} - V_{\mathrm{TH}}\right)\right]^2}{L^3_7} \times\frac{1}{f}\frac{1}{4\left(R_{\mathrm{LQ}}||r_{\mathrm{on7}}||r_{\mathrm{on2}}\right)C_{\mathrm{LQ}}}, \tag{26}$$

where K_{f} is a constant relating to the technology.

In the frequency domain, the transfer function between the flicker noise current spectrum and the output noise voltage spectrum is

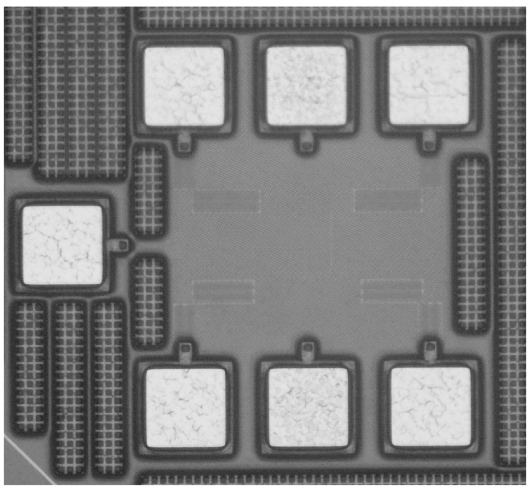


Fig. 4. Chip photograph of the designed frequency divider.

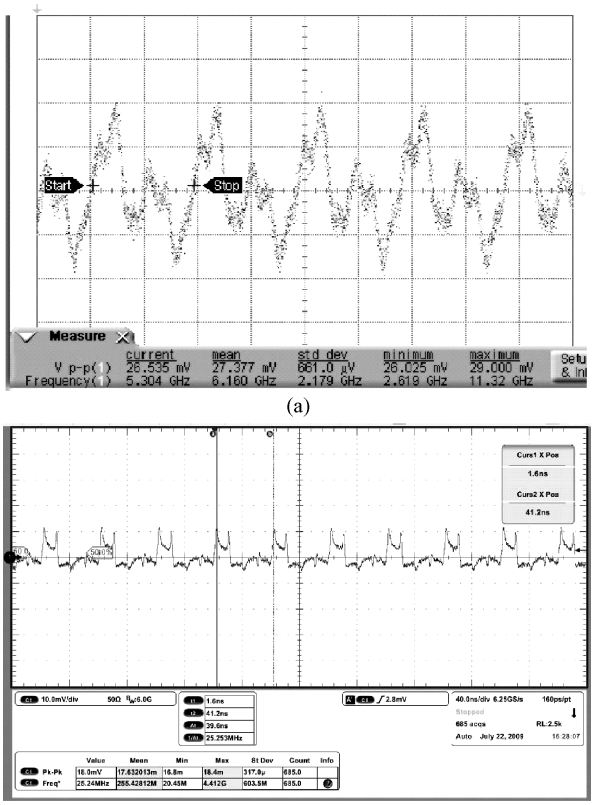
$$
\begin{aligned}
\left|Z_{\mathrm{Q}}(f)\right|^2 &= \frac{1}{4\pi^2 f^2 {C_{\mathrm{LQ}}}^2 + \left(\dfrac{1}{R_{\mathrm{LQ}}} + \dfrac{1}{r_{\mathrm{on7}}} + \dfrac{1}{r_{\mathrm{on2}}}\right)^2} \\
&\quad \times \left[\sum_{n=0}^{\infty} Sa(\frac{n\pi}{2})\delta(2\pi f - 2n\pi f_{\mathrm{out}})\right] \\
&= \frac{1}{2}\sum_{n=-\infty}^{\infty}\left\{Sa\left(\frac{n\pi}{2}\right) \times \left[4\pi^2 (f - nf_{\mathrm{out}})^2 {C_{\mathrm{LQ}}}^2 \right.\right. \\
&\quad \left.\left. + \left(\frac{1}{R_{\mathrm{LQ}}} + \frac{1}{r_{\mathrm{on7}}} + \frac{1}{r_{\mathrm{on2}}}\right)^2\right]^{-1}\right\},
\end{aligned}
\tag{27}
$$

$$
S_{\mathrm{V,Q}}^{\mathrm{folded}}(f) = \left|Z_{\mathrm{Q}}(f)\right|^2 \hat{i}_{\mathrm{o7,f}}^2. \tag{28}
$$

In order to simplify the analysis, we assume the corner frequency of the voltage spectrum is lower than $f_{\mathrm{out}}/2$. Thus, the phase noise can be written as

$$
\begin{aligned}
\ell_{\mathrm{Q,F}}(f) &= \frac{\pi^2}{2}\frac{f_{\mathrm{out}}^2}{S_{\mathrm{LQ}}}\frac{K_{\mathrm{f}} C_{\mathrm{ox}} W_7 \left[kT\alpha\gamma\mu_{\mathrm{n}}\left(V_{\mathrm{GS7}} - V_{\mathrm{TH}}\right)\right]^2}{L_7^3} \\
&\quad \times \frac{1}{f}\frac{1}{\left(R_{\mathrm{LQ}} || r_{\mathrm{on7}} || r_{\mathrm{on2}}\right) C_{\mathrm{LQ}}} \\
&\quad \times \frac{1}{4\pi^2 f^2 C_{\mathrm{LQ}}^2 + \left(\frac{1}{R_{\mathrm{LQ}}} + \frac{1}{r_{\mathrm{on7}}} + \frac{1}{r_{\mathrm{on2}}}\right)^2},
\end{aligned}
\tag{29}
$$

$$
\begin{aligned}
\ell_{\overline{\mathrm{Q}},\mathrm{F}}(f) &= \frac{\pi^2}{2}\frac{f_{\mathrm{out}}^2}{S_{\mathrm{L}\overline{\mathrm{Q}}}}\frac{K_{\mathrm{f}} C_{\mathrm{ox}} W_6 \left[kT\alpha\gamma\mu_{\mathrm{n}}\left(V_{\mathrm{GS6}} - V_{\mathrm{TH}}\right)\right]^2}{L_6^2} \\
&\quad \times \frac{1}{f}\frac{1}{\left(R_{\mathrm{L}\overline{\mathrm{Q}}} || r_{\mathrm{on6}} || r_{\mathrm{on5}}\right) C_{\mathrm{L}\overline{\mathrm{Q}}}} \\
&\quad \times \frac{1}{4\pi^2 f^2 C_{\mathrm{L}\overline{\mathrm{Q}}}^2 + \left(\frac{1}{R_{\mathrm{L}\overline{\mathrm{Q}}}} + \frac{1}{r_{\mathrm{on6}}} + \frac{1}{r_{\mathrm{on5}}}\right)^2}.
\end{aligned}
\tag{30}
$$



(a)

(b)

Fig. 5. Measured output voltage of single port (a) with 1.2-V-peak input signal at 10 GHz and (b) with 1.2-V-peak input signal at 50 MHz.

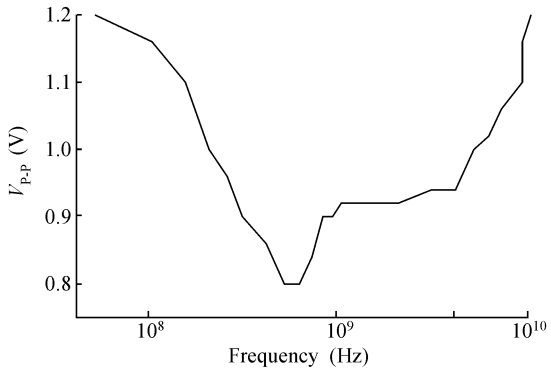


Fig. 6. Measurement of the sensitivity of the designed frequency divider.

4.2.2. Total flicker phase noise

The flicker noise of M5 has no effect on port ($\overline{\mathrm{Q}}$) due to the analysis in 4.1.2. According to Eqs. (6) and (7), the total flicker phase noise spectrum can be written as:

$$
\ell_{\mathrm{total,F}}(f) = \ell_{\mathrm{Q,F}}(f) + \ell_{\overline{\mathrm{Q}},\mathrm{F}}(f). \tag{31}
$$

5. Measurement results analysis

The divide-by-two dividers have been implemented in the 90-nm CMOS process of IBM. The chip photograph is shown in Fig. 4. The chip area is $360 \times 380\ \mu\mathrm{m}^2$ including the test circuits. The output waveforms are plotted in Fig. 5 for 10 GHz

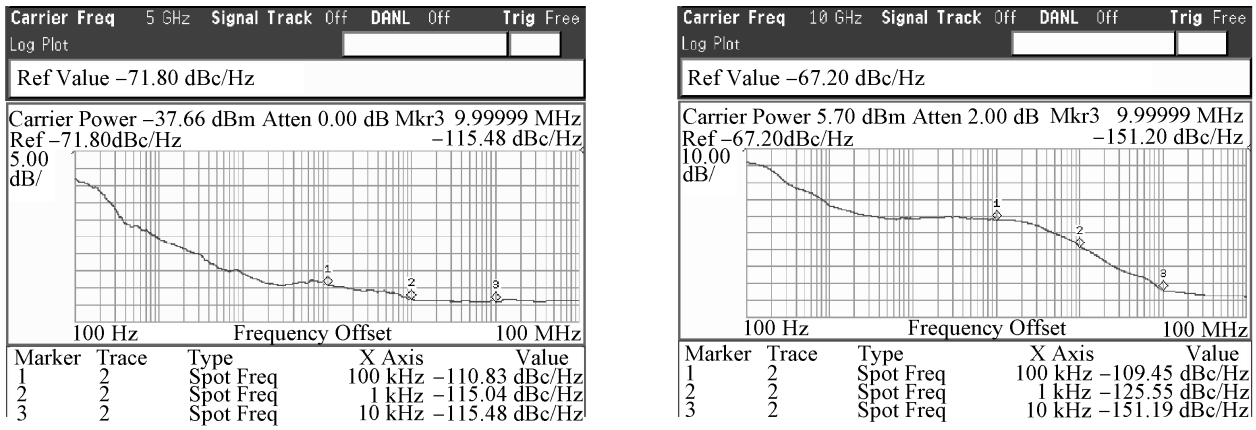


Fig. 7. Measured phase noise of single output port (a) with 1.2-V-peak input signal at 10 GHz and (b) 1.2-V-peak input signal at 10 GHz.

Table 1. Phase noise of single port output signal with input signal at 10 GHz.

Frequency offset	PN_{total} (dBc/Hz)	$PN_{in} + PN_m$ (dBc/Hz)	$PN_{fd} + PN_{tc} + PN_{sp}$ (dBc/Hz)	$PN_{fd} + PN_{tc}$ (dBc/Hz)
100 kHz	–110.83	–112.45	–123.90	–139.83
1 MHz	–115.04	–128.56	–123.24	–159.83
10 MHz	–115.48	–154.19	–123.48	–179.83

Table 2. Comparison with published results.

Technology	Operating frequency range (GHz)	Phase noise @ 1 MHz (dBc/Hz)	Power consumption (mW)	FOM (dB)
90 nm CMOS SOI, Ref. [8]	13–34	–127	60	115
90 nm CMOS SOI, Ref. [9]	5–66	–102	51	89
90 nm CMOS, Ref. [1]	2–35.5	–124.6	28.8	109.2
90 nm CMOS SOI, Ref. [10]	65–81	–112.6	2.75	87
90 nm CMOS, this work	0.05–11	–159.8	9.12	139.4

and 50 MHz input sinusoid signals with 1.2-V peak. The measured minimum input sensitivity V_{P-P} versus the input frequency of the frequency divider is plotted in Fig. 6. Above the minimum input voltage reliable operation is guaranteed. The minimum input voltage of the frequency dividers is less than 1.2 V in the frequency range of 0.05–10 GHz. The 1.2-V-peak input signal at the maximum operating frequency and minimum operating frequency are needed for the frequency divider. The measured power dissipation changes from 6.48 to 9.12 mW with the input signal frequency from 50 MHz to 10 GHz.

The phase noise of the output signal and input signal is measured by means of a spectrum analyzer. The measured results are shown in Fig. 7. From Fig. 7(a), we can see that the phase noise does not always decrease with increasing offset frequency. The results of measuring include the phase noise of the input signal (PN_{in}), the phase noise of the sampling effect (PN_{sp}), the phase noise of the measuring instrument (PN_{mi}), the phase noise of test circuits of the designed frequency divider (PN_{tc}) and the phase noise of the designed frequency divider (PN_{fd}). Among them, PN_{fd}, PN_{in} and PN_{tc} strictly increase with increasing operating frequency, the effect of PN_{sp} increases with decreasing operating frequency, and PN_{mi} is constant. The relationship between them is

$$PN_{total} = PN_{fd} + PN_{in} + PN_{sp} + PN_{mi} + PN_{tc}. \quad (32)$$

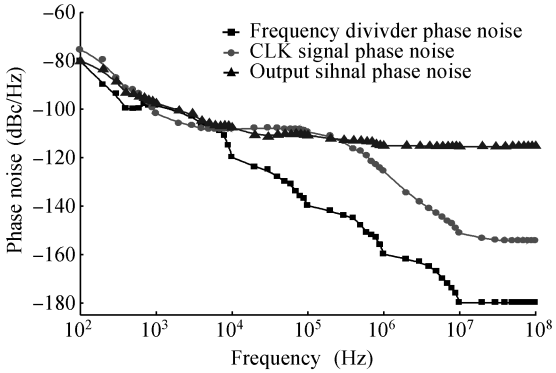


Fig. 8. Measured phase noise with 1.2-V-peak input signal at 10 GHz.

In practice, we cannot isolate PN_{tc} from PN_{fd}, thus, the result of the analysis contains PN_{tc} and PN_{fd}. On further analysis of the measured results of phase noise, the measured phase noise floor is equal to the sum of the essential phase noise floor replication. The essential floor phase noise is white noise and uncorrelated with frequency offset according to the analysis of part 4. Based on the analysis of Ref. [7], we can estimate the phase noise floor. From Fig. 7(a) and Eqs. (29)–(31), we can see the slope of the phase noise is approximately –20 dBc/dec and the frequency corner is nearby 10 MHz. Thus, we get Fig. 8 and Table 1. From Fig. 8, we can see the output signal phase

noise is 4.6 dB less than the clk signal phase noise at 100 Hz offset. The more the frequency offset increases, the larger the phase noise of the sampling effect is. Thus, the phase noise of the output signal begins to be larger than the phase noise of the CLK signal at 1 MHz offset nearby and the output signal phase noise reaches the floor phase noise at 1 MHz offset.

6. Conclusion

A modified frequency divider architecture employing a novel D latch is designed and realized. The D latch requires only a single clock signal and uses a switch transistor with dynamic loading to increase the bandwidth at low supply voltage. The frequency divider prototype achieves an operating frequency range of 50 MHz to 10 GHz at 1.2 V supply voltage using the IBM 90-nm CMOS process. The frequency divider consumes only a power of 9.12 mW. The phase noise of the frequency divider is –159.83 dBc/Hz at 1 MHz offset from the 5 GHz carrier. A useful analytical expression to accurately predict the bandwidth and phase noise is presented and validated by measurement. The design presents a viable solution to realize the high spectrum purity and wideband divider with low supply voltage. This technique is still not realized with the existing divider design. Compared with other recently published results using the 90-nm CMOS process, the designed frequency divider shows the best FOM[4], as shown in Table 2. The presented frequency divider is particularly suited for ultra wideband, low phase noise and low power applications.

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