A 2.4 GHz high-linearity low-phase-noise CMOS LC-VCO based on capacitance compensation

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Abstract: A 2.4 GHz high-linearity low-phase-noise cross-coupled CMOS LC voltage-controlled oscillator (VCO) is implemented in standard 0.18-μm CMOS technology. An equalization structure for tuning sensitivity base on the three-stage distributed biased switched-varactor bank and the differential switched-capacitor bank is adopted to reduce the variations of the VCO gain, achieve high linearity, and optimize the phase-noise performance. Compared to the conventional VCO, the proposed VCO has more constant gain over the entire tuning range. The tuning range is about 18.7% from 2.23 to 2.69 GHz, and the phase noise is –95 dBc/Hz at 100-kHz offset and –117 dBc/Hz at 1-MHz offset from the carrier frequency of 2.42 GHz. The power dissipation is 2.1 mW from a 1.8 V power supply. The active area of this VCO is 500×810 μm^2.

Key words: switched-capacitor; varactor; VCO; phase noise; tuning range; linearity
DOI: 10.1088/1674-4926/31/7/075005 **EEACC:** 1230B; 2570K

1. Introduction

The CMOS LC voltage-controlled oscillator (VCO) is one of the most important building blocks in the implementation of a single radio chip in today's various wireless communication systems. Recently, the features of wide tuning range and low phase noise have been in high demand in LC-VCO for realizing the multiband RF transceivers[1−3]. Combining digital and analog tuning is the most effective way to achieve simultaneously a wide tuning range and small VCO gain by using the switched-capacitor bank and varactor respectively[4].

However, the VCO gain ($K_{\rm VCO}$) of conventional structure is variable across the entire tuning range, which increases the noise sensitivity but is useful for widening the tuning range of the VCOs, and this essentially nonlinear characteristic will deteriorate the phase noise performance of VCO and phase-locked loop (PLL)[5, 6]. For this reason, it is desirable to minimize the variation of $K_{\rm VCO}$ across the entire tuning range. Different methods of gain compensation have been used to cope with the nonlinear characteristic and to achieve constant $K_{\rm VCO}$. In Refs. [5–8], the combined structures of switched-capacitor bank and varactor are adjusted to reduce the variation. However they need too much additional capacitor which dissipates large area resources, makes the automatic frequency calibration (AFC) of PLL too complex, or considers it isolatedly only from switched-capacitor bank or varactor. So, compared to the conventional structure, their methods would be limited in their effects.

In this paper, the limitation of the conventional VCO structure is discussed, and then, a novel equalization structure is proposed based on the distributed biased switched-varactor and the differential switched-capacitor bank. Finally, a CMOS LC-VCO adopting the proposed equalization structure is implemented to demonstrate the linear tuning and low phase noise characteristic.

2. AMOS varactor and phase noise

2.1. AMOS varactor

The accumulation MOS (AMOS) varactor has been a popular choice for VCO varactor, and has been employed in many VCO circuits[1−7]. The AMOS varactor has three modes of operation: accumulation, depletion, and inversion, and the capacitance of this device depend on the mode of operation[4]. According to the analysis in Ref. [9], we can describe a formula for $C_{\rm V}$ of the AMOS varactor as

$$C_{\rm V} = \frac{\oint i\,{\rm d}V}{\pi\omega_{\rm o}V_{\rm o}^2} = \frac{A}{\pi\omega_{\rm o}V_{\rm o}^2}, \tag{1}$$

where $C_{\rm V}$ is the equivalent capacitance of the varactor, ω_0 is the oscillation frequency, $V_{\rm o}$ is the output amplitude, i is the varactor current, V is the voltage across the varactor, A represents the area enclosed by the I–V curve.

The structure and operation of the AMOS capacitor is shown in Fig. 1(a), and the C–V characteristic is shown in Fig. 1(b). When the gate electrode is biased at the positive end, the AMOS is operated in the accumulation mode, the $C_{\rm V}$ represents $C_{\rm max}$. As the gate electrode becomes negative, a depletion region is formed, and the $C_{\rm V}$ represents $C_{\rm min}$.

The AMOS varactor has a wider tuning range and lower parasitic resistance, and the VCOs adopting the AMOS varactors demonstrate low power dissipation and low phase noise[8, 10]. The C–V characteristic of the AMOS varactor exhibits a good adjusting ratio ($C_{\rm max}/C_{\rm min}$). However, the C–V curve has a highly nonlinear characteristic, which means $K_{\rm var}$ is not constant across the tuning range, and the more the curve departs from linearity, the more it converts low frequency noise into phase noise[4].

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Received 28 November 2009, revised manuscript received 26 January 2010

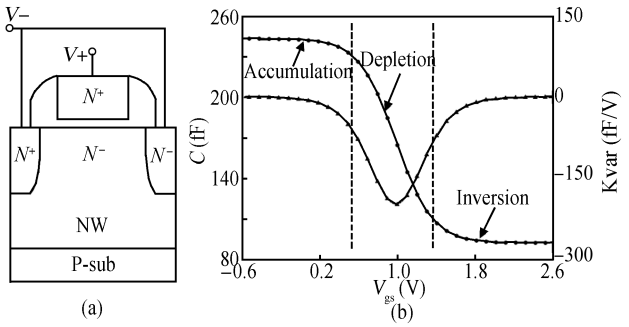

Fig. 1. AMOS varactor. (a) Structure and operation. (b) C–V characteristic.

2.2. Phase noise

The nonlinear characteristic complicates the phase noise analysis of VCO[11]. The sources of noise coming from several different frequencies make it difficult to discern which noises are the dominant ones. In the conventional Leeson's formula[12], phase noise is given by

$$L(f_{\rm m}) = 10\lg\left\{\frac{2FkT}{P_{\rm s}}\left[1+\left(\frac{f_0}{2Qf_{\rm m}}\right)^2\right]\left(1+\frac{f_{\rm c}}{f_{\rm m}}\right)\right\}, \tag{2}$$

where $f_{\rm o}$ is the carrier frequency, $f_{\rm m}$ is the offset frequency from $f_{\rm o}$, $f_{\rm c}$ is the flicker noise corner frequency, Q is the quality factor, $P_{\rm s}$ is the power dissipation, F is the noise factor, k is Boltzmann's constant, and T is the temperature.

AMOS varactor has a nonlinear C–V characteristic, namely $K_{\rm VCO}$ is not constant across the tuning curve. This feature can make the phase noise non-uniform over the tuning range. Any noise on the control line will modulate the carrier frequency and create additional phase noise[4]. Taking this additional noise mechanism into account, the Leeson's formula can be modified as:

$$L(f_{\rm m}, K_{\rm VCO}) = 10\lg\left\{\left(\frac{f_0}{2Qf_{\rm m}}\right)^2\left[\frac{FkT}{2P_{\rm s}}\left(1+\frac{f_{\rm c}}{f_{\rm m}}\right)\right] + \frac{1}{2}\left(\frac{K_{\rm VCO}V_{\rm m}}{2f_{\rm m}}\right)^2\right\}, \tag{3}$$

where $V_{\rm m}$ is total amplitude of all low frequency noise sources. Analyzed form above formula, large $K_{\rm VCO}$ will degrade the phase noise $L(f_{\rm m}, K_{\rm VCO})$[4, 13].

3. Linear frequency tuning

The typical schematic and tuning characteristic of conventional fully-integrated cross-coupled CMOS LC-VCO is shown in Fig. 2. Coarse and fine tuning is realized by setting a proper digital code to the switched capacitor bank and applying an analog voltage to the varactor respectively, and the digital and analog tuning sensitivities are defined as $K_{\rm CT}$ and $K_{\rm FT}$ respectively. To achieve linear tuning characteristic, we should reduce the variation of fine and coarse tuning sensitivity[5], which means to achieve constant $K_{\rm CT}$ and $K_{\rm FT}$.

According to the analysis in Ref. [8], we can obtain an equalized $K_{\rm var}$ by connecting several varactors in parallel and

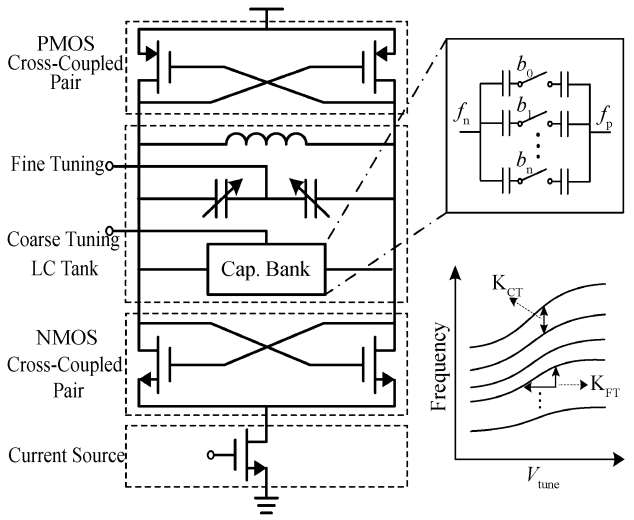

Fig. 2. Schematic and tuning characteristic of conventional CMOS LC-VCO.

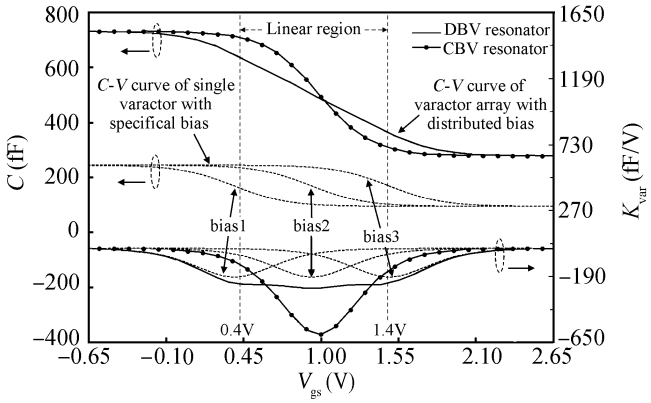

Fig. 3. Simulated C–V characteristic and $K_{\rm var}$.

to bias them with different DC biases. In this paper, a three-stage distributed biased varactor (DBV) resonator is analyzed compared to the conventional biased varactor (CBV) resonator which has the same total number of varactors. The simulated C–V characteristic and $K_{\rm var}$ are represented in Fig. 3, in which the linear part of single stage is merged together, so the $K_{\rm var}$ is approximately constant over the specified voltage control range (0.4–1.4 V).

It is well known that the oscillation frequency of LC VCO can be expressed by

$$f(V) = \frac{1}{2\pi\sqrt{LC_{\rm T}}}, \tag{4}$$

where L is the inductance, and $C_{\rm T}$ is the total capacitance of LC tank and can be described by the following equation,

$$C_{\rm T} = C_{\rm V} + C_{\rm B}, \tag{5}$$

where $C_{\rm V}$ is the capacitance of varactor, and $C_{\rm B}$ is the capacitance of the switched-capacitor bank and can be expressed by

$$C_{\rm B} = C_{\rm p} + \sum_{n=0}^{N} nC_{\rm u}, \tag{6}$$

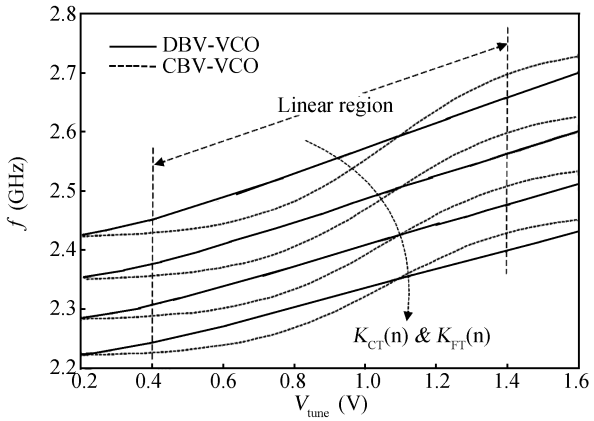

Fig. 4. Simulated f–V characteristic of different VCO structures.

where C_p is the parasitic capacitance, n is the digital code, and C_u is the unit capacitance of the switched-capacitor.

For the defect of high nonlinearity, the conventional CMOS LC-VCO, as shown in Fig. 2, is improved by using the distributed biased varactor resonator. As an example, we adopt the structure of the three-stage distributed biased varactor bank analyzed above for the fine tuning, and 2-bit digital controlled switched-capacitor bank for the coarse tuning. The simulated f–V characteristic of DBV-VCO and CBV-VCO is shown in Fig. 4.

As represented in Fig. 4, the linearity of every single tuning curve of DBV-VCO is improved largely compared to the CBV-VCO, and the curves can almost be seen as beelines, especially at the voltage ranged from 0.4 to 1.4 V, which just meet the requirement of our charge pump. However, the $K_{FT}(n)$ and $K_{CT}(n)$, defined by Eqs. (7) and (8), decreased when the digital code n is increased. The tuning sensitivities are variable across the entire tuning range, and according to Eq. (3), this nonlinearity characteristic will deteriorate the phase noise performance of the VCO and the PLL adopt this VCO[13].

$$K_{FT}(V,n) = \frac{\partial f(V,n)}{\partial V}, \quad 1 \leqslant n \leqslant 4 \tag{7}$$

$$K_{CT}(V,n) = f(n+1) - f(n)\,|_{V=V_x}, \quad 1 \leqslant n \leqslant 3 \tag{8}$$

where V is the tuning voltage, and V_x is a specified voltage in the range from 0.4 to 1.4 V.

By analyzing Eqs. (1) and (4), we can see that ΔV of the tuning voltage will result in ΔC of the varactor capacitance, and then causes ΔF of the tuning frequency, and the follow equation can be achieved.

$$\frac{\Delta f(V,n)}{\Delta C} = \frac{-1}{4\pi C_T \sqrt{LC_T}}. \tag{9}$$

Combining Eq. (9) with Eqs. (5) and (6), we can see if the digital code n increased, the total capacitor C_T of VCO LC tank will also increased correspondingly. Conventionally, the size of the varactor is unchanged during the tuning process, so the ΔC will be constant, and this will result in the decrease of Δf, which means the decrease of $K_{FT}(n)$. Such a large variation in $K_{FT}(n)$ will prevent keeping the PLL bandwidth constant for optimal phase noise performance[14].

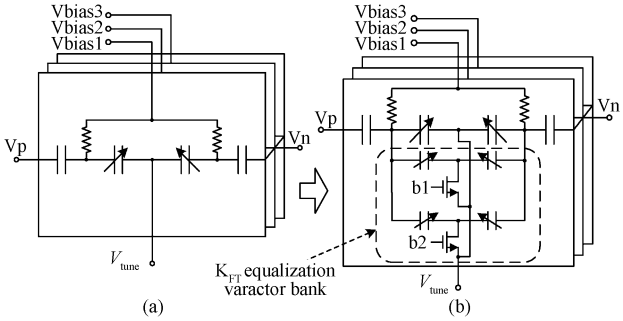

Fig. 5. Conventional DBV resonator. (b) Proposed equalization structure base on switched-varactor DBV resonator.

The solution proposed here is to change the size and structure of the varactor resonator to compensate the decrease of tuning sensitivity which caused by the variation of C_T. The proposed equalization structure is shown in Fig. 5. Based on the analyzed structure of the three-stage distributed biased varactor resonator, a number of unit varactors are added in the LC tank by switches controlled by the digital code n. At the lower frequency, the $K_{FT}(n)$ becomes lower, we set the digital code n to enable the relevant switches and the unit varactor will be connected in the varactor resonator to increase the size of varactor, which will add the ΔC of varactor resonator. By using this equalization structure, we can not only realize high linearity for single tuning curve, but also compensate the decrease of $K_{FT}(n)$, namely the $K_{FT}(n)$ will keep constant across the entire tuning range. The parasitics of the capacitors and transistors in the equalization structure and the process will worsen the effect of linearity, so careful simulation will be done to determine the accurate size of varactors and the value of biases.

The conventional structure of the switched-capacitor bank is a binary-weighted structure, as shown in Fig. 6(a). This structure can cause unacceptably large variations in the coarse tuning sensitivity $K_{CT}(n)$ across the entire tuning range[5], which has been described in Fig. 4, and this variation is not desirable for the VCO and PLL. In this paper, we apply the differential switched-capacitor bank in which the drain and source terminals of the switch are connected to the inverse gate voltage via a large resistance as shown in Fig. 6(b). The Q factor of this structure is given by Eq. (10), compared to the conventional structure, the Q factor of the differential switch will be doubled[15], and the phase noise of VCO is lower according to Eqs. (2) and (3).

$$Q = \frac{\mu_n C_{OX} W(V_{GS} - V_t)}{\omega_0 LC}. \tag{10}$$

According to Eq. (4), to obtain a linear coarse tuning characteristic, the total capacitance C_T of the LC tank must take an exponential form of n^{-2}, rather than a linear form of Eq. (6)[5]. In this paper, based on the structure of the differential switched-capacitor bank, a differential $K_{CT}(n)$ equalization capacitor bank is connected in the LC tank which is controlled by the digital code n, as shown in Fig. 6(b). By using this proposed structure, an additional ΔC is compensated to the C_T to make an approximately exponential form between C_T and f and so achieve a constant $K_{CT}(n)$.

Combining the equalization structures of the three-stage

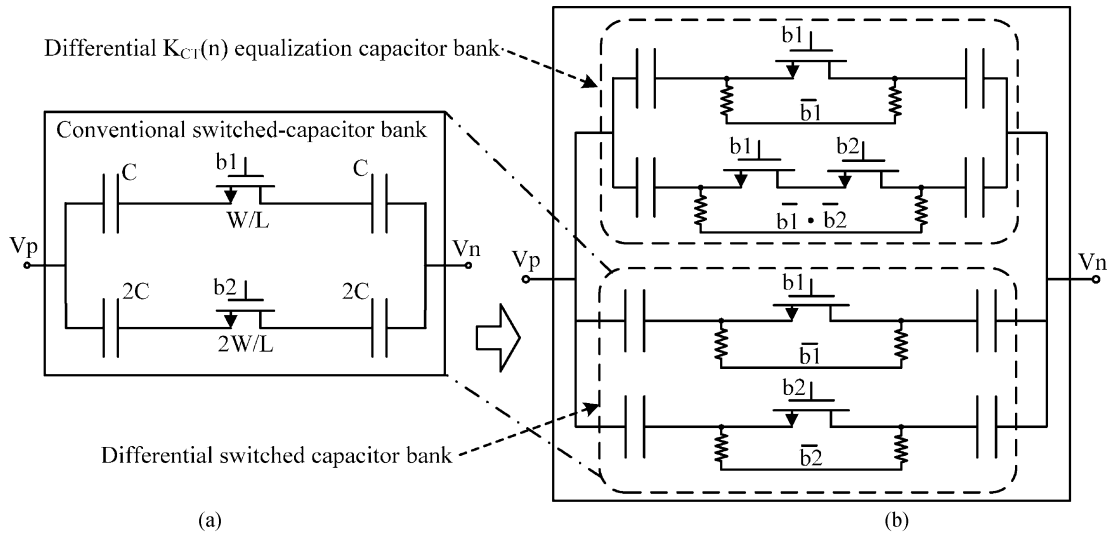

Fig. 6. (a) Conventional binary-weighted structure. (b) Proposed equalization structure base on differential switched-capacitor.

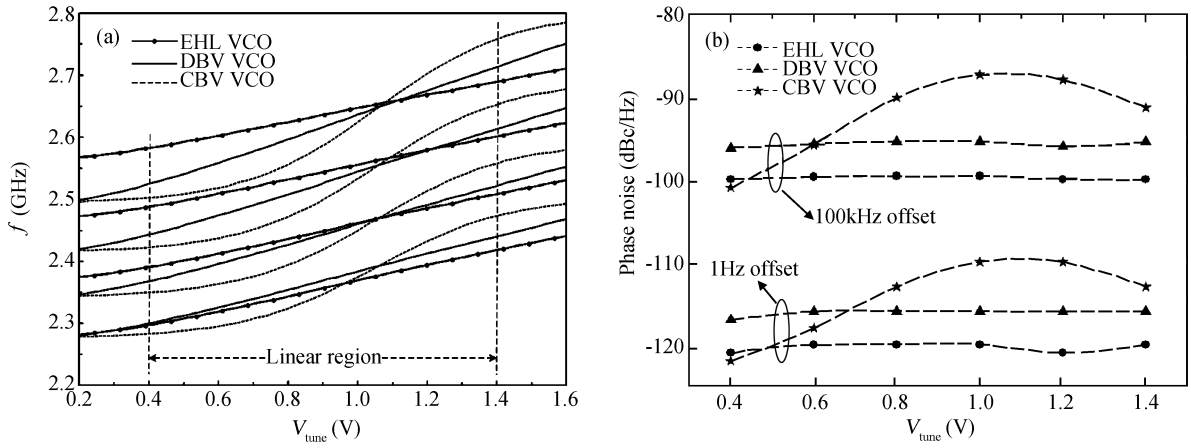

Fig. 7. Simulated results of different VCO structures. (a) f–V characteristic. (b) Phase noise.

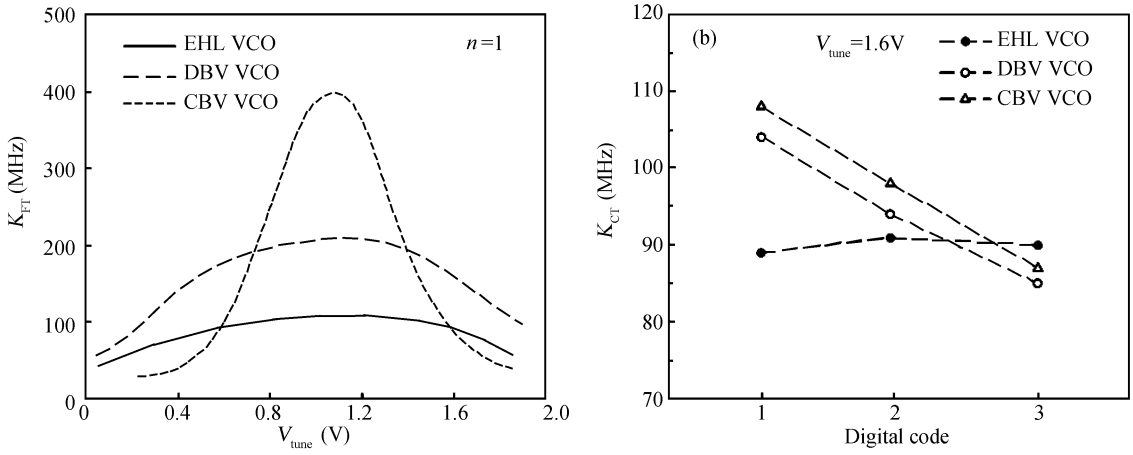

Fig. 8. Simulated tuning sensitivity. (a) $K_{FT}(n)$. (b) $K_{CT}(n)$.

distributed biased switched-varactor bank and the differential switched-capacitor bank proposed above, an equalized high linearity (EHL) VCO is realized. The simulated f–V characteristic, phase noise performance, and tuning sensitivity of EHL-VCO compared to the CBV-VCO and DBV-VCO are shown in Figs. 7 and 8, illustrate the differences between these structures. The phase noise is simulated versus the frequency offset at the top of the tuning range by setting the digital code

Table 1. VCO simulation summary.

Parameter	Tuning range at 0.2–1.6 V (MHz)	Bandwidth (%)	K_{FT} variation at 0.4–1.4 V (%)	K_{CT} variation (%)	Phase noise (b0 = 0, b1 = 0; V_{tune} = 0.9 V) (dBc/Hz)		
					@ 10 kHz	@ 100 kHz	@ 1 MHz
EHL-VCO	2280−2712	17.3	121	102	79	99.6	120
DBV-VCO	2279−2745	18.6	134	122	74.8	95.4	116
CBV-VCO	2278−2780	19.8	667	124	66.6	87.3	110

n to the minimum value.

As shown in the above figures, it is clear that the f–V characteristic of EHL-VCO has perfect linearity, and based on the contribution of $K_{FT}(n)$ and $K_{CT}(n)$, the unitary tuning sensitivity of the VCO will remain constant over the entire tuning range with the tiny decrease of tuning range. This feature will improve the phase noise performance of the VCO and the PLL adopting the VCO. The addition of switch transistors in switched-varactor bank will affect the phase noise performance of VCO in theory, but it is far less than the contribution made by the proposed equalization structure, so the phase noise performance of the VCO will be improved ultimately. This proposed equalization structure dissipates some area resources, but compared to the other methods[5−8], the proposed structure has less area dissipation, an effective adjust process and better effect.

4. Circuit design and measurements

Based on the core structure shown in Fig. 2, and integrating the equalization structures proposed above, a high linear VCO is designed for an RF receiver. It is an LC differential cross-coupled VCO with nMOS and pMOS latch, which generate negative resistance to cancel losses in the LC-tank. The current source I_{dc} draws 0.8 mA from a 1.8 V power supply. The simulation results of EHL-VCO, DBV-VCO, and CBV-VCO are summarized in Table 1, in which the bandwidth and gain variation can be defined by $2(f_{max} - f_{min})/(f_{max} + f_{min})$ and K_{max}/K_{min} respectively[5].

This proposed high linearity VCO is integrated in an RF frequency synthesizer which is fabricated in a standard 0.18 μm CMOS technology. In our synthesizer, the VCO outputs is divided by a 2:1 quadrature frequency divider to generate 1.2 GHz quadrature local oscillating (LO) signal for a quadrature downconversion RF receiver. An output buffer amplifier which is directly driven by the frequency divider outputs is adopted in our synthesizer for testing. Figure 9 shows the micrograph of the VCO; its active area is 500×810 μm^2. The RF synthesizer chip is tested on a printed circuit board. An Agilent E4440A spectrum analyzer is used to measure the synthesizer parameters. The f–V tuning characteristic of the VCO is shown in Fig. 10, in which the frequency tuning range is 18.7 %, from 2.23 to 2.69 GHz. It is clear that the oscillation frequency is fairly linear over the entire voltage range, especially between 0.4 and 1.4 V, which just meets the requirement of the charge pump in our synthesizer.

The output spectrum of LO signal is given in Fig. 11. Figure 12 shows the phase noise measured at the middle of the tuning range of the LO signal, and the measured results are –101 dBc/Hz at 100-kHz offset and –123 dBc/Hz at 1-MHz offset. The phase noise at lower frequency is better than the result at higher frequency. According to analysis, the phase noise of VCO is higher than LO's about 6 dBc/Hz, which means the

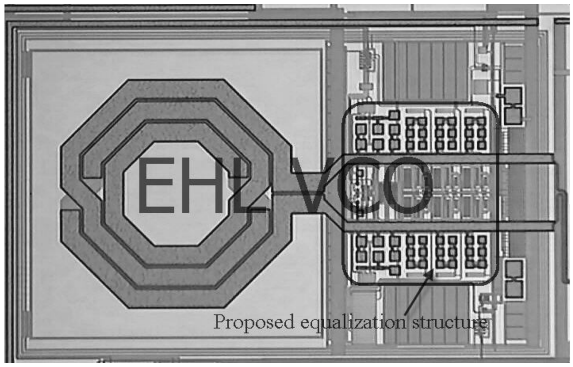

Fig. 9. Micrograph of proposed VCO.

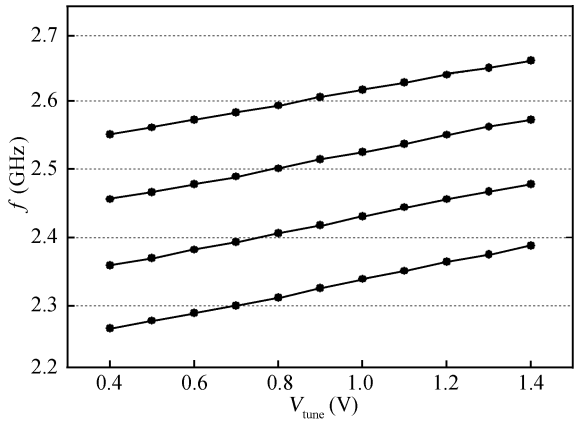

Fig. 10. Measured tuning characteristic of the VCO.

phase noise of VCO are about −95 dBc/Hz at 100-kHz offset and –117 dBc/Hz at 1-MHz offset.

A widely used figure-of-merit (FOM) [14,15] to make a fair comparison between different VCOs are defined as

$$\mathrm{FOM} = L(\Delta f) - 20\lg\frac{f_0}{\Delta f} + 10\lg\frac{P_{dc}}{1\ \mathrm{mW}}, \qquad (11)$$

where $L(\Delta f)$ is the measured phase noise at the frequency offset Δf from the carrier at f_0, and P_{dc} is the measured dc power dissipation in mW. The FOM in this design is –181.5 dBc/Hz. The performances of the proposed EHL-VCO are compared with other recently published CMOS LC VCOs in Table 2.

Based on the above experimental results, we can say that the proposed equalization topology reduces the variation of unitary tuning sensitivity remarkably when compared to the conventional frequency tuning. Therefore, it relaxes the requirements for the other integrated components and their calibration in order to meet the requirements of the PLL. The bandwidth can be expanded easily by adding to the number of switched-capacitors.

Table 2. Comparison with other VCOs.

Parameter	Ref. [5]	Ref. [14]	Ref. [16]	Ref. [17]	This work
Technology	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS
Frequency (GHz)	1.752	3.1	5.24	1.8	2.42
Tuning range (GHz)	0.924–1.85	3.1–5.2	5.15–5.35	1.67–1.93	2.23–2.69
Bandwidth (%)	66.7	50	3.8	14.4	18.7
PN (dBc/Hz)	–127.1 @ 1 MHz	–119 @ 1 MHz	–104 @ 1 MHz	–138 @ 3 MHz	–117 @ 1 MHz
FOM (dBc/Hz)	–181.6	–179.3	–165.8	–181	–181.5
PDC (mW)	10.8	9.2	18	18	2.1
Supply voltage (V)	1.8	1.2	1.8	1.2	1.8

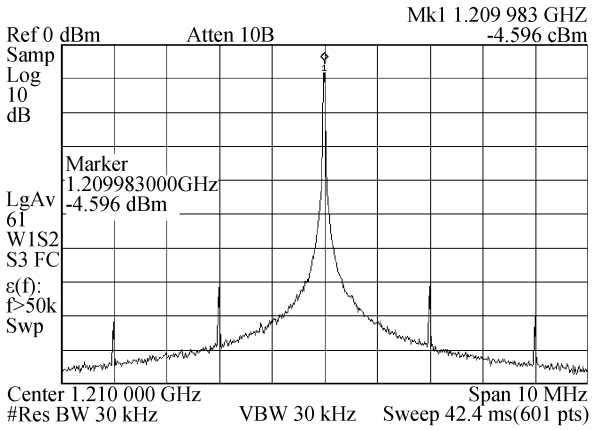

Fig. 11. Measured LO output spectrum.

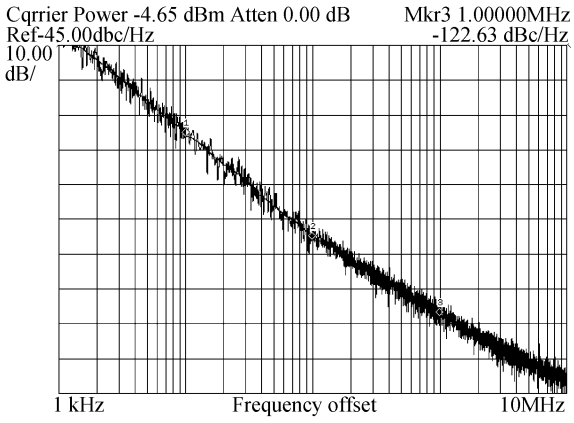

Fig. 12. Measured LO output phase noise at 1-MHz offset.

5. Conclusion

The variation of VCO gain over the entire tuning range and the significant impact of VCO gain on phase noise have been studied, and a high linearity CMOS LC-VCO employing novel equalization structures of three-stage distributed biased switched-varactor bank and differential switched-capacitor bank is demonstrated. Compared to the conventional VCO, the proposed VCO remarkably reduced the variations of tuning sensitivity and optimized the phase noise performance across the entire tuning range. The EHL-VCO was fabricated in 0.18 μm standard CMOS technology, achieving a tuning range of 2.23–2.69 GHz, and phase noise is –95 dBc/Hz at 100-kHz offset and –117 dBc/Hz at 1-MHz offset for 2.42 GHz output frequency. The power dissipation is 2.1 mW from a 1.8 V power supply.

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