Hot carrier effects of SOI NMOS*

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Abstract: Hot carrier effect (HCE) is studied on annular NMOS and two-edged NMOS such as H-shape gate NMOS, T-shape gate NMOS and common two-edged NMOS. Based on the chemical reaction equation of HCE degradation and a geometry dependent reaction diffusion equation, a HCE degradation model for annular NMOS and two-edged NMOS is proposed. According to this model, we conclude that the time exponent of the threshold voltage degradation depends on the configuration of the gate, and annular NMOS has more serious HCE degradation than two-edged NMOS. The design, fabrication and HCE experiments of these NMOS in a 0.5-μm PD SOI process verify the correctness of the conclusion.

Key words: annular NMOS; two-edged NMOS; hot carrier effects; reaction diffusion model
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1. Introduction

For devices that need to operate for a very long time in space radiation environments, long term reliability issues such as negative bias temperature instability (NBTI) and hot carrier effect (HCE) should be considered in addition to radiation inducing long term degradation such as total ionizing dose effect (TID). Besides TID[1−3], NBTI and HCE are also very important reasons for long term degradation of the devices[4−6].

Since common two-edged NMOS is sensitive to TID, annular NMOS and special two-edged NMOS such as H-shape gate NMOS and T-shape gate NMOS are commonly used in radiation environment due to their high resistance against TID. However, in bulk silicon process, the experimental results produced by Silvestri *et al.* have shown that[7, 8]: annular NMOS have more serious HCE degradation than common two-edged NMOS, and that the time exponent (n) is 0.65 for annular NMOS but only 0.5 for common two-edged NMOS in their experiments, thus the implication is annular NMOS may have shorter lifecycle than that of our expectation because of our ignorance about its worse HCE degradation.

In the SOI process, whether annular NMOS have more serious HCE degradation is still not verified in the experiments; at the same time, the special two-edged NMOS such as H-shape gate NMOS and T-shape gate NMOS are also other important TID hardened NMOS in the SOI process, whether these NMOS have more serious HCE degradation is also not clear, so it's very important to widely investigate HCE of various TID hardened NMOS to exactly expect the lifetime of them.

2. Theoretical model

In MOSFETs, a portion of channel carriers receiving enough energy can overcome the surface barrier and inject into the oxide layer, a fraction of the injected hot carriers can be trapped by oxide traps and become the surplus charges, and interface states occur at the Si/SiO_2 interface in this process, then V_t and other important electrical parameters gradually degrade over time.

Silicon dangling bond ($\equiv$ Si$\bullet$) at the Si/SiO_2 interface is one of the primary interface states which comes from the chemical reaction between silicon hydrogen bond (Si–H) and positive hydrogen (H^+), and the chemical reaction equation is as follows[4]:

$$\mathrm{Si_3 \equiv Si\text{–}H + H^+ + e^- \rightarrow [Si_3 \equiv Si\bullet] + H_2}. \quad (1)$$

And some scholars have also further proposed the other chemical reaction equation[9]:

$$\mathrm{Si_3 \equiv Si\text{–}H + H^+ \rightarrow [Si_3 \equiv Si\bullet] + H_2}, \quad (2)$$

which is more likely to be the main HCE degradation mechanism when NMOS work under normal operating voltage[9]. H_2 produced from the chemical reaction will diffuse into the oxide.

Based on Eq. (1) or Eq. (2), and according to a novel reaction diffusion equation[5, 10], we propose that the generation rate of N_{it} follows the formula:

$$\frac{\mathrm{d}N_{it}}{\mathrm{d}t} = k_f[N_0 - N_{it}]N_{H^+} - k_r N_{it} N_{H_2}^{(0)}. \quad (3)$$

Here, k_f and k_r are the forward and reverse reaction rate of Eq. (1) or Eq. (2), N_0 is the maximum density of available Si–H bonds, $N_{H_2}^{(0)}$ is H_2 density at the Si/SiO_2 interface, N_{H^+} is H^+ density at the Si/SiO_2 interface. The interface states generation process is a competing process between Si–H breaking and passivation. Since the rate of H_2 generating from the chemical reaction is far greater than the rate of H_2 diffusing into the oxide[5], the diffusion rate determines the generation rate and further determines the chemical reaction rate and the generation rate of N_{it}.

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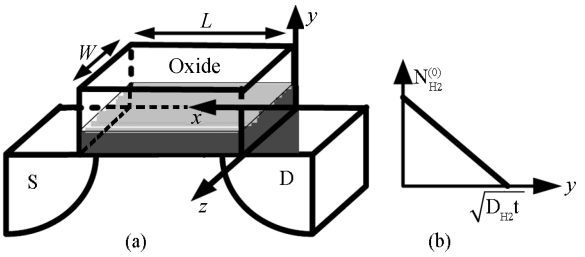

Fig. 1. Hydrogen diffusion in the interface of the gate. (a) Diffusion region. (b) H_2 density profile.

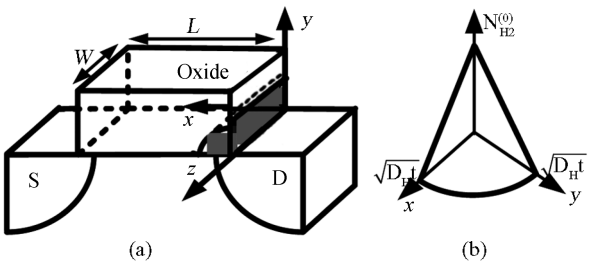

Fig. 2. Hydrogen diffusion in the edge of the gate. (a) Diffusion region. (b) H_2 density profile.

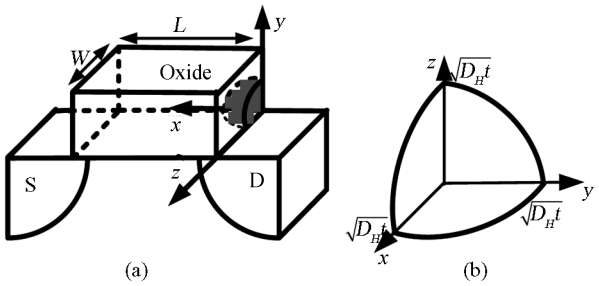

Fig. 3. Hydrogen diffusion in the corner of the gate. (a) Diffusion region. (b) H_2 density profile.

Meanwhile, H_2 diffusion rate follows the diffusion equation:

$$\frac{\mathrm{d}N_{\mathrm{H}_2}}{\mathrm{d}t} = D_{\mathrm{H}_2}\left(\frac{\partial^2 N_{\mathrm{H}_2}}{\partial x^2} + \frac{\partial^2 N_{\mathrm{H}_2}}{\partial y^2} + \frac{\partial^2 N_{\mathrm{H}_2}}{\partial z^2}\right). \tag{4}$$

Here, D_{H2} is the diffusion coefficient of H_2. From Eq. (4), the diffusion rate of H_2 depends on the geometry of the diffusion region, and the diffusion region can be divided into 1-, 2-, 3-dimensional diffusion region, as shown in Figs. 1(a), 2(a), 3(a) respectively.

From Refs. [5, 10], in 1-dimensional region, along with y axis, H_2 density profile can be approximated in Fig. 1(b). Since every two interface states correspond to one H_2, the total amount of generated interface states is two times more than the total amount of generated H_2. The total amount of H_2 can be obtained by quadraturing the curve in Fig. 1(b). So, assume the degraded interface area is A, then:

$$\begin{aligned} N_{\mathrm{it}}(t) &= 2\times\frac{1}{A}\int_0^{\sqrt{D_{\mathrm{H}_2}t}} AN_{\mathrm{H}_2}(y,t)\,\mathrm{d}y \\ &= \frac{2}{A}\int_0^{\sqrt{D_{\mathrm{H}_2}t}} AN^{(0)}_{\mathrm{H}_2}\left(1-\frac{y}{\sqrt{D_{\mathrm{H}_2}t}}\right)\mathrm{d}y \\ &= N^{(0)}_{\mathrm{H}_2}\sqrt{D_{\mathrm{H}_2}t}. \end{aligned} \tag{5}$$

Similarly, in 2-dimensional region, H_2 density profile can be approximated in Fig. 2(b), assume the gate width is W, degraded interface area is B, then:

$$\begin{aligned} N_{\mathrm{it}}(t) &= \frac{2}{B}\int_0^{\sqrt{D_{\mathrm{H}_2}t}} \frac{1}{4}WN^{(0)}_{\mathrm{H}_2}\left(1-\frac{r}{\sqrt{D_{\mathrm{H}_2}t}}\right)2\pi r\,\mathrm{d}r. \\ &= \frac{W\pi}{6B}N^{(0)}_{\mathrm{H}_2}D_{\mathrm{H}_2}t. \end{aligned} \tag{6}$$

In 3-dimensional region, H_2 density can be approximated by Fig. 3(b), assume degraded interface area is C, then:

$$\begin{aligned} N_{\mathrm{it}}(t) &= \frac{2}{C}\int_0^{\sqrt{D_{\mathrm{H}_2}t}} \frac{1}{8}N^{(0)}_{\mathrm{H}_2}\left(1-\frac{r}{\sqrt{D_{\mathrm{H}_2}t}}\right)4\pi r^2\mathrm{d}r. \\ &= \frac{\pi}{12C}N^{(0)}_{\mathrm{H}_2}(D_{\mathrm{H}_2}t)^{1.5}. \end{aligned} \tag{7}$$

Similar to Ref. [5], assume a relatively slow generation rate of interface state under steady state condition, then $\frac{\mathrm{d}N_{\mathrm{it}}}{\mathrm{d}t} = K$ (constant), and assume H^+ with a sufficient stable quantity at the Si/SiO_2 interface, then $N_{\mathrm{H}^+} = M$(constant), and $N_{\mathrm{it}} \ll N_0$, so Equation (3) can be simplified as:

$$K = k_{\mathrm{f}}MN_0 - k_{\mathrm{r}}N_{\mathrm{it}}N^{(0)}_{\mathrm{H}_2}. \tag{8}$$

According to Eq. (5), $N^{(0)}_{\mathrm{H}_2} = N_{\mathrm{it}}(t)\sqrt{D_{\mathrm{H}_2}t}$, and introduce into Eq. (8), then:

$$N_{\mathrm{it}}(t) = \sqrt{\frac{k_{\mathrm{f}}MN_0 - K}{k_{\mathrm{r}}}}(D_{\mathrm{H}_2}t)^{0.25} = at^{0.25}. \tag{9}$$

Similarly according to Eqs. (6)–(8), then:

$$N_{\mathrm{it}}(t) = \sqrt{\frac{W\pi(k_{\mathrm{f}}MN_0 - K)}{6Bk_{\mathrm{r}}}}(D_{\mathrm{H}_2}t)^{0.5} = bt^{0.5}, \tag{10}$$

$$N_{\mathrm{it}}(t) = \sqrt{\frac{\pi(k_{\mathrm{f}}MN_0 - K)}{12Ck_{\mathrm{r}}}}(D_{\mathrm{H}_2}t)^{0.75} = ct^{0.75}. \tag{11}$$

So, from Eqs. (9)–(11), the generation rate of N_{it} follows a power law of stress time and the time exponent (n) are 0.25, 0.5 and 0.75 for 1-, 2-, 3-dimensional HCE degradation respectively.

Furthermore, ΔV_{t} is proportional to ΔN_{it}[11]:

$$\Delta V_{\mathrm{t}} = \left(\frac{KI_{\mathrm{ds}}L_{\mathrm{eff}}}{\mu_0 W_{\mathrm{eff}}C_{\mathrm{ox}}V_{\mathrm{ds}}} + \frac{q}{C_{\mathrm{ox}}}\right)\Delta N_{\mathrm{it}}. \tag{12}$$

So, the degradation of V_{t} follows a power law of stress time, that is:

$$\Delta V_{\mathrm{t}} = A(t_{\mathrm{stress}})^n. \tag{13}$$

And the time exponent (n) are 0.25, 0.5 and 0.75, for 1-, 2-, 3-dimensional HCE degradation respectively.

HCE degradation mainly occurs near the drain side, as shown in the shaded area in Fig. 4, for two-edged NMOS

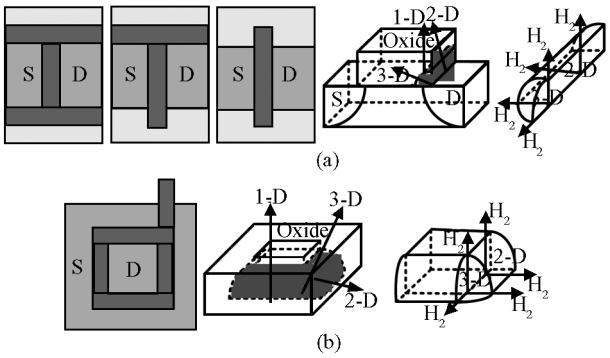

Fig. 4. Hydrogen diffusion region. (a) In different 2-edged NMOS. (b) In annular NMOS.

such as H-shape gate NMOS, T-shape gate NMOS and common two-edged NMOS, as shown in Fig. 4(a), H_2 follows 3-dimensional diffusion in the corner of the gate, 2-dimensional diffusion in the edge of the gate, and 1-dimensional diffusion in other degraded region; for annular NMOS, as shown in Fig. 4(b), H_2 follows 3-dimensional diffusion in four corners of the gate, 2-dimensional diffusion in the edge of the gate, and 1-dimensional diffusion in other degraded regions. Since 3-dimensional diffusion is the fastest and annular NMOS own significantly greater 3-dimensional diffusion regions than 2-edged NMOS, annular NMOS have more serious HCE degradation and the time exponent (n) is larger than 2-edged NMOS.

3. Experimental verification

3.1. Experimental set and test devices

HCE tests are usually carried out under three kinds of bias stress conditions[13, 14], including: high gate voltage stress condition ($V_{gs} \approx V_{ds}$), middle gate voltage stress condition ($V_{gs} \approx V_{ds}/2$) and low gate voltage stress condition ($V_{gs} \approx V_{ds}/4$). In the tests, source and substrate are held at ground potential, then gate and drain are both biased under corresponding voltage, and V_{ds} is typically above normal operating voltage (V_{dd}) to speed up the tests. In our experiments, V_{ds} is 1.6 times than V_{dd}, that is, $V_{ds} = 8$ V, then $V_{gs} = 8$, $V_{gs} = 4$, $V_{gs} = 2$ V for high, middle and low stress conditions respectively. Tests are carried out at room temperature and Agilent-4156C precision semiconductor parameter analyzer is used for the tests. During the tests, we periodically interrupt the stress, to measure I_{ds}–V_{gs} and I_{ds}–V_{ds} curves, which are used to extract the main electrical parameters, including I_{sat}, transconductance, V_t, etc. The passivation of the stress-induced defects during the measurement period may affect the accuracy of the tests; we use the automatic mothod to control the test process with the purpose to decrease the switch time. This method agrees with the one used in Refs. [7, 8].

NMOS used in our experiments were manufactured by a domestic foundry in a 0.5-μm PD SOI process. The gate oxide thickness (T_{ox}) is 12.5 nm, channel doping concentration (N_{ch}) is 4.0329000×10^{12} cm^{-3}, source/drain junction depth (X_j) is 100 nm, $V_{th0} = -0.929208$ V. All NMOS used the body tied technology to suppress the impact of floating body effects. The layouts of NMOS used in the experiments are shown in Fig. 5.

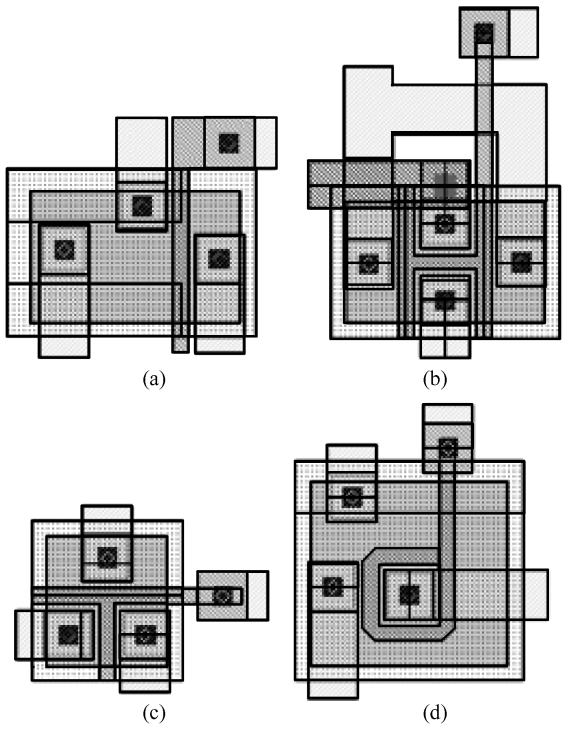

Fig. 5. Layout of the devices with body tied. (a) Common 2-edged NMOS. (b) H-shape gate NMOS (c) T-shape gate NMOS. (d) Annular NMOS.

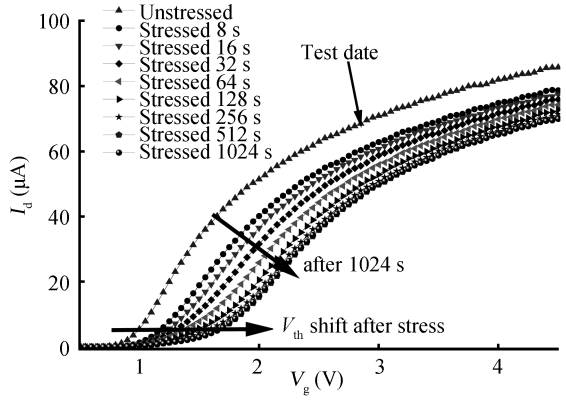

Fig. 6. Linear region (V_{ds} = 50 mV) I_{ds}–V_{gs} curves at different stress times.

3.2. Experimental results and results analysis

3.2.1. HCE degradation for annular NMOS and common two-edged NMOS

Figure 6 shows the linear region (V_{ds} = 50 mV) I_{ds}–V_{gs} curves of annular NMOS ($L = 0.5$ μm, $W = 9.4$ μm) at different stress time. The curves positively drift with the stress time, and V_t also positively drifts; when the stress time is up to 512 s, the degradation reaches saturation.

Under middle gate voltage stress conditions, in order to verify whether the annular NMOS has more serious HCE, we extract ΔV_t for common two-edged NMOS and annular NMOS at different stress times from the linear region ($V_{ds} = 50$ mV) I_{ds}–V_{gs} curves by using parabolic interpolation to find the gate bias at which the maximum transconductance occurs, then we

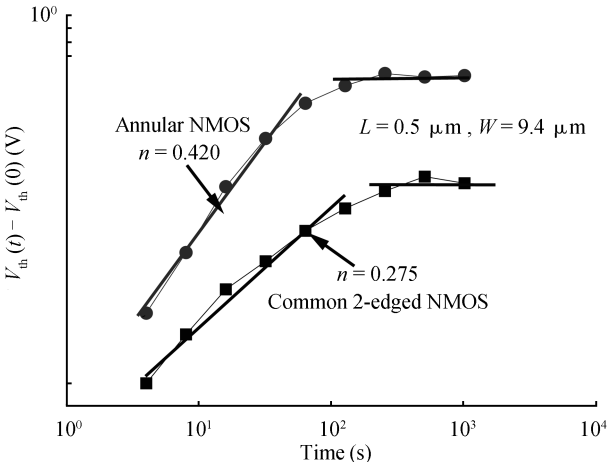

Fig. 7. Degradation of V_t between annular NMOS and common two-edged NMOS under middle gate voltage stress.

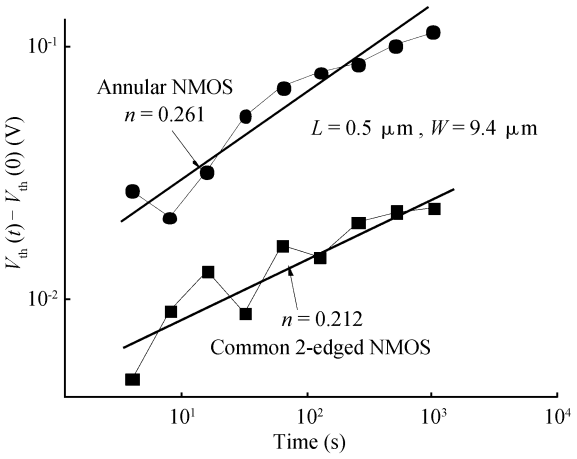

Fig. 8. Degradation of V_t between annular NMOS and common two-edged NMOS under high gate voltage stress.

fit the data in Matlab based on Eq. (11). As shown in Fig. 7, the time exponent (n) of common 2-edged NMOS is 0.275, but the time exponent (n) of annular NMOS is 0.420, which significantly increased by 52.7%, and the absolute value of ΔV_t of annular NMOS is far greater. Annular NMOS has more serious HCE degradation than two-edged NMOS under middle gate voltage stress conditions.

Under high gate voltage stress conditions, we use the same method to extract ΔV_t for both the two NMOS at different stress times. Test results are shown in Fig. 8; the time exponent (n) of common two-edged NMOS is 0.212, but the time exponent (n) of annular NMOS is 0.261, which significantly increased by 23.1%, and the absolute value of ΔV_t is also far greater. Annular NMOS also has more serious HCE degradation than two-edged NMOS under high gate voltage stress conditions.

As shown in Figs. 7 and 8, the experiments basically verify the theoretical prediction. Annular NMOS has more serious HCE degradation and the time exponent (n) is larger than two-edged NMOS.

Under low gate voltage stress conditions, as shown in Fig. 9, the results show a little difference, V_t degradation of annular NMOS rapidly reaches saturation, and V_t degradation of common two-edged NMOS after a brief rise also soon reaches saturation. The absolute value of ΔV_t of annular NMOS is also far greater than common 2-edged NMOS. Annular NMOS also has more serious HCE degradation than two-edged NMOS under low gate voltage stress conditions.

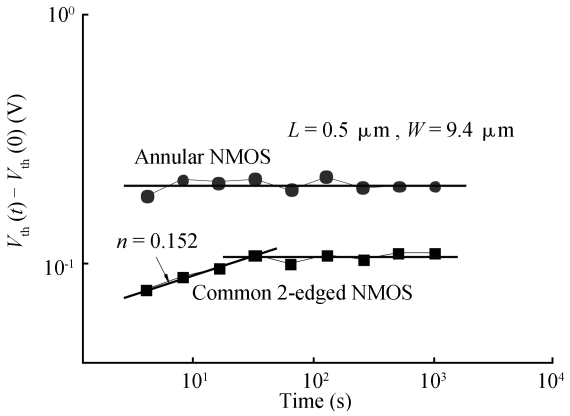

Fig. 9. Degradation of V_t between annular NMOS and common two-edged NMOS under low gate voltage stress.

As shown in Fig. 9, the time exponent (n) of annular NMOS is not larger than two-edged NMOS and the degradation quickly reaches saturation. This is a little inconsistent with our model. But our model is based on the assumption that the generation rate of H_2 from the chemical reaction is far greater than the diffusion rate of H_2, so the diffusion rate of H_2 determines the chemical reaction rate and then further determines the generation rate of N_{it}. However, under low gate voltage stress, the hot carriers injecting into oxide were relatively small which can produce relatively small H^+ in the oxide. Then due to the low gate voltage, vertical electric field favors to prevent H^+ from reaching the interface to participate in the chemical reaction, so less than the enough amount of H^+ becomes the major factor to make the chemical reaction can't continue, thus the degradation of V_t reaches saturation quickly.

3.2.2. HCE degradation for H-shape gate, T-shape gate NMOS and common two-edged NMOS

In our model, not only special two-edged NMOS but also common two-edged NMOS should have the same time exponent (n) because of the same configuration of the gate. We use the same method to extract ΔV_t for H-shape gate NMOS, T-shape gate NMOS and common two-edged NMOS ($L = 0.5$ μm, $W = 2.0$ μm) at different stress time and under middle gate voltage stress condition. The results are shown in Fig. 10, the time-exponent (n) of these three NMOS is almost the same, the fitting results in Matlab are as follows: $n = 0.335$, $n = 0.342$, $n = 0.356$, and H-shape gate NMOS and T-shape gate NMOS have weaker HCE degradation than common two-edged NMOS. Test results agree with the theoretical prediction.

3.2.3. HCE degradation for common two-edged NMOS with different gate widths

In our model, as shown in Fig. 4(a), if two-edged NMOS has the same gate length (L) but different gate widths (W), their 3-dimensional diffusion region will remain unchanged,

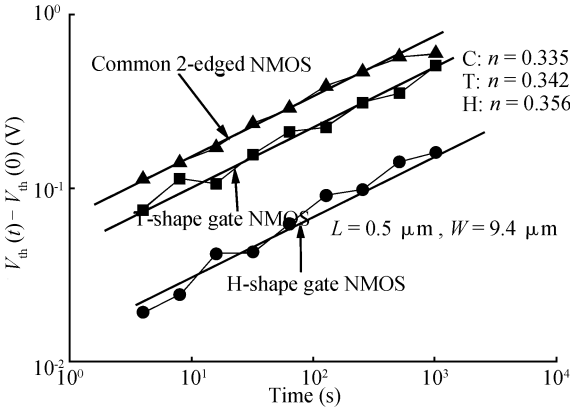

Fig. 10. Degradation of V_t between H-shape gate NMOS, T-shape gate NMOS and common two-edged NMOS.

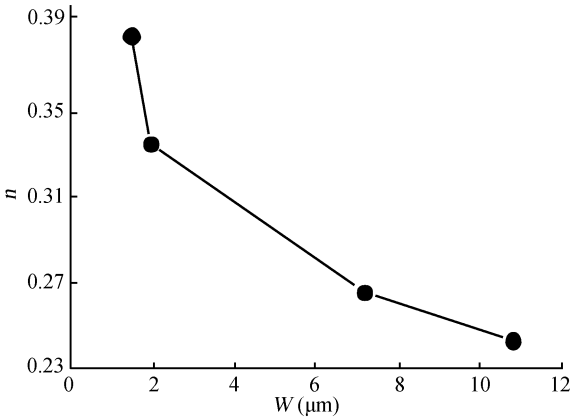

Fig. 11. Time-exponent (n) of V_t degradation for different gate width of common two-edged NMOS.

but 1-, 2-dimensional diffusion region will decrease with W decreasing. Since the proportion of 3-dimensional diffusion region increases and 3-dimensional diffusion is the fastest, the time-exponent (n) of V_t degradation will increase with W decreasing for 2-edged NMOS.

We have further tested and extracted the time-exponent (n) for four common 2-edged NMOS with $L = 0.5$ μm, $W = 1.5$ μm, 2.0 μm, 9.4 μm and 10.8 μm respectively. The results are shown in Fig. 11. The time-exponent (n) are as follows: $n = 0.386$, 0.335, 0.266, and 0.243 respectively. Test results are consistent with the theoretical prediction.

4. Conclusion

In this paper, HCE was studied on annular NMOS and two-edged NMOS such as H-shape gate NMOS, T-shape gate NMOS and common two-edged NMOS in a 0.5-μm PD SOI process. Compared with common 2-edged NMOS, annular NMOS has more serious HCE degradation, the time-exponent (n) of V_t degradation increased by 52.7% under middle gate voltage stress condition, and increased by 23.1% under high gate voltage stress condition, the absolute value of ΔV_t of annular NMOS is also far greater than common 2-edged NMOS under three different stress conditions; while special two-edged NMOS such as H-shape gate NMOS and T-shape gate NMOS have weaker HCE degradation than common two-edged NMOS, and almost have the same time-exponent (n) with common two-edged NMOS. Based on the chemical reaction equation of HCE degradation and a geometry dependent reaction diffusion equation, the HCE degradation model for annular NMOS and two-edged NMOS is established. The experimental results verified the correctness of this model.

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