A monolithic 3.1–4.8 GHz MB-OFDM UWB transceiver in 0.18-μm CMOS*

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Abstract: A monolithic RF transceiver for an MB-OFDM UWB system in 3.1–4.8 GHz is presented. The transceiver adopts direct-conversion architecture and integrates all building blocks including a gain controllable wideband LNA, a I/Q merged quadrature mixer, a fifth-order Gm–C bi-quad Chebyshev LPF/VGA, a fast-settling frequency synthesizer with a poly-phase filter, a linear broadband up-conversion quadrature modulator, an active D2S converter and a variable-gain power amplifier. The ESD protected transceiver is fabricated in Jazz Semiconductor's 0.18-μm RF CMOS with an area of 6.1 mm^2 and draws a total current of 221 mA from 1.8-V supply. The receiver achieves a maximum voltage gain of 68 dB with a control range of 42 dB in 6 dB/step, noise figures of 5.5–8.8 dB for three sub-bands, and an in-band/out-band IIP_3 better than -4 dBm/+9 dBm. The transmitter achieves an output power ranging from -10.7 to -3 dBm with gain control, an output P_{1dB} better than -7.7 dBm, a sideband rejection about 32.4 dBc, and LO suppression of 31.1 dBc. The hopping time among sub-bands is less than 2.05 ns.

Key words: MB-OFDM; UWB; transceiver; receiver; transmitter; synthesizer
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1. Introduction

Ultra wide-band (UWB) technology is used for short-range high-speed wireless interconnection systems due to its data rate up to 480 Mbps within 2–10 meters[1−3]. According to Federal Communication Committee (FCC) in the USA, the allocated frequency spectrum is 3.1–10.6 GHz. The spectrum shape of the modulated output and maximum power level are limited to -41.3 dBm/MHz to ensure that the UWB system is co-existent with existing spectrum users like GSM, WLAN and Bluetooth. WiMedia has proposed a standard based on a multi-band orthogonal frequency division multiplexing (MB-OFDM) approach[4]. The UWB frequency spectrum is divided into 14 sub-bands, each with a bandwidth of 528 MHz. The frequency-hopping among 14 sub-bands is combined with OFDM modulation. Thus, the multi-path effect and narrow-band interferences are eased in achieving high data-rate. The first three sub-bands from 3168 to 4752 MHz are denoted band #1, which is mandatory.

From FCC, a key requirement for a UWB transmitter is that the spectral density is limited to -41.25 dBm/MHz over a bandwidth of 528 MHz. Accounting for the power loss in the front-end, antenna and band pass filter, the required output power is about -7 dBm[4,5], which is feasible with an integrated CMOS power amplifier (PA). Another key issue for the performance is the input stage of the receive path featuring a wideband low noise-figure (NF) to support the high data rate and a high linearity to suppress strong out-band blocking signals from WLAN at 2.4 GHz/5 GHz. Moreover, the frequency synthesizer has to deal with the frequency hopping from one sub-band to another within 9 ns. Special attention has to be paid to the design of the synthesizer to meet the spectrum mask imposed by Ref. [4].

In this paper, to optimize the output power efficiency, input referred NF and low-spur local oscillation (LO) signals, a monolithic 3.1–4.8 GHz OFDM UWB transceiver with a block diagram is presented, as shown in Fig. 1.

The received signal from the antenna is filtered by an external passive bandpass filter to reduce the level of out-band interferers. The transceiver uses direct-conversion architecture with the advantages of low power and no image problem. The circuit includes a receiver chain, a transmitter front-end, a frquency

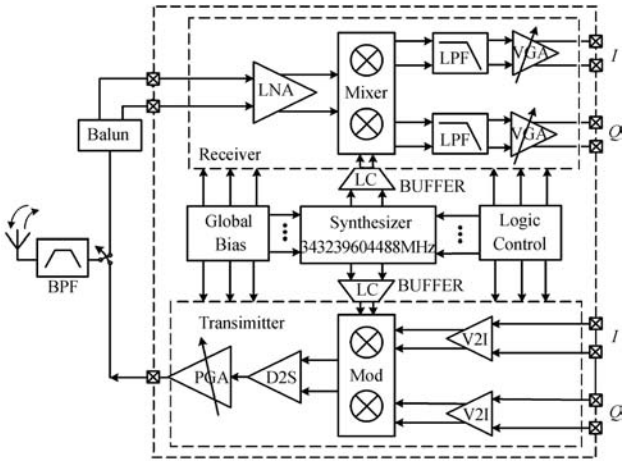

Fig. 1. Block diagram of the UWB transceiver.

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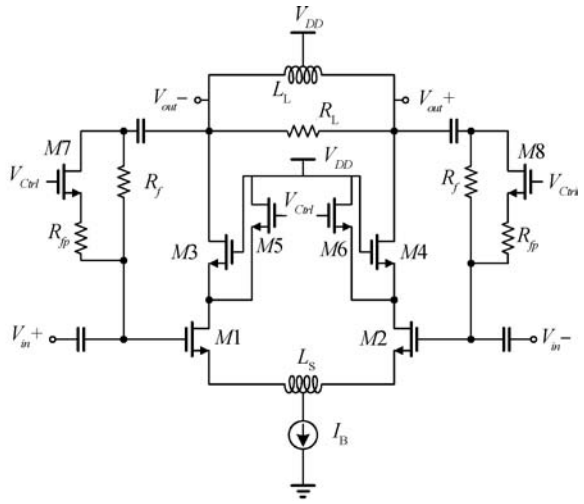


Fig. 2. Proposed gain controllable UWB LNA.

synthesizer hopping between 3.432 GHz, 3.690 GHz and 4.488 GHz, a global bias, 40-bit logic control, LC buffers between the synthesizer and the RF transceiver.

Sections 2, 3 and 4 describe the design of the receiver chain, the transmitter chain and the synthesizer, respectively. The chip implementation and measurements will be presented in section 5 and conclusions will be drawn in section 6.

2. Receiver chain

A block diagram of a fully differential receive path is shown in Fig. 1. The weak RF signal is filtered to ease the linearity requirement and then is amplified and converted into IF signals, which are large enough to drive the following analog-to-digital converter (ADC). With a sensitivity of −70.4 dBm for 480 Mbps data-rate, the differential peak-peak input voltage is about 600 mV (0 dBm in 50-Ω-system) for requirements from ADC. Considering 6-dB peak-to-average ratio (PAR) for OFDM signals, the required total voltage gain is over 65 dB with 40-dB variable range for different input signals. The NF is required to be as good to optimize the signal-to-noise ratio (SNR). It is set to 7–8 dB for a 0.18-μm CMOS realization. For its viability in an environment of strong in-band signals and out-band interferences, the input referred third intercept point (IIP_3) and 1-dB compression point (P_{1dB}) should be better than −9 dBm and −23 dBm, respectively, and the filters should provide at least 40 dB attenuation at 600 MHz to effectively reject out-band interferences. The IF signals covers from 4.125 to 264 MHz; the spectrum fraction near DC is avoided due to flicker noise and DC offset[3] in the direct-conversion architecture[6].

The proposed low noise amplifier (LNA) is based on resistive-shunt feedback circuit topology, as shown in Fig. 2. With gain control, it works at high-gain mode or low-gain mode to optimize the linearity of the receiver in scenarios of signals of different strengths and interferences.

Compared with the LC ladder[7] and transformer feedback matching[8] techniques, the proposed LNA achieves a wideband matching with a slight degradation in the NF at high frequency. The smaller area makes the design more attractive. Meanwhile, the AC feedback resistors R_f and differential source degeneration inductor L_S provide the wideband gain with low NF, high linearity and input matching. With V_{ctrl}, current bypassing transistors M5, M6 is set off for high gain-mode and on for low-gain mode. Compensation resistors (R_{fp}) controlled by M7 and M8 are connected in parallel with R_f to improve the input matching in low-gain mode. As the load, differential inductor L_L is shunt peaking with the parasitic capacitance at output and the capacitance from the following stage to exhibit a wideband load characteristic with the quality factor controlled by resistor R_L.

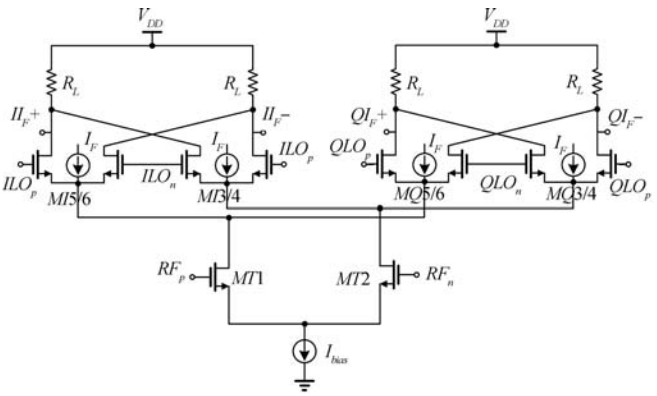


Fig. 3. Proposed quadrature mixer topology.

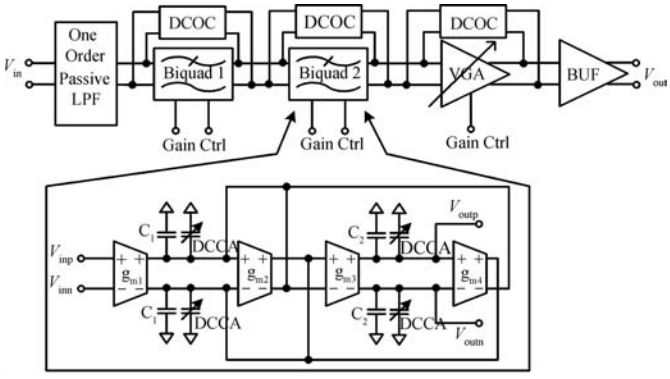


Fig. 4. Block diagram of LPF-VGA.

A merged Gilbert-type quadrature mixer following the LNA is shown in Fig. 3. The switching units (MI_3–MI_6, MQ_3–MQ_6) share the same transconductance stage (MT1, MT2), which minimizes the capacitive load to the LNA for a better receiver gain and noise performance. In Fig. 3, static currents (I_F) are injected into the common-source nodes of the switching stages. As the result, the static current in the load resistors is reduced. This improves the conversion gain and noise figure while keeping all the transistors in saturation as well as the flicker noise in switching transistors at IF outputs[6].

A low pass filter/variable gain amplifier (VGA), shown in Fig. 4, is employed following the mixer to suppress the strong interference signals and provide enough gain for different input signals. With a 264-MHz cutoff frequency, a fifth-order Chebyshev approximation filter is built with a Gm–C biquad structure. An operational transconductance amplifier (OTA) is realized with a pseudo differential topology to maximize the linearity of the filter[6].

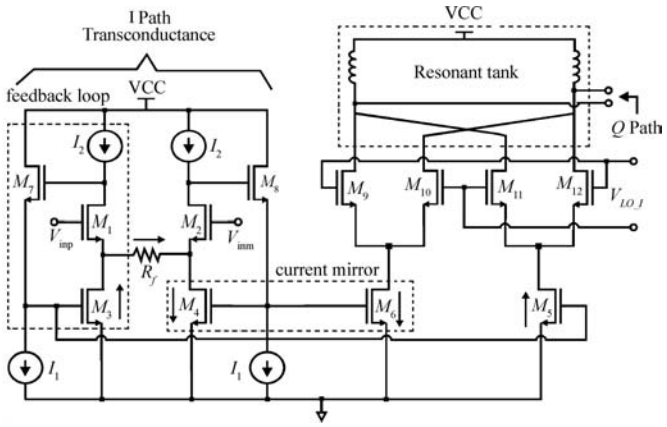


Fig. 5. Circuit schematic for the V2I converter of the I path.

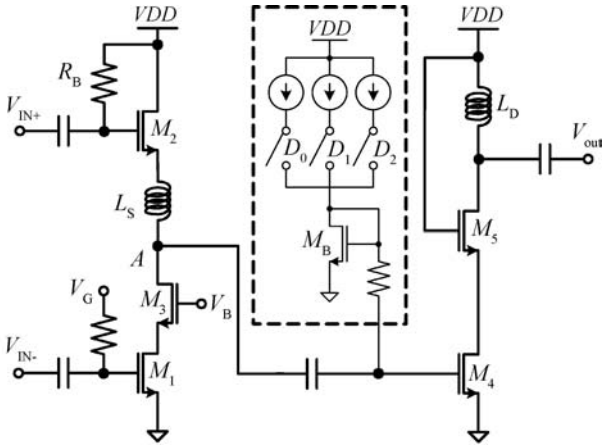


Fig. 6. Simplified schematic of D2S and PGA.

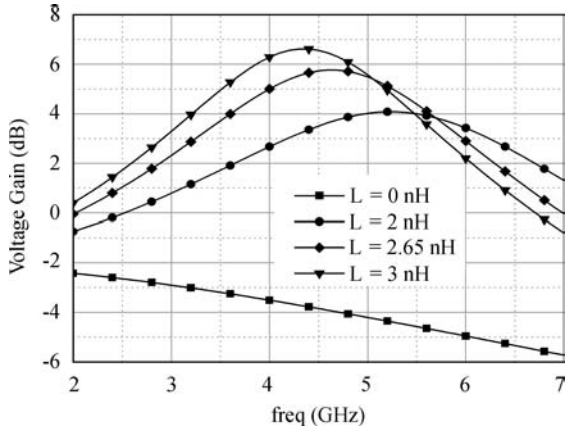


Fig. 7. Voltage gain response with inductor L_S.

The VGA is realized in a source-degeneration enhanced amplifier with source degeneration resistor and capacitor to widen the bandwidth. DC offset correction (DCOC) and digital controlled capacitance arrays (DCCA) are introduced to calibrate the DC offset and adjust the cutoff frequency in term of process variations. The simulation shows that this filter/VGA chain achieves a gain of 6–48 dB with 42-dB variable in 6-dB step, a total harmonic distortion (THD) less than −54 dBc with 100-mV peak-to-peak input voltage, an IIP3 of −6.35 dBV, and a NF less than 25 dB.

3. Transmitter chain

In the transmit path, the baseband I/Q signals are up modulated to RF signals with an output power spectral density of −41.25 dBm/MHz over the entire 1.585-GHz band. To satisfy the spectral-mask requirement, the output power should be less than −7 dBm. Thus, a variable gain control is needed. The transmitter (in Fig. 1) includes a voltage-to-current (V2I) converter, an up-conversion quadrature modulator, an on-chip differential-to-single (D2S) converter and an output programmable gain amplifier (PGA).

In the I-path, an up-conversion modulator with a voltage-to-current (V2I) converter is used (in Fig. 5). The linearity is mainly determined by the transconductance stage of the modulator. The stage uses a source degeneration resistor to improve the linearity. With a double-balanced Gilbert topology, the up-conversion mixer suppresses the carrier leakage. The differential baseband input signal is applied at the gate of M1, M2, which have a constant drain current controlled by I_2. With the feedback loop of M7, I_1, and M3, the applied signals $V_{\rm inp}$ and $V_{\rm inm}$ are converted to current by feedback resistor $R_{\rm f}$. The generated current I is circulated in M3, M4, which is amplified by the mirror transistor M5, M6, respectively, and sent to the mixer stage.

Compared with the common source input in traditional Gilbert mixers, this transconductance stage offers better linearity. A 1.8-V supply is large enough for the overdrive voltage $V_{\rm DS6}$ plus $V_{\rm DS9}$ with current mirror topology[5].

The transistor size is increased to reduce the mismatch in the transconductance stage, and thus, improve the sideband/carrier-signal suppression. The size of M6 is twice the size of M4 to compensate the gain drop due to the large feedback resistor for linearity.

At the output nodes, the modulated signals from the I-path and the Q-path are summed and converted into a voltage signal by a shunt peaking load of $R_{\rm L}$, $L_{\rm load}$ and $C_{\rm load}$ (parasitic capacitance at the output plus capacitance from the next stage). The differential inductor $L_{\rm load}$ is tuned to resonate with the relatively constant $C_{\rm load}$ around 3.5 GHz. The Q-factor of the resonant tank is determined by the resistor $R_{\rm L}$ Here, $L_{\rm load} = 4.2$ nH, $R_{\rm L} = 40\ \Omega$.

A simplified schematic of D2S and PGA is shown in Fig. 6. The differential output signals of the modulator are AC coupled to the D2S. The converted single-end RF signal is amplified by PGA with a 3-bit gain-control range. The output signal is sent to the antenna directly without an external balun, providing higher on-chip integration.

To minimize the high frequency gain reduction due to the parasitic capacitance at node A, the cascade transistor M3 is used to reduce the Miller capacitor and improve the load impedance characteristics. The inductor $L_{\rm s}$ serves as a peaking element with the capacitance at the output of D2S for wideband applications. The voltage gain of D2S versus different values of $L_{\rm S}$ is shown clearly in Fig. 7. With a proper value of $L_{\rm S}$ (2.65 nH), the gain peaks around 4.5 GHz (achieving a 3.1–4.8 GHz flat gain response with the modulator resonant at 3.5 GHz) and obtains 9-dB more gain without extra current compared to the

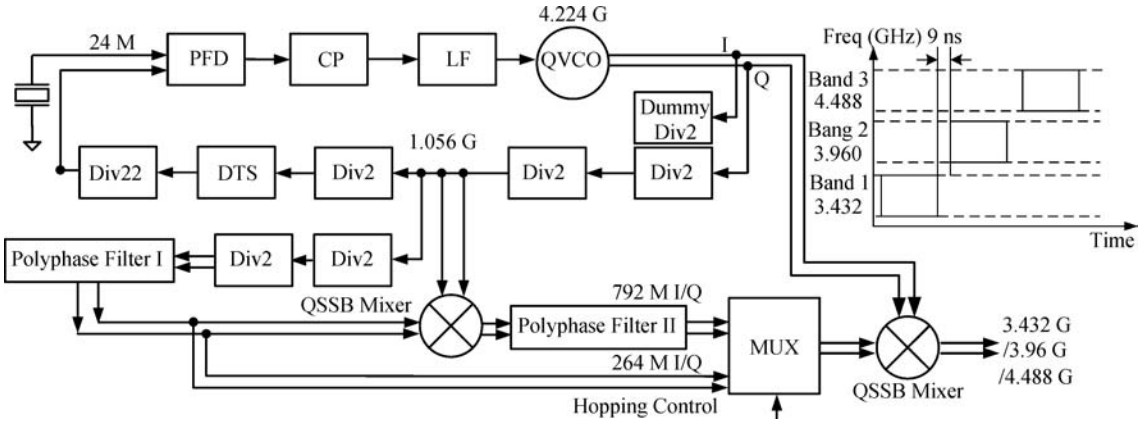


Fig. 8. Proposed synthesizer architecture.

case with no inductor.

The PGA uses a cascade single-end common-source amplifier. M5 reduce the Miller capacitance to improve the isolation and gain performance, and prevent M4 from being broken down by a possible high voltage of $2V_{DD}$ at the output. An output matching circuit consists of an on-chip inductor L_D and a coupling capacitor to the 50-Ω antenna. For the bias, a current mirror between M4 and MB is used. With the control bits D_0, D_1 and D_2 the gain of PGA is adjusted to satisfy the output power requirement. By co-design of the modulator, D2S and PGA, the gain flatness of the transmitter over 3.1–4.8 GHz is obtained with low power consumption[5].

4. Synthesizer

The synthesizer is necessary to generate quadrature LO signals for hopping among three sub-bands. Unlike traditional synthesizers, one of its design challenges is a wide LO frequency range covering 3.432 GHz, 3.960 GHz and 4.488 GHz for the direct conversion receiver and transmitter. The other is a fast hopping time less than 9 ns. To satisfy these requirements, one proposed method[1] is to use three dedicated phase-locked-loops (PLLs) to generate each LO frequency. One of the LO frequencies is selected by a multiplexer each time. This is an optimum solution for a good performance without spurs in RF bands. But this results in higher power consumption due to three PLLs. In Ref. [3], a fixed frequency of 4.442 GHz is obtained by a single PLL while variable signals of ±264-MHz or −792 MHz are obtained by a direct digital synthesizer (DDS). This approach employs only one single side-band (SSB) mixer to avoid spurs due to the additional SSB mixer. Unfortunately, with state of art technology, the power budget of this DDS circuit implementation is still beyond our expectation. A new proposed design is presented here.

Our proposed synthesizer is based on the architecture in Ref. [3], as shown in Fig. 8. It uses only one PLL with an LC oscillator to achieve a trade-off between power and area. To obtain a hopping time less than 9 ns, a topology based on SSB-mixers is adopted. A 24-MHz reference is fed for the PLL to generate a steady frequency of 4.224 GHz. With this 4.224-GHz frequency, a SSB-mixer generates 264-MHz and 1024-MHz tones simultaneously by dividers inside the PLL. An additional SSB-mixer combines these two tones into 792 MHz, and an inverter simply changes the sign of the 264-MHz signal. When LO frequency for band #1 (3.432 GHz) is required, the 4.224-GHz tone is shifted down by 792 MHz. When band #2 or band #3 is needed, the ±264 MHz signal would be used instead by the multiplexer. In terms of simplicity, this frequency plan is the optimum solution. However, some challenges are posed due to the non-ideal effects along with this solution.

First, for an ideal 264-MHz rectangular signal, its third order harmonic is only 9.5 dBc lower than the fundamental tone. This harmonic tone will mix the 4.224-GHz signal up to unwanted spurs, as does the fifth-order harmonic. This harmonic tone consumes less power which is further suppressed by subsequent circuits, since it is far away from the desired frequencies. A low frequency mixer combines a 264-MHz signal with 1024-MHz tones to generate 792-MHz signals. However, with the harmonics of 264-MHz, the tone of 792-MHz as well as the spurs will appear at the output of the mixer. These tones are difficult to remove due to the relatively close spacing. To solve this problem, poly-phase filters are used to suppress harmonic tones in UWB frequency synthesizers[2]. In this paper, two poly-phase filters are employed following the divider chain, as shown in Fig. 8. With the anti-phase relationship between the 264-MHz tone and its third harmonic, this filter suppresses the harmonics effectively. However, very few publications mention another function of the poly-phase filter in phase/amplitude correction, which is useful to suppress the spurs due to phase-amplitude imbalances in quadrature paths. This extra spur-suppression by the poly-phase filters is the special point of our synthesizer, though the mismatch along with the filter slightly degrades the suppression.

Figure 8 shows the insertion of the poly-phase filters and how to remove the unwanted signals. When the signals are applied with a clockwise input sequence (in Fig. 9(a)), two adjacent branches counteract each other since an additional 45° phase-shift is introduced for each branch. This is not the case for applying signals with a counter-clockwise sequence (in Fig. 9(b)). Two adjacent branches enhance each other, contributing a 3-dB gain[9]. The key point is that if the 264-MHz (from the divider in Fig. 8) is applied to the filter with a counter-clockwise sequence, its third harmonic of 792-MHz would be in a clockwise sequence. So does the relationship between 792-MHz and 264-MHz at the output of the low frequency SSB-mixer. Simulation shows that with a two order poly-phase fil-

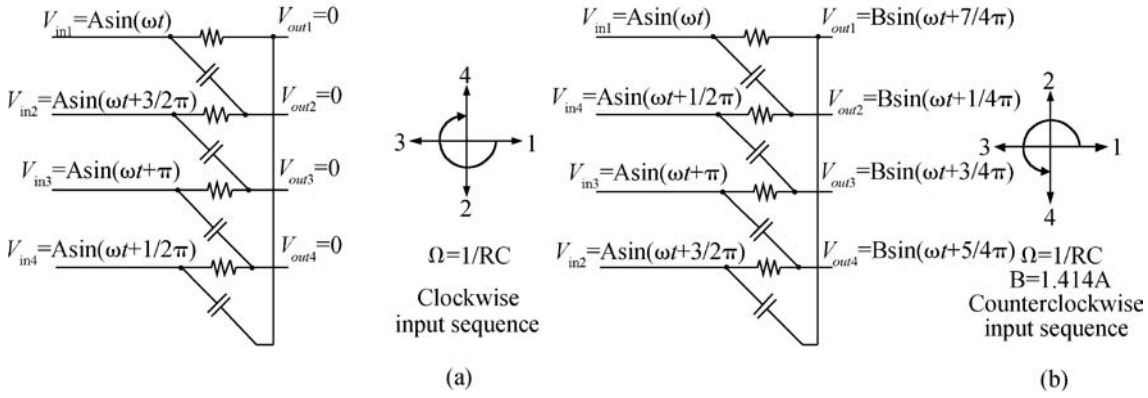


Fig. 9. Poly phase filter characteristic with respect to different input sequences.

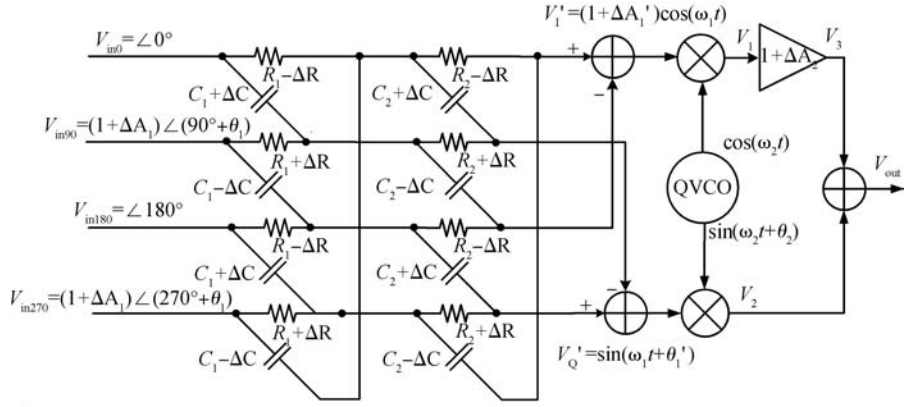


Fig. 10. Poly-phase filter model with RC mismatch.

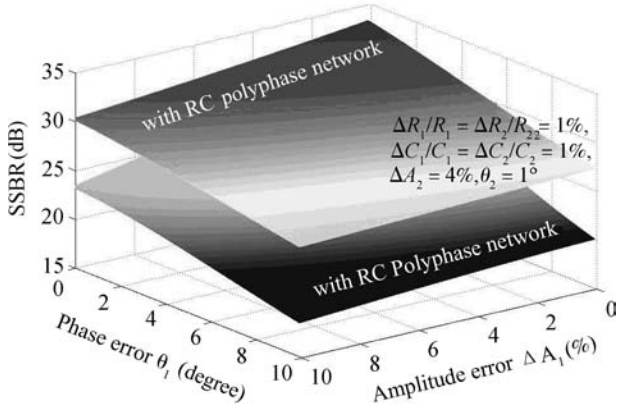


Fig. 11. Simulated SSBR with mismatch.

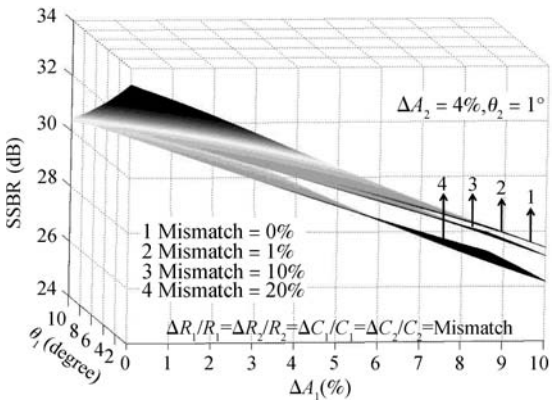


Fig. 12. Impact of mismatch on SSBR.

ter, 27-dB spur suppression is achieved under the ±15% process variation.

With an in-depth analysis, it is interesting to find that the RC poly-phase network also reduces the phase-amplitude imbalance of the signals at ±264 MHz or –792 MHz. Taking the mismatch between the RC component of the network and other non-ideal effects into account, a more complex model is proposed in Fig. 10, where V_e and θ_e represent an amplitude error and a phase error before the RC network, respectively, θ_2 and ΔA_2, a phase error of quadrature VCO and an amplitude error of the SSB-mixer, respectively, and ΔR and ΔC, resistance mismatch and capacitance mismatch of the RC network, respectively.

The sideband rejection ratio (SBRR) can be expressed as:

$$\mathrm{SBRR} = 10\lg\frac{1+K_1^2K_1^2+2K_1K_2\cos(\theta_1'-\theta_2)}{1+K_1^2K_1^2-2K_1K_2\cos(\theta_1'+\theta_2)}, \quad (1)$$

with $K_1 = 1+\Delta A_1$, $K_2 = 1+\Delta A_2$. The SSBR versus amplitude error and phase error is shown in Fig. 11, in a practical case of $\Delta R_1/R_1 = \Delta R_2/R_2 = \Delta C_1/C_1 = \Delta C_2/C_2 = 1\%$, $\Delta A_2 = 4\%$, $\theta_2 = 1°$. It is observed that without the poly-

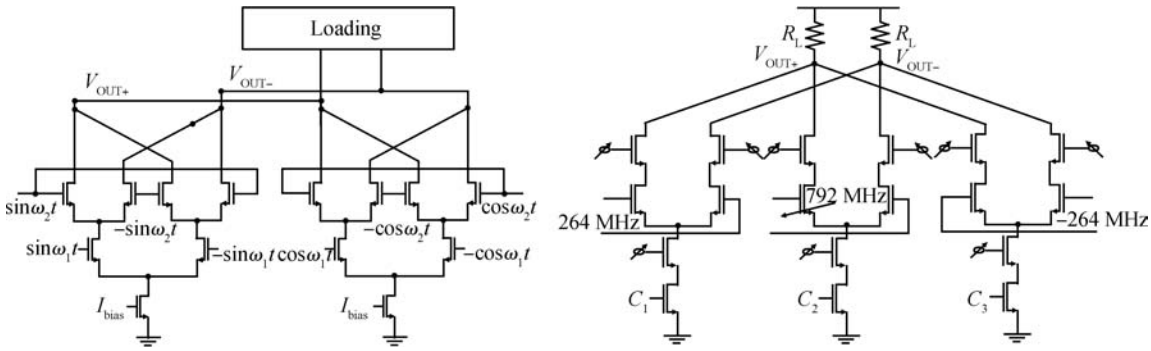


Fig. 13. SSB-mixer and multiplexer.

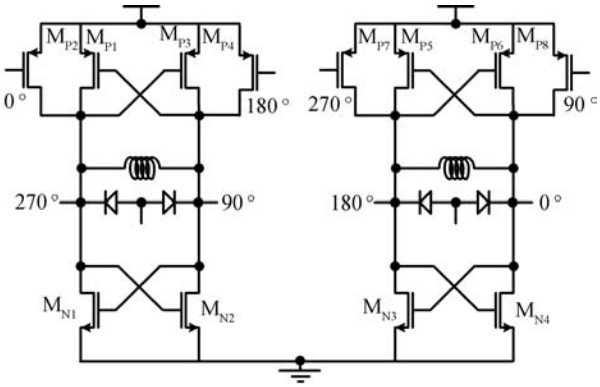


Fig. 14. Schematic of QVCO.

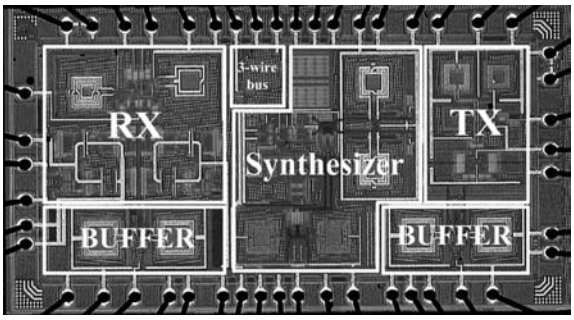


Fig. 15. Transceiver chip photograph.

phase filter, if $\theta_1 = 2°$ and SSBR = 30 dB, ΔA_1 should be less than 1%. With the poly-phase filter, ΔA_1 is relaxed to 5% which eases the design in the CMOS process. Figure 12 exhibits the influence of RC mismatch with $\Delta A_2 = 4\%$, $\theta_2 = 1°$. In a case of mismatch less than 1%, degradation to SSBR is negligible.

As shown in Fig. 13, an SSB-mixer consists of two Gilbert cells and a loading network. The trans-conductance stage of each mixer converts input voltages into currents which are summed up via the loading network. The low-frequency SSB-mixer uses resistor load while the RLC network provides sufficient conversion gain for the high-frequency SSB-mixer. Figure 13 also shows the −792-MHz signal are applied to three trans-conductance stages sharing the same loading. A cascade stage is preferred to provide better isolation. Simulation shows a 15-dB isolation improvement.

Two identical LC oscillators are cross-coupled to generate quadrature signals (shown in Fig. 14). Each of the oscillators uses a complementary structure to reduce power dissipation. In the current-limited regime, the swing of the complementary one is twice as large as the NMOS-only one with the same current and LC tank[10]. The tail current source is avoided to eliminate its phase noise contribution through thermal and flicker noise conversion[11]. Although there is a trade-off between phase accuracy and phase noise[12], a stronger coupling strength (MP2/MP1 = 1) is preferred in the design for better phase error performance, because SSBR is sensitive to phase error, and the phase noise requirement is relatively easy to achieve (−100 dBc/Hz @ 1-MHz offset). Through a wide-band LC buffer, the generated LO signals are sent to the receive path (RX) and the transmit path (TX), respectively, which have a flat gain response between 3.1–4.8 GHz.

5. Chip implementation and measurements

For a monolithic transceiver, good isolation between different building blocks is a critical issue. A patterned grounding shielding (PGS) technique is used with the inductors. The ADS momentum simulation shows that the PGS provides 20-dB extra isolation between 3–5 GHz. The transceiver is realized in Jazz Semiconductor's 0.18 μm RF CMOS technology. As shown in Fig. 15, the die size is 3.4×1.8 mm^2 including ESD protection pads. The chip is packaged on a Rogers-4003C PCB with chip-on-board (COB) technology and measured under a 1.8-V supply.

The receiver gain at the 3960-MHz band versus frequency is shown in Fig. 16 with different gain control bits. The gain varies from 16 to 68 dB with 10 dB from LNA and 42 dB from LPF/VGA at 6 dB/step. The cut-off frequency is about 264 MHz. At 600 MHz, the attenuation is better than 45 dB, satisfying the system requirements. In the pass-band, the gain flatness is below 1 dB at low gain mode and degrades to 3 dB at high gain mode due to output buffer saturation.

The noise figure versus IF frequency in three sub-bands is shown in Fig. 17. A lower NF of 5.5 dB in the 3.96-GHz band and a higher NF up to 8.8 dB in the 3.432-GHz band are obtained. This higher NF is due to the imperfect LNA input matching, and gain variation in different sub-bands caused by LO power variation from the synthesizer. In the same band, the NF degradation at higher IF offset frequency is due to the poor noise suppression of the first biquad stage in the low pass

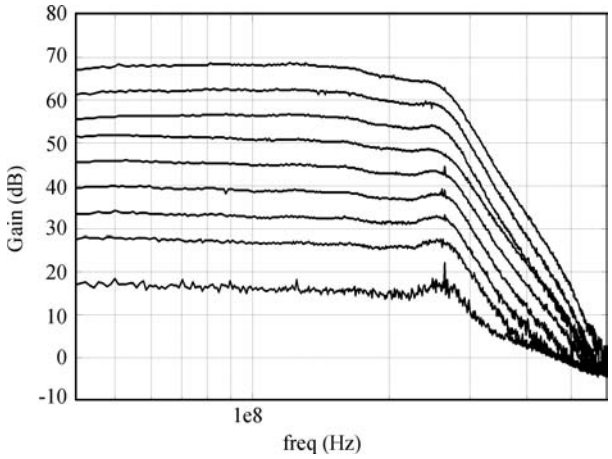


Fig. 16. Receiver gain steps at the 3.96-GHz band.

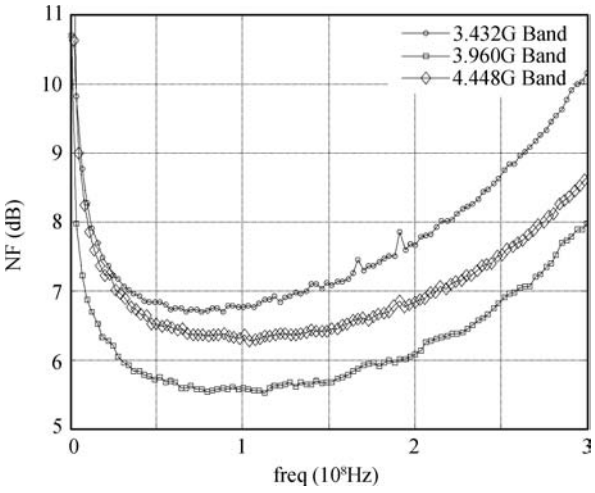


Fig. 17. Noise figure at different bands.

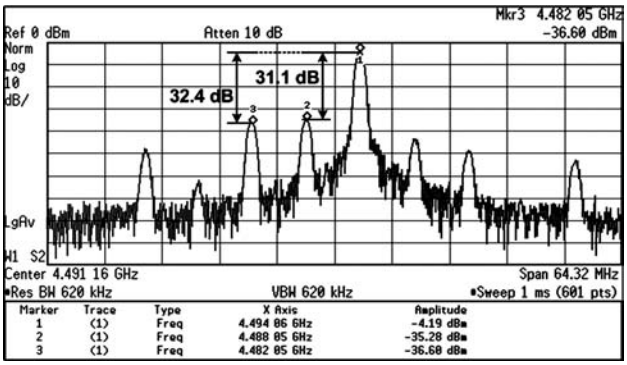
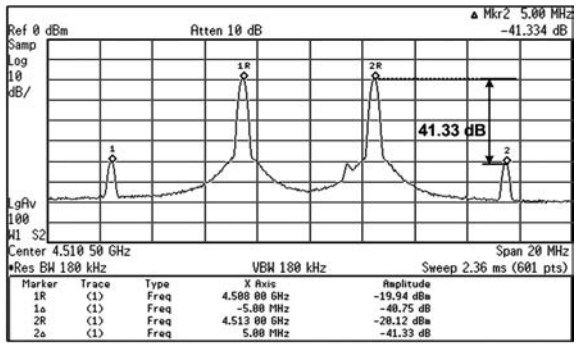


Fig. 18. TX output power at 4.488 GHz.

filters.

The output power of the transmitter at band #3 is shown in Fig. 18. 6-MHz I/Q baseband signals from a vector signal generator (E4438C) and 4488-MHz LO signals from a synthesizer are fed into the I/Q inputs of the transmitter. The sideband rejection and LO leakage suppression are measured as 32.4 dBc and 31.1 dBc, respectively, which can be further improved with calibration.



Output third order intermodulation point (OPI3) at band#3 4488MHz

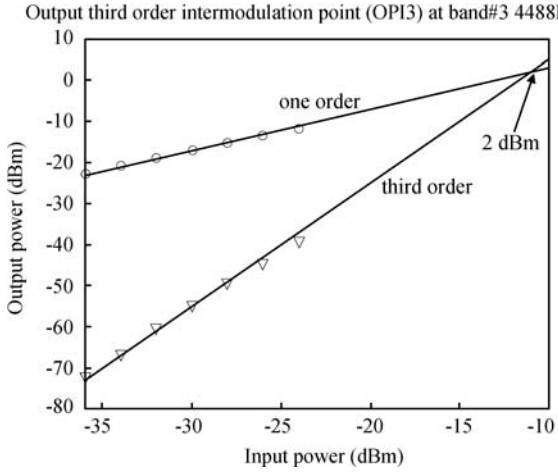


Fig. 19. OIP3 of the RF transmitter with two-tone test.

In testing of the two tones with 5-MHz spacing, the corresponding transmit output third order intercept point (OIP3) at band #3 (worst case) is about 2 dBm, as shown in Fig. 19, with better values at band #1 and #2 of 11 dBm, 6.5 dBm, respectively, as summarized in Table 1.

With a MUX controlled by an external signal, the LO hopping time among sub-bands is below 2.05 ns, as shown in Fig. 20. The overall performance of the transceiver is summarized in Table 1. Input matching S_{11} is unexpectedly above –10 dB in lower sub-bands; one factor comes from the inaccurate ESD pad and bonding wire models at 3–5 GHz. Another is due to the unmatched characteristic impedance of the signal trace on the PCB, which causes the measured real impedance to be much lower than 50 Ω below 4 GHz.

For the transmit path, the gain at band #3 drops 3 dB beyond our expectation due to parasitic capacitance from the ESD pads at the output node and extra from the PCB at high frequency. This gain drop can be compensated with one gain control bit available.

Table 2 gives a performance comparison of this work with published UWB transceivers. It shows a better receive linearity and a lower transmit power consumption with a low cost 0.18-μm RF CMOS.

6. Conclusion

A monolithic 3.1–4.8 GHz transceiver for an MB-OFDM UWB system is realized with 0.18-μm RF CMOS. With a receive gain of 68 dB, an out-band IIP_3 of 9 dBm, a controllable output power from –10.7 to –3 dBm and an intra-band

Table 1. Summary of the performance of the transceiver.

Transceiver	Parameter	3.1–4.8 GHz
Receive path	Voltage gain	68–13 dB
	NF	5.5–8.8 dB
	S_{11}	–5 to –15 dB
	IIP_3	–4 dBm (in-band), 9 dBm (out-band)*
	out-band IIP_2	30.2 dBm
Synthesizer	PN @ 1 MHz	–103.4 dBc/Hz**
	RMS noise	2.138 ° (to 100M?)
	Sideband suppression	32.43–42.59 dBc
	LO suppression	23.01–25.27 dBc
Transmit path	Output P_{1dB}	–10.7 to –3 dBm
	Output IP_3	2–11 dBm
	Sideband rejection	30–34 dBc
	LO suppression	23–31 dBc
Others	Supply voltage	1.8 V
	Current consumption	95 mA (RX)
		65 mA (SYN)
		20 mA (TX)
		41 mA (LC buffer)
	Chip area	3.4×1.8 mm^2

*out-band IIP_3 measured with LNA at low gain mode, using 5.2 GHz and 5.8 GHz out-band signals.
** The worst case at band #3 4.488 GHz

Table 2. UWB transceiver comparison.

Parameter	Ref. [1]	Ref. [2]*	Ref. [3]	This work
Technology	0.13 μm CMOS	0.25 μm GeSi	0.13 μm CMOS	0.18 μm CMOS
Frequency range (GHz)	3.1–4.8	3.1–4.8	3.1–4.8	3.1–4.8
Gain (dB)	69–73	59	37	13–68
NF (dB)	6.5–8.4	4.5	3.6–4	5.5–8.8
RX_{IIP3} (dBm)**	n/a	-6	$+2$	$+9$
TX_{P1dB} (dBm)	-10	n/a	$+5$	-7.7
Phase noise @ 1 MHz (dBc/Hz)	-104 to -106	-104	n/a	-103.4
Power RX/TX (mW)	105 RX + TX	195 RX + LO	237/284	288/183***
Total area (mm^2)	1	4	6.6	6.1

* Receiver and synthesizer only.
** RX_{IIP3} refers to out-band IIP3 at low gain mode.
***Power of synthesizer and its buffers are included in RX and TX.

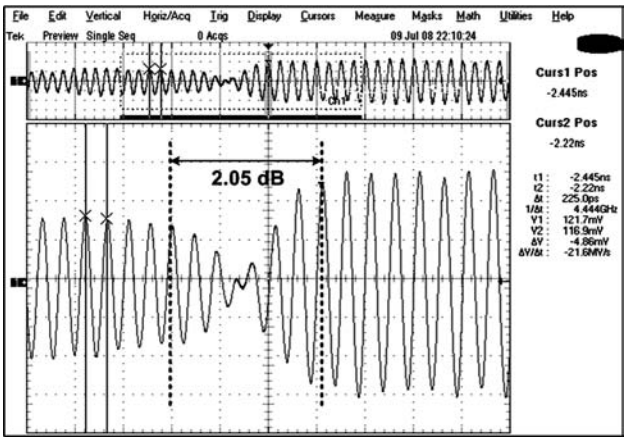


Fig. 20. Frequency hopping time from band #2 to band #3.

hopping time less than 2.05 ns, the work shows the feasibility of a good performance cost-effective CMOS solution for MB-OFDM UWB RF transceivers.

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