A fast lock frequency synthesizer using an improved adaptive frequency calibration*

Yin Yadong(阴亚东), Yan Yuepeng(阎跃鹏)†, Liang Weiwei(梁伟伟), and Du Zhankun(杜占坤)

(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

Abstract: An improved adaptive frequency calibration (AFC) has been employed to implement a fast lock phase-locked loop based frequency synthesizer in a 0.18 μm CMOS process. The AFC can work in two modes: the frequency calibration mode and the store/load mode. In the frequency calibration mode, a novel frequency-detector is used to reduce the frequency calibration time to 16 μs typically. In the store/load mode, the AFC makes the voltage-controlled oscillator (VCO) return to the calibrated frequency in about 1 μs by loading the calibration result stored after the frequency calibration. The experimental results show that the VCO tuning frequency range is about 620–920 MHz and the in-band phase noise within the loop bandwidth of 10 kHz is –82 dBc/Hz. The lock time is about 20 μs in frequency calibration mode and about 5 μs in store/load mode. The synthesizer consumes 12 mA from a single 1.8 V supply voltage when steady.

Key words: adaptive frequency calibration; frequency detector; frequency synthesizer; phase-locked loop
DOI: 10.1088/1674-4926/31/6/065011 **EEACC:** 2570

1. Introduction

As wireless communication develops, frequency synthesizers with a wide frequency range and short lock time are becoming more and more imperative. If the wide frequency range is implemented using a single band voltage-controlled oscillator (VCO), the frequency–voltage gain of the VCO will be high and this will deteriorate the phase noise seriously by conversing amplitude modulation (AM) noise into frequency modulation (FM) noise[1]. Thus the gain has to remain low while the frequency range is broadened. One general method to keep the gain low is using a switched capacitors array (SCA) to divide the VCO frequency range into several low gain sub-bands. However, this requires an extra operation to choose the right sub-band, so the lock time is increased.

Fortunately, the lock time problem can be solved by using the adaptive frequency calibration (AFC) technique[2−4]. In the AFC, the frequency detector (FD) is the key component, and its detecting time and detecting error directly determine the performance of the AFC. In the AFC of Ref. [2], its FD is implemented by counters which need large enough counts to obtain an acceptable error. So a large amount of time will be needed. Another FD is the rotational frequency detector in Refs. [3, 4], in which the detecting time is inversely proportional to the input frequency difference. When the difference is small, it will take a lot of time to make a decision. Another of its flaws is that the difference must be less than half of the input frequencies. The frequency calibration results of AFC in these examples cannot be saved. Even if the synthesizer wants to switch back to the former frequency point, the AFC has to calibrate the frequency again. In our design, two improvements have been proposed: first, a novel FD is designed to shorten the frequency calibration time; and second, the results obtained after frequency calibration can be stored, so the frequency synthesizer can return to the calibrated frequency point rapidly by loading the results.

2. Circuit design and implementation

Figure 1 illustrates the structure of the proposed frequency synthesizer which consists of a reference divider (Rdivider), a phase frequency detector/charge pump (PFD/CP), an improved AFC, a low-pass filter (LPF), an SCA-VCO, a programmable loop divider (Pdivider) and a serial peripheral interface (SPI). All circuits are integrated in the chip except for the LPF and the tune inductor of the VCO.

The AFC can operate in two modes: the frequency calibration mode and the store/load mode. In the former mode, the AFC detects the frequency difference between the reference frequency ($f_{\rm FD}$) and the loop feedback frequency ($f_{\rm BAK}$), and then calibrates the VCO's band and the tune voltage ($V_{\rm tune}$) to make its frequency ($f_{\rm VCO}$) approach the expected frequency based on the binary search algorithm (BSA). In the latter mode, the results obtained after frequency calibration are stored in the memory and can be loaded to make the synthesizer return to the corresponding frequency point.

When the signal STR or RD become active, the AFC is triggered. First, by pulling the signal RST, SW and FSH down to 0, the AFC turns off the PFD/CP, closes the analog switches (SW1, SW2 and SW3), and loads the divide ratio FN1 into the Pdivider. Then the AFC works in frequency calibration mode (if STR = 1) or stored/load mode (if RD = 1) to adjust $f_{\rm VCO}$ to the expected one. When the operation is finished, the AFC turns on the PFD/CP, opens the analog switches, makes the divide ratio of Pdivider return to FN2, and idles itself. When the calibration is over, $f_{\rm VCO}$ has been very close to the expected frequency, so the synthesizer achieves the locked state in no

* Project supported by the National High Technology Research and Development Program of China (No. 2007AA01Z2a8).
† Corresponding author. Email: yanyuepeng@ime.ac.cn
Received 30 November 2009, revised manuscript received 18 January 2010

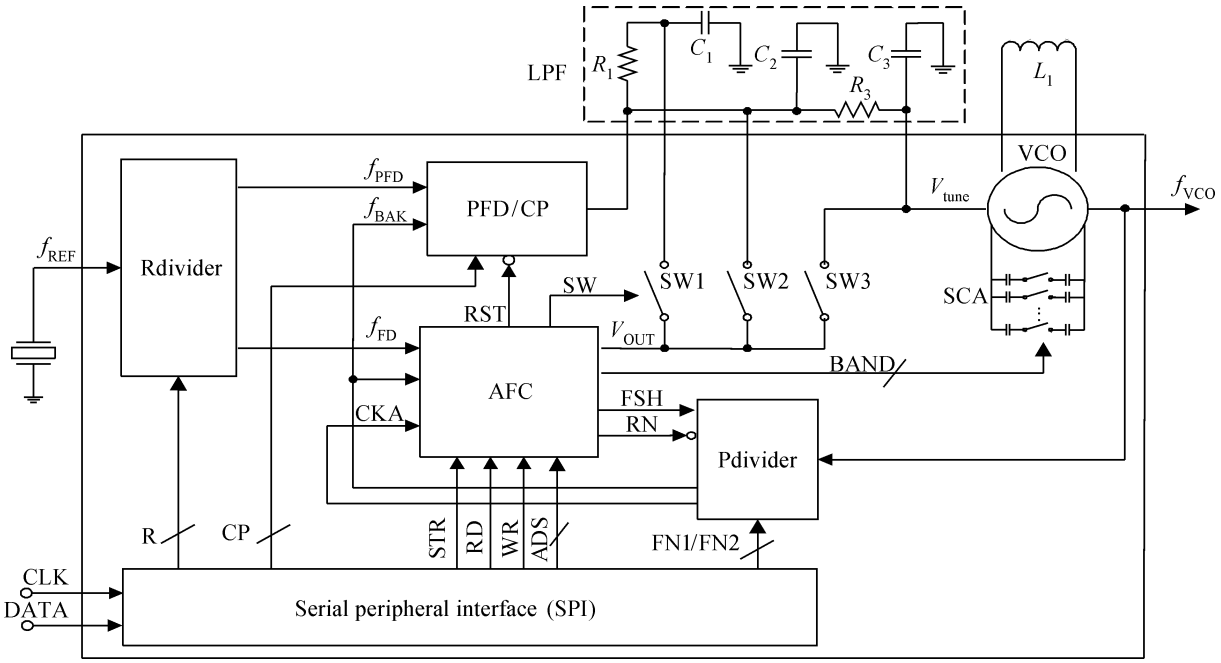

Fig. 1. Schematic of the proposed frequency synthesizer with improved AFC.

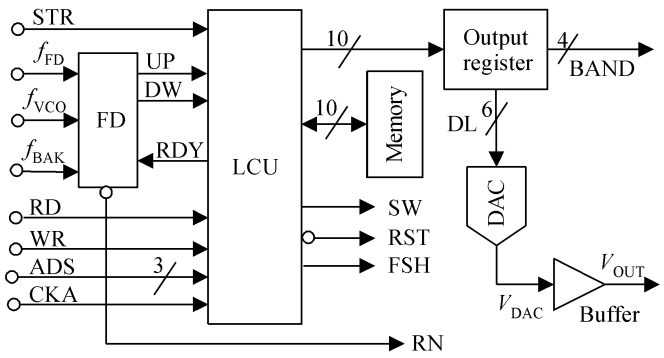

Fig. 2. Schematic of the improved AFC.

time.

The total lock time of the frequency synthesizer (t_s) is expressed as Eq. (1) and it is the sum of the frequency calibration time (t_{AFC}) and the normal phase-locked time (t_{PLL}). In Eq. (2), t_{AFC} relates to the frequency calibration cycle (T_C), which is determined by the frequency detecting time (t_{FD}) and the delay for the LPF capacitors' charging/discharging (t_d), and the number of frequency calibration cycles (n), which is no larger than the total bits of the AFC quantization value (K).

$$t_S = t_{AFC} + t_{PLL}, \tag{1}$$

$$t_{AFC} = nT_C = n\,(t_{FD} + t_d)\,, \quad n \leqslant K. \tag{2}$$

Since a novel frequency detector is used in AFC, t_{FD} is shortened to min $(1/f_{FD}, 1/f_{BAK})$. In the store/load mode, the AFC only need one cycle without frequency detection, so $t_{AFC} = t_d$. Obviously, t_{AFC} does not relate to the PLL loop bandwidth and can remain constant while the loop bandwidth becomes narrower.

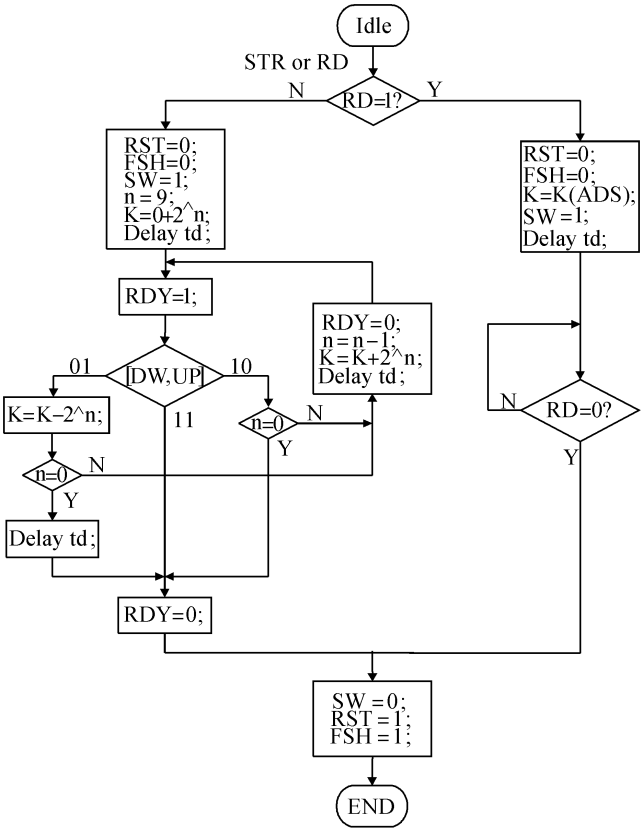

Fig. 3. State diagram of the proposed AFC.

2.1. The improved AFC

A schematic of the improved AFC is shown in Fig. 2 and a state diagram of the AFC is given in Fig. 3. The AFC consists of an FD, a logic control unit (LCU), an output register, a memory, a digital to analog converter (DAC) and a buffer. In

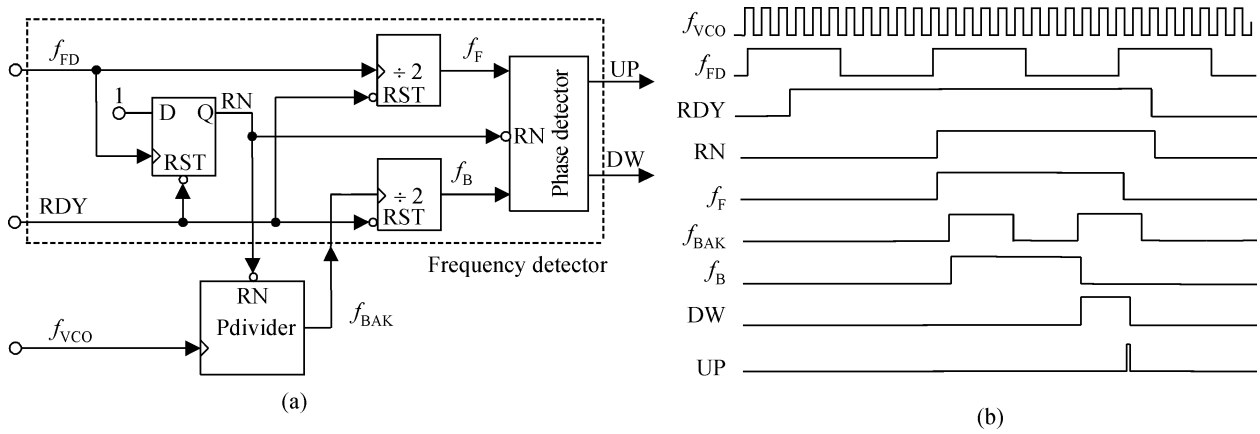

Fig. 4. (a) Schematic of the novel FD. (b) Time chart of the FD.

Fig. 2, STR is the trigger signal, RD/WR is the write/read signal, ADS is the 3bit address bus, CKA is the drive clock, SW is the control signal of the analog switch, RST is the PFD/CP reset signal, RN is the synchronizing signal of the Pdivider and FSH is the AFC's finish signal. As the core of AFC, the LCU is responsible for all operations, such as adjusting the quantization results based on the results of FD and storing or loading the results. The 10 bit quantization result, whose high 4-bit output (BAND) is used to select the sub-band of VCO and low 6-bit output (DL) is converted into an analog voltage by DAC, is presented at the output register. Then the conversion voltage is strengthened by the buffer and is loaded onto the LPF capacitors to generate the VCO tune voltage (V_{tune}). The memory is composed of 8 groups of registers and each group has its individual address. When WR or RD is active, quantization results will be stored in or loaded from the registers indicated by ADS.

2.1.1. Frequency detector

As Section 1 described, the frequency detectors reported in the literature have several drawbacks, such as long detecting time and limit of the input frequency difference. In this paper, a novel FD without these flaws is proposed and its principle is explained.

Apparently, the phase difference between f_{FD} and f_{BAK} can be expressed as Eq. (3).

$$\Delta\phi = \Delta f t_{\text{FD}} + \phi_{\text{o}}, \tag{3}$$

where $\Delta\phi$ and Δf are the phase and frequency difference between f_{FD} and f_{BAK}, and ϕ_{o} is the initial phase difference. ϕ_{o} can be eliminated effectively by synchronizing f_{BAK} with f_{FD} [5, 6], so Δf becomes directly proportional to $\Delta\phi$ and can be detected indirectly by detecting $\Delta\phi$ with the phase detector (PD).

A schematic of the novel FD is illustrated in Fig. 4(a), and the timing diagram of the detection operation is shown in Fig. 4(b). In the figures, RDY is the trigging input, and the RN is the synchronizing output. Before the action of frequency detection, the RDY and RN are low and the circuit is disabled. When the RDY becomes high, the FD returns to work. As the rising edge of f_{FD} triggers RN to become high, the Pdivider starts to work and f_{BAK} comes out. The signals f_{F} and f_{B}, which are the 1/2 divided results of f_{FD} and f_{BAK} respectively, enter into the phase detector (PD). Assuming $f_{\text{BAK}} > f_{\text{FD}}$, the PD will detect the falling edge of f_{B} first, then the DW gets and remains high until the falling edge of f_{F} comes. When the RDY becomes low, the circuit turns disabled and waits for next operation. The novel frequency detection operation can be finished within a period of f_{FD}, and saves a large amount of time because it is without counting. Moreover, there is no limit of the input frequency difference.

2.1.2. DAC and buffer

The low 6-bit quantization result of AFC is converted into an analog voltage by the DAC shown in Fig. 5. The 6-bit input DL is decoded into two groups of 7-bit data which drive the equally weighted current source (EWCS) to generate current $I_{\text{TB, L}}$ and $I_{\text{TB, H}}$. The voltage V_{TB} determines the unit current I_{o} in the EWCS. V_{BL} adds itself to the output voltage through the current I_{BL}. The output V_{DAC} can be expressed as Eq. (3). The output V_{DAC} should not overrun the dynamic range of the charge pump to make sure that the charge pump can work properly after AFC. This can be guaranteed with an appropriate dynamic range of V_{DAC} attained by choosing V_{TB} and V_{BL} appropriately.

$$\begin{aligned} V_{\text{DAC}} &= R_{\text{L}} \left(I_{\text{TB, L}} + I_{\text{TB, H}} + I_{\text{BL}}\right) \\ &= V_{\text{BL}} + \frac{V_{\text{TB}}}{32} \sum_{i=0}^{5} 2^i t\text{DL}[i]. \end{aligned} \tag{4}$$

The output voltage of the DAC is strengthened by the buffer shown in Fig. 6 and then drives the capacitors in the LPF to generate V_{tune}. Since the bandwidth of the LPF could be low, the capacitance would be large. A buffer that can achieve significant performances in speed and driving capability while getting a low power consumption is needed[7].

2.2. Other functional blocks

The wide-band VCO with SCA is shown in Fig. 7. The LC tank of the VCO is constituted by an off-chip inductor (L_1), varactors (C_3, C_4) and SCA. The SCA consists of a 4-bit binary weighted array of NMOS switches and MIM capacitors and splits the frequency range of the VCO up into 16 sub-bands. A PMOS programmable current source has been used to provide the tail current and its current can be altered from 0 to 10 mA.

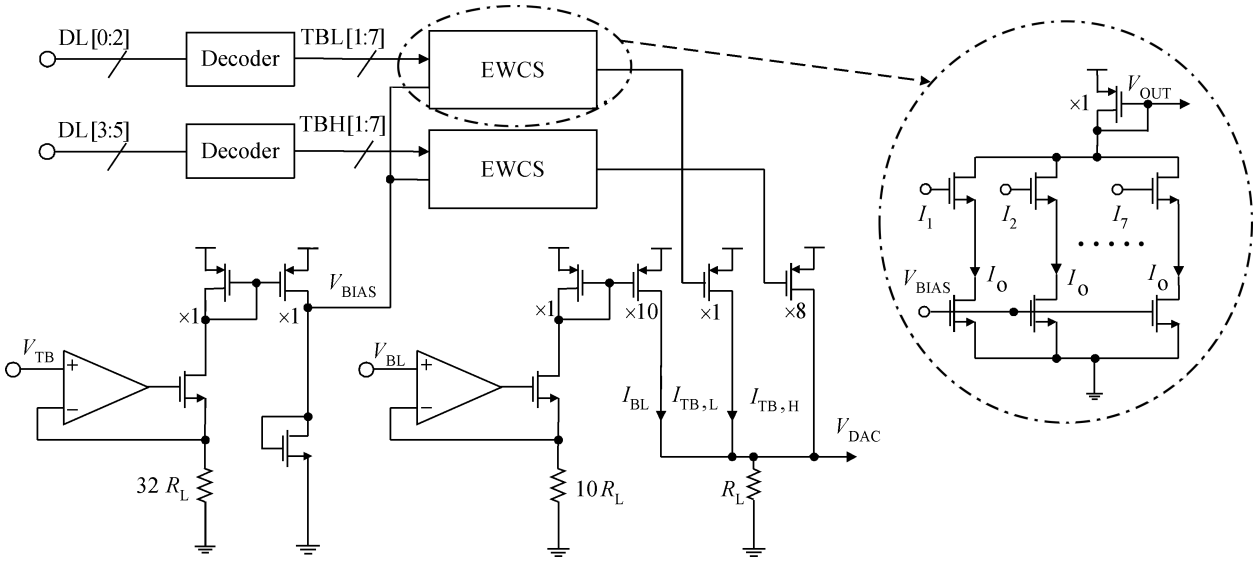

Fig. 5. Schematic of the DAC.

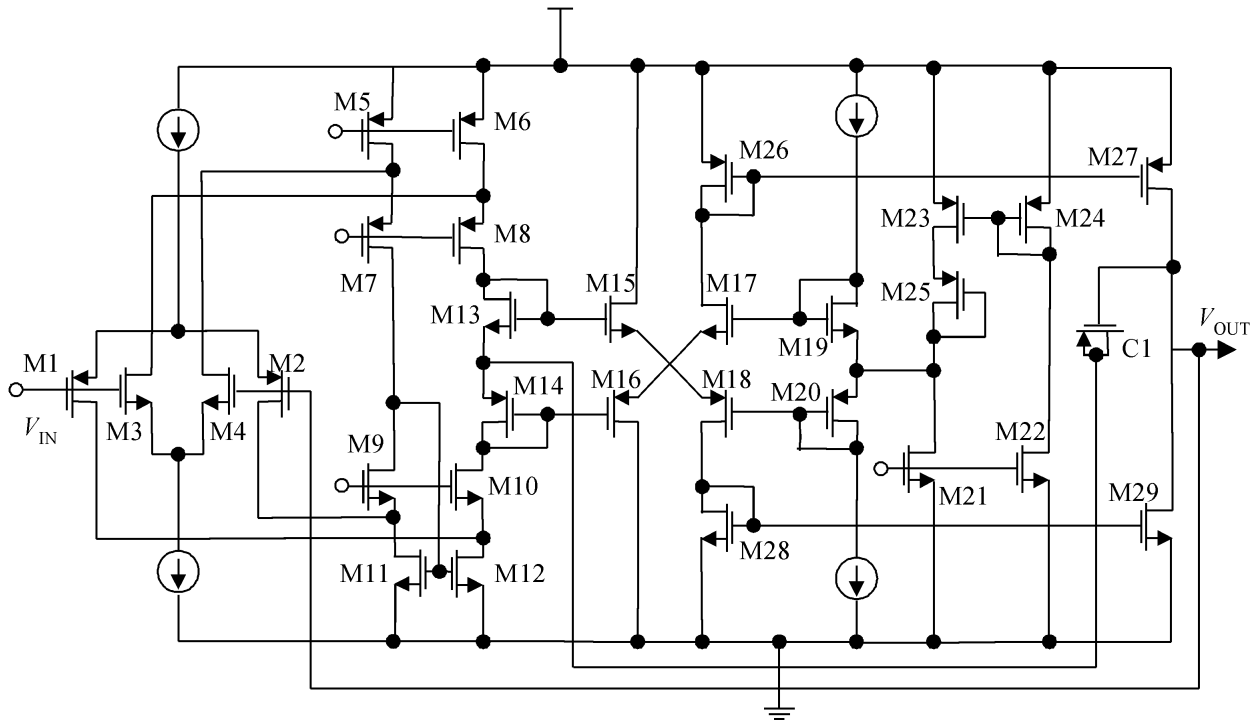

Fig. 6. Schematic of the buffer.

The programmable loop divider (Pdivider) consists of a dual-modulus prescaler (DMP), a swallow pulse counter and a modulus controller, as shown in Fig. 8. The FN1 and FN2 are the divide ratios for frequency calibration and the normal phase-locked loop respectively. As the input FSH is low, the modulus controller loads FN1 onto the swallow pulse counter; otherwise, FN2 is loaded. RN is the synchronizing reset input of the Pdivider and is provided by the AFC.

A dead-zone-free PFD and a current programmable charge pump are used in the frequency synthesizer. The reference divider provides the reference frequencies for the AFC and the PFD. A serial peripheral interface is integrated on the chip to configure the parameters of the synthesizer. A third out-chip loop low-pass filter is used and can be rebuilt conveniently.

3. Experimental results

The proposed frequency synthesizer has been fabricated in a 0.18 μm COMS process. Figure 9 shows a microphotograph of the frequency synthesizer with a die area less than 1.1 mm^2.

To verify the performances of the synthesizer, a PLL loop bandwidth of about 10 kHz, a 1.6 MHz reference frequency for AFC and PFD, an LPF with 13 nF capacitance were used. The measured VCO frequency range was from 620 to 920 MHz

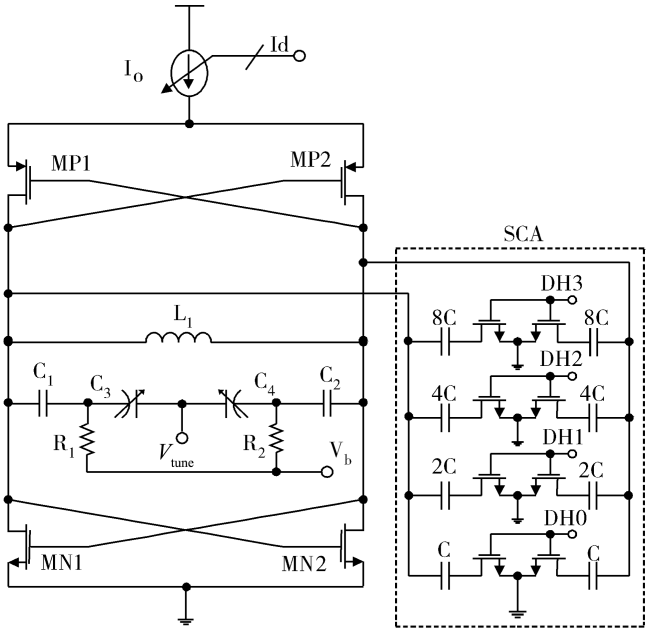

Fig. 7. Schematic of the SCA-VCO.

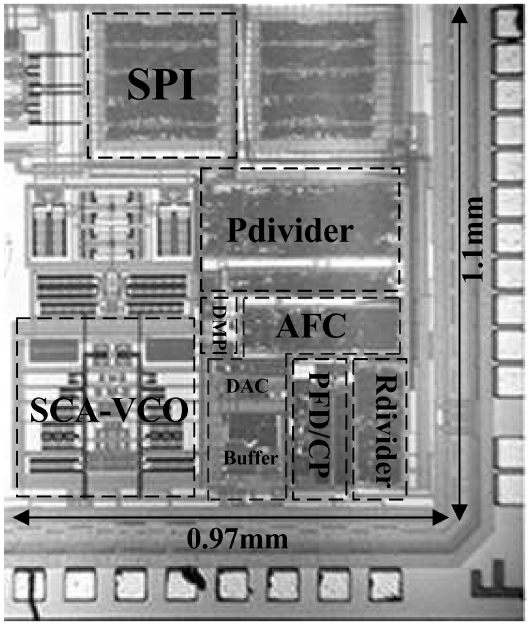

Fig. 9. Die photo of the frequency synthesizer.

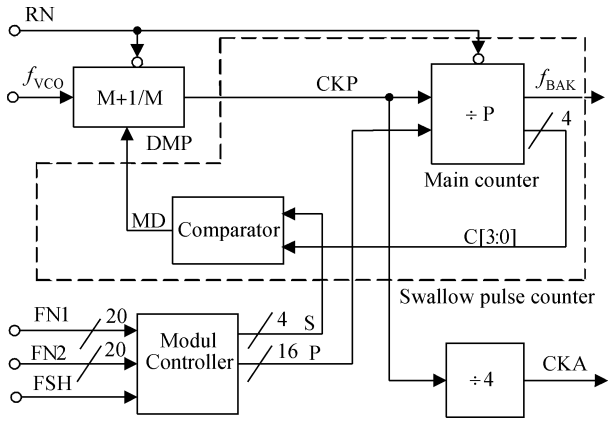

Fig. 8. Schematic of Pdivider.

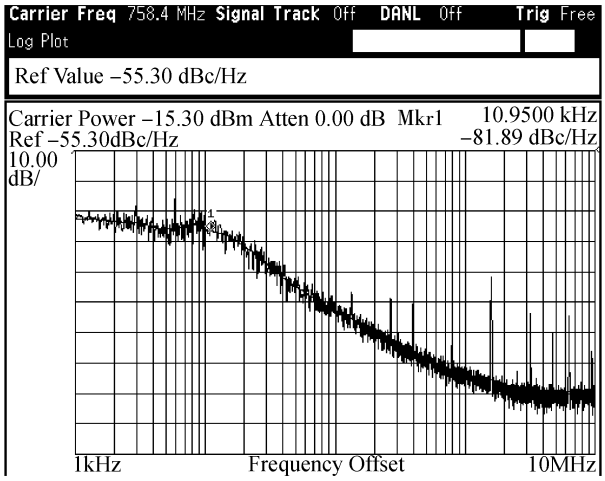

Fig. 10. Measured phase noise of frequency synthesizers at 758.4 MHz.

with 16 sub-bands. As Figure 10 shows, the measured phase noise of 758.4 MHz carrier frequency is –82 dBc/Hz in-band, –109 dBc/Hz @ 100 kHz and –130 dBc/Hz @1 MHz. When the synthesizer is steady, it consumes 12 mA from a single 1.8 V supply voltage.

Figure 11 shows the measured frequency acquisition responses of the frequency synthesizer working in frequency calibration mode and store/load mode. The response of the frequency calibration mode is shown as the curve *a*, whose frequency calibration time t_{AFC} is about 16 μs and total lock time t_s is no more than 20 μs. Because there is no frequency calibration, t_{AFC} of the store/load mode response shown as the curve *b* is only 1 μs and t_s is about 5 μs.

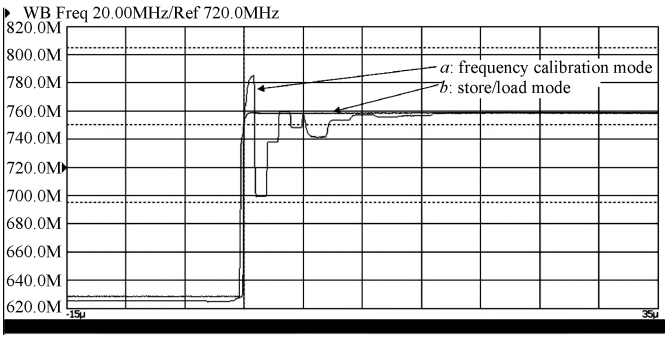

Fig. 11. Measured frequency acquisition response. (a) Frequency calibration mode. (b) Store/load mode.

4. Conclusion

A fast lock frequency synthesizer using an improved AFC has been developed using a 0.18 μm CMOS process. The synthesizer can work in the frequency calibration mode or the store/load mode. In the frequency calibration mode, a novel frequency detector has been adopted to speed up the frequency calibration. In the store/load mode, the AFC can store the cal-

ibration results and load them to rapidly resume the frequency point. The experimental results show that the lock time is about 20 μs in frequency calibration mode and 5 μs in store/load mode.

Acknowledgment

The authors are grateful to Luo Jian, Li Li, Dong Toby of Agilent, Beijing, China, for measurements.

References

[1] Hegazi E, Abidi A A. Varactor characteristic, oscillator tuning curves, and AM-FM conversion. IEEE J Solid-State Circuits, 2003, 38(6): 1033

[2] Lee H I, Cho J K, Lee K S, et al. A Σ–Δ fractional-N frequency synthesizer using a wide-band integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA applications. IEEE J Solid-State Circuits, 2004, 39(7): 1164

[3] Messerschmitt D. Frequency detectors for PLL acquisition in timing and carrier recovery. IEEE Trans Commun, 1979, 27(9): 1288

[4] Rao A, Mansour M, Singh G, et al. A. 4–6.4 GHz LC PLL with adaptive bandwidth control for a forwarded clock link. IEEE J Solid-State Circuits, 2008, 43(9): 2099

[5] Yin Yadong, Chen Jie, Wang Haiyong. A band III PLL frequency synthesizer. Journal of Semiconductors, 2008, 29(6): 1216

[6] Yin Yadong, Chen Jie, Ding Guangcai, et al. A fast setting band-switching circuit in wideband PLL. Research & Progress of Solid State Electronics, 2009, 29(1): 58

[7] Fisher J A, Koch R. A highly linear CMOS buffer amplifier. IEEE J Solid-State Circuits, 1987, sc-22(3): 330