An A/D interface based on ΣΔ modulator for thermal vacuum sensor ASICs*

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Abstract: A new ΣΔ modulator architecture for thermal vacuum sensor ASICs is proposed. The micro-hotplate thermal vacuum sensor fabricated by surface-micromachining technology can detect the gas pressure from 1 to 10^5 Pa. The amplified differential output voltage signal of the sensor feeds to the ΣΔ modulator to be converted into digital domain. The presented ΣΔ modulator makes use of a feed-forward path to suppress the harmonic distortions and attain high linearity. Compared with other feed-forward architectures presented before, the circuit complexity, chip area and power dissipation of the proposed architecture are significantly decreased. The correlated double sampling technique is introduced in the 1st integrator to reduce the flicker noise. The measurement results demonstrate that the modulator achieves an SNDR of 79.7 dB and a DR of 80 dB over a bandwidth of 7.8 kHz at a sampling rate of 4 MHz. The circuit has been fabricated in a 0.5 μm 2P3M standard CMOS technology. It occupies an area of 5 mm^2 and dissipates 9 mW from a single 3 V power supply. The performance of the modulator meets the requirements of the considered application.

Key words: integrated sensor; analog to digital conversion; feed-forward path; correlated double sampling; ΣΔ modulator
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1. Introduction

With the rapid development of micro-electro-mechanical systems and large scale integrated circuits, the sensors have been integrated with the analog to digital converters (ADCs), digital signal processing circuits and memories into a chip. The integrated sensors have presently become the main developing tendency of sensors due to the benefits of small size, low power dissipation, fast response speed and long distance transmission. The thermal vacuum sensors have been widely used in the fields of metal smelting, food processing, thin film preparation and electronic packaging because of their simple structures, wide measure ranges and long lives. Many monolithic integrated CMOS thermal vacuum sensor systems have been successfully realized abroad. Among these researches, Mastrangelo[1] proposed a thermal absolute pressure system integrating a gas pressure sensor, a constant-resistance bias circuit and an ADC; Haberli[2] presented a pressure sensor system consisting of a biasing circuit, a bandgap reference and two ADCs in order to keep the sensor operate at a constant relative temperature; Klaassen[3] integrated a thermal vacuum sensor with an operational amplifier (OPAMP) and a DAC to maintain a constant temperature difference between the sensor and the substrate.

Among all the types of ADCs, the SAR ADC and ΣΔ ADC are usually used in the integrated sensor system[1,4−7]. The SAR ADC is an attractive choice because of the advantages of small area and low power[4]. However, the SAR ADC needs to use some forms of error correction techniques when the required resolution is 12 bit or more. The circuit complexity is increased. On the other hand, the ΣΔ ADC is most suitable for low frequency, high resolution applications[5]. It is easy for the ΣΔ ADC to achieve an accuracy over 12-bit. Furthermore, the ΣΔ ADC is an adequate choice for the conditions where the operating environment is poor. Therefore, the ΣΔ ADC is a good candidate for the sensor applications, where the bandwidth is small and the circuit operating environment is bad.

The ΣΔ modulator is the critical component of the ΣΔ ADC. A second-order single-bit modulator architecture is chosen for the sensor system since the loop is unconditionally stable[6,7], and the required digital post-processing is simple. The correlated double sampling technique is adopted in the 1st integrator to decrease the flicker noise. The feed-forward path is adopted to lower the internal signal swing[8,9] and suppress the harmonic distortions effectively. Compared with the feed-forward structures presented before[8,9], the adder, which is the absolutely necessary element in their structures, is excluded from the proposed modulator. The power dissipation, circuit complexity and chip area are decreased, while the output swings of the integrators are almost uniform with those structures. The modulators with feed-forward paths reported by the domestic research institutes[10,11] are only simulated, and the structures are not validated by the fabricated chip. This paper researches carefully the effects of the feed-forward path. The circuits are discussed in detail for low supply voltage and realized in a 0.5 μm standard CMOS process to verify the performance of the proposed structure.

2. Thermal vacuum sensor system

The micro-hotplate (MHP) thermal vacuum sensor is fabricated by surface-micromachining technology. The diagram of the sensor is shown in Fig. 1. The micro-hotplate with an

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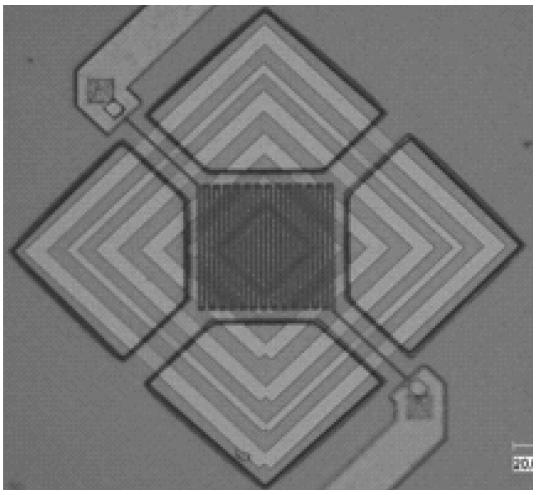

Fig. 1. Micro-hotplate thermal vacuum sensor.

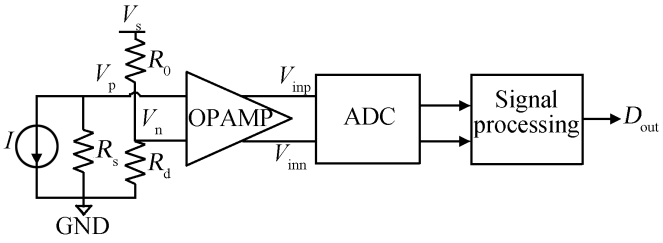

Fig. 2. Diagram of the integrated thermal vacuum sensor system.

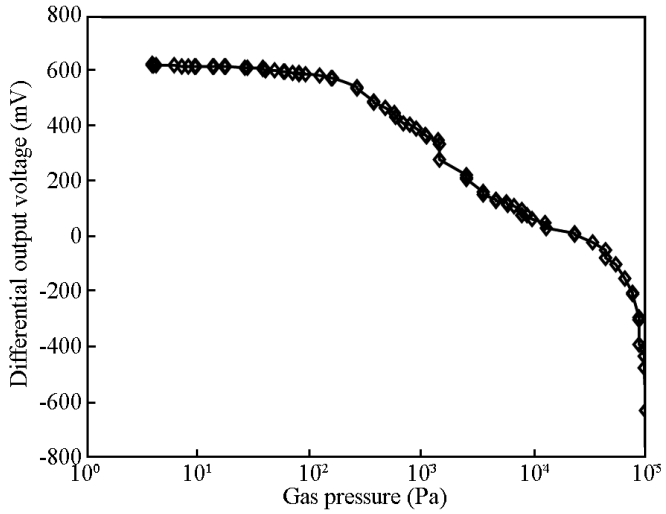

Fig. 3. Voltage difference between V_{inp} and V_{inn} versus gas pressure.

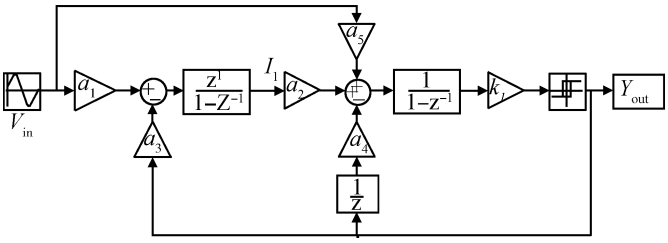

Fig. 4. Block diagram of the proposed ΣΔ modulator.

area of 40 × 40 μm^2 is supported by four cantilever beams of 30 × 15 μm^2. The heat resistor on the micro-hotplate is made from tungsten. The temperature compensating resistor is made on the substrate. After the sacrificial layer is eroded, the micro-hotplate suspends over the substrate, and the vacuum cavity is formed[12]. The temperature of the micro-hotplate is determined by the electrical power and the heat loss induced by the conduction of the surrounding gas. The thermal conductivity increases with gas pressure. Under the condition that the electrical power remains constant, the temperature of the micro-hotplate is decreased with the increase of the gas pressure. The heat resistance on the micro-hotplate decreases correspondingly. Thus, the air gas pressure in vacuum can be detected by measuring the heat resistance. The fabrication flow of the thermal vacuum sensor is compatible with the standard CMOS process except the erosion of the sacrificial layer. The sensor works in constant-current mode. The diagram of the sensor system is shown in Fig. 2. Here, R_s is the heat resistor, R_d is the temperature compensating resistor, and R_0 is the adjustable resistor off the chip. At the beginning of the test, R_0 is regulated to make the electric bridge balance under the low gas pressure. The output voltage V_p is equal to V_n. Then, the gas pressure is increased, and the resistance R_s decreases correspondingly. The electric bridge loses balance, and the voltage difference between V_p and V_n is amplified by the OPAMP. The differential signal between V_{inp} and V_{inn} is shown in Fig. 3. It is clear that the sensor can detect the gas pressure from 1 to 10^5 Pa. The output voltage changes slowly during the gas pressure from 1 to 200 Pa. Therefore, the resolution of the ADC should be above 12-bit.

3. Architecture design of the ΣΔ modulator

The theoretical dynamic range of ΣΔ modulators is the maximum signal to quantization noise ratio (i.e. peak SNR), as shown in Eq. (1):

$$\mathrm{SNR}_{\mathrm{peak}} = \frac{3}{2}\frac{2L+1}{\pi^{2L}}M^{2L+1}(2^B-1)^2. \qquad (1)$$

The performance of ΣΔ modulators can be optimized by a tradeoff between the order L, the over-sampling ratio M and the resolution of the quantizer B. A second-order single-bit ΣΔ modulator is suited for the thermal vacuum sensor. The area and power consumption of the second-order architecture are intrinsically low. Furthermore, the single-bit quantizer owns inherent linearity, and the quantization output can be easily transmitted. In the small signal bandwidth applications, it is easy for M to achieve 256. To depress the harmonic distortions, a feed-forward path is introduced. The block diagram of the proposed ΣΔ modulator is shown in Fig. 4. Compared with the conventional structure, the feed-forward path a_5 is added in the proposed modulator. The adder is not included in the modulator, which is an indispensable element in the feed-forward structures presented before[8, 9]. The power dissipation and chip area of the proposed modulator are effectively decreased, while the output swings of the integrators are almost uniform with those structures. By applying linear analysis to the architecture in Fig. 4, the output of the modulator

can be expressed as:

$$Y(z) = \frac{D_2(z)}{D_1(z)} V_{\text{in}}(z) + \frac{(1-z^{-1})^2}{D_1(z)} Q(z), \tag{2}$$

where,

$$\begin{cases} D_1(z) = 1 + \left(\dfrac{a_2 a_3 + a_4}{a_5} - 2\right) z^{-1} + \left(1 - \dfrac{a_4}{a_5}\right) z^{-2}, \\ D_2(z) = 1 + \left(\dfrac{a_1 a_2}{a_5} - 1\right) z^{-1}. \end{cases} \tag{3}$$

$Q(z)$ is the quantization error. To obtain a pure second-order modulator, such conditions should be satisfied:

$$a_1 = a_3, \quad a_4 = a_5 = a_2 a_3 \tag{4}$$

So, the output of the modulator can be simplified as:

$$Y(z) = V_{\text{in}}(z) + \left(1 - z^{-1}\right)^2 Q(z). \tag{5}$$

By the Matlab/Simulink behavioral simulations, the optimum parameters are $a_1 = a_3 = 0.25$, $a_2 = 0.5$, $a_4 = a_5 = 0.125$. The large output swings of the integrators can not only cause the nonlinearity of the OPAMPs but also limit the power supply voltage of the analog circuit. Consequently, the integrator output swings should be reduced. By adding the feed-forward path, the signal can be largely cancelled at the output of integrators. The dynamic range is increased, and the effects of circuit non-idealities are weakened[9].

The OPAMP nonlinear open-loop gain, A_v, depends on the output voltage of the OPAMP and can be approximated by the expression, $A_v = A_0(1 + \lambda_1 v + \lambda_2 v^2)$, where A_0 is the DC gain, and λ_1 and λ_2 are the 1st and 2nd order deviation coefficients respectively. Thus, the output of the switched capacitor (SC) integrator is:

$$\begin{aligned} V_0(n) = V_0(n-1) + g_1 \Bigg[& V_{\text{i}}(n-1) - \frac{V_{\text{i}}(n-1) + V_0(n)}{A_0} \\ & + \lambda_1 V_0(n) \frac{V_{\text{i}}(n-1) + V_0(n)}{A_0} \\ & + \lambda_2 V_0^2(n) \frac{V_{\text{i}}(n-1) + V_0(n)}{A_0} \Bigg], \end{aligned} \tag{6}$$

where V_{i} and V_0 are the input and output of the integrator respectively. Suppose the input and output of the integrator are estimated by their 1st harmonic, the amplitudes of 2nd and 3rd harmonics referred to the integrator input can be obtained by performing a Fourier series expansion of the terms in the parenthesis of Eq. (6)[8]:

$$A_{\text{H2}} = \frac{|\lambda_1|}{2A_0} V_0 \sqrt{V_{\text{i}}^2 + V_0^2}, \quad A_{\text{H3}} = \frac{|\lambda_2|}{4A_0} V_0^2 \sqrt{V_{\text{i}}^2 + V_0^2}. \tag{7}$$

From Eq. (7), it is clear that the harmonic distortions improve with the amplitudes of V_{i} and V_0. Owing to the feed-forward path, the output of the 1st integrator in Fig. 4 becomes:

$$I_1(z) = -a_3 \left(1 - z^{-1}\right)^2 Q(z). \tag{8}$$

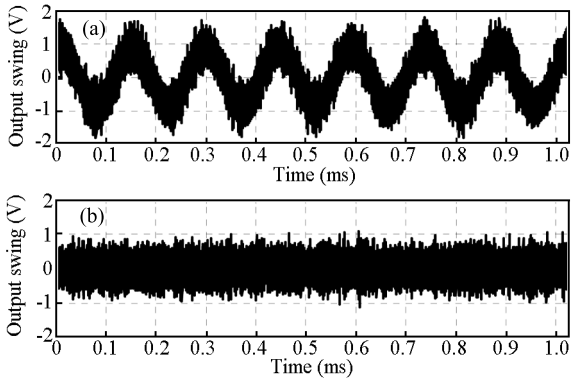

Fig. 5. 1st integrator output swings of the (a) conventional and (b) proposed topology.

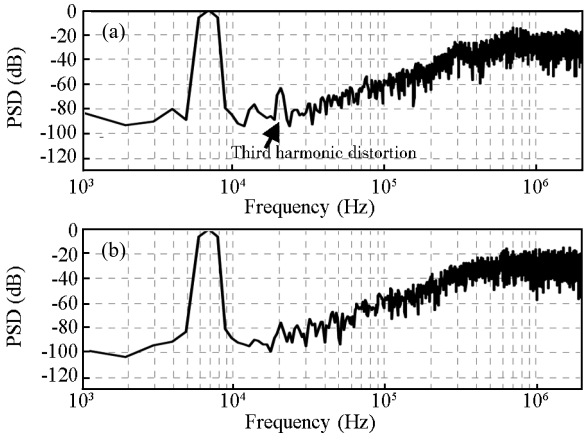

Fig. 6. Power spectral densities of the (a) conventional and (b) proposed topology.

The input signal $V_{\text{in}}(z)$ is cancelled from $I_1(z)$. The amplitudes of V_{i} and V_0 are decreased, thereby the harmonic distortions are reduced. The simulated 1st integrator output waveforms of the conventional and proposed topology are shown in Fig. 5. The correlated double sampling circuit is added to the 1st integrator to decrease the flicker noise of the OPAMP. According to Fig. 5, the output swing of the proposed topology is much smaller than the conventional one. The output swing of the conventional topology ranges from –1.8 to 1.8 V, while the output swing of the proposed topology ranges from –1 to 1 V. Furthermore, the output frequency of the proposed topology is not related to the frequency of the input signal. The power spectral densities of the conventional and proposed topology are shown in Fig. 6. From Fig. 6, the 3rd harmonic distortion is removed effectively from the proposed topology.

4. Circuit implementation

4.1. Design of the correlated double sampling circuit

The main error sources of the $\Sigma\Delta$ modulator include the non-idealities of OPAMP, switch on-resistance and so on. The flicker noise in the modulators for the sensor applications cannot be neglected[5, 13]. The auto-zeroing, correlated double sampling (CDS) and chopper stabilization (CHS) are three effective methods to reduce the flicker noise[14]. The CHS

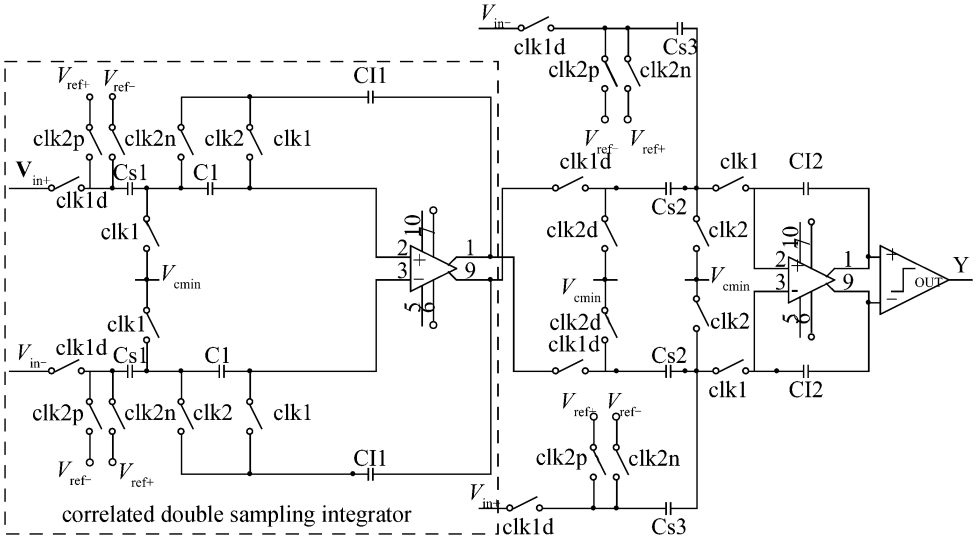

Fig. 7. Schematic of the proposed modulator.

based on modulation technology is a preferable choice for the continuous-time system[14]. The CDS technique reduces the low frequency noise by high-pass filtering, which is inherently a sampled data method and widely used in the switched capacitor circuits. The CDS technique can not only reduce the flicker noise, eliminate DC offset, but also lower the sensitivity of circuit performance to the finite DC gain of the OPAMP[14]. Therefore, the CDS circuit is applied in the 1st integrator.

The modulator is implemented by the fully differential SC circuit with the advantages of double input voltage swing, common-mode noise elimination, high power supply noise rejection and even order harmonic distortion extermination[13]. The input and DAC feedback signal share a common set of capacitors. Due to the capacitor sharing, the *kT/C* noise contributing to the overall noise floor is reduced. The bottom-plate sampling technique is employed to minimize the signal-dependent charge injection and clock feed-through. The circuit schematic of the modulator is shown in Fig. 7.

4.2. Design of the OPAMP and comparator

The OPAMP is the most important building block in the $\Sigma\Delta$ modulator. Its gain, bandwidth, slew-rate, noise, output swing and power dissipation largely determine the whole modulator performance. Usually the requirements for the 1st OPAMP are much stricter than for the following one.

The two-stage fully differential miller OPAMPs are designed for the integrators. The folded-cascode architecture has been employed in the 1st stage for high DC gain, high speed and large capacitive load drive capability. The PMOS transistors have been used as the input differential pair because the flicker noise of PMOS transistors is superior to NMOS transistors under the same conditions. The common-source output stage is followed to provide the desirable output swing. A continuous-time common-mode feedback circuit is adopted to stabilize the output common-mode voltage. The circuit of the OPAMP is shown in Fig. 8. The performance of the two-stage OPAMP with 3 pF load capacitor is listed in Table 1.

The comparator consists of a preamplifier stage, a CMOS latch stage and a SR latch stage. In the preamplifier stage, the diode-connected transistors are used as load, which suppress the over-swings of the output voltages and contribute to high speed operation. The analog preamplifier is separated from the positive feedback dynamic latch to reduce the influence of kickback noise. The SR latch further drives the voltages from the CMOS latch to digital level and keeps the results until the regenerate phase of the next clock period.

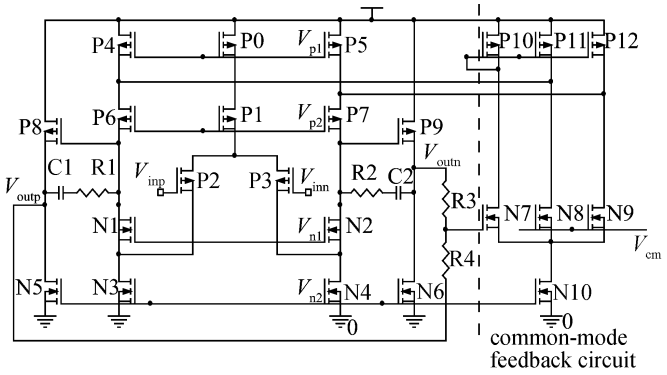

Fig. 8. Two-stage miller OPAMP.

Table 1. Performance of the two-stage OPAMP.

Parameter	1st integrator	2nd integrator
Supply voltage (V)	3	3
Technology	0.5 μm CMOS	0.5 μm CMOS
DC gain (dB)	79.8	80.4
Phase margin (°)	60	60
Unity gain bandwidth (MHz)	77	59
Slew rate (V/μs)	53	38
Output swing (V)	$\pm$2.5	$\pm$2.35
Bias current (μA)	200	110
Power consumption including bias (mW)	4	3.6

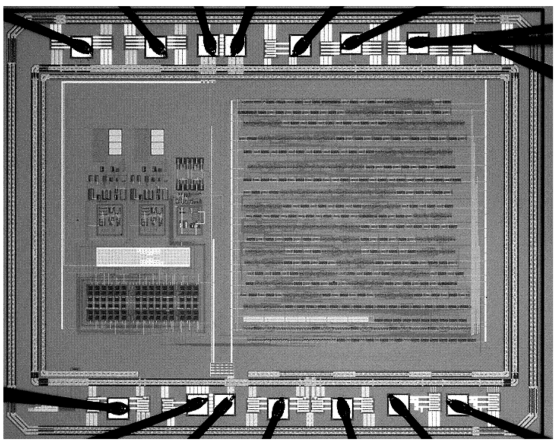

Fig. 9. Chip microphotograph.

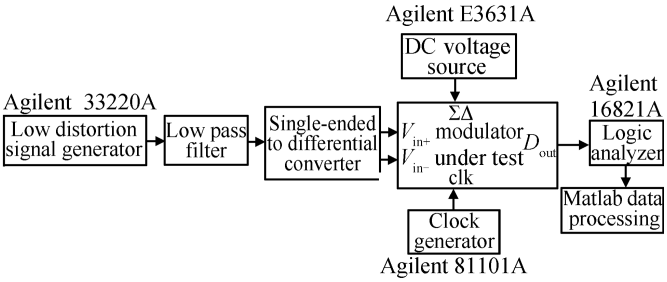

Fig. 10. Block diagram of the test system.

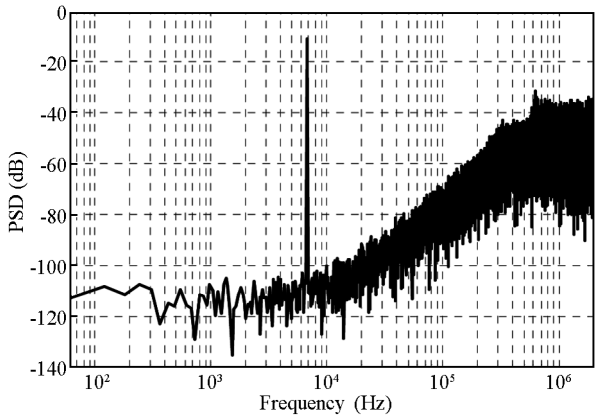

Fig. 11. Measured power spectral density of the proposed modulator.

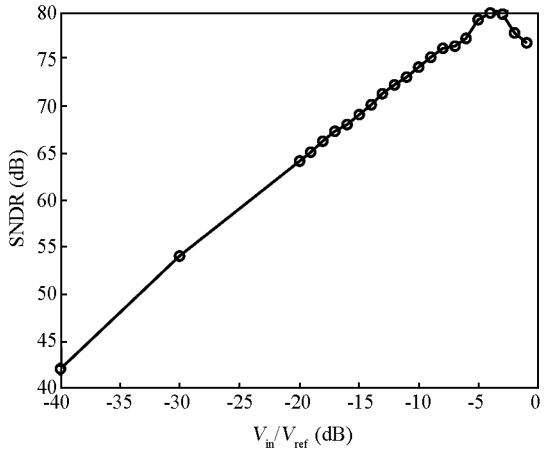

Fig. 12. SNDR versus relative input signal amplitudes.

5. Measurements and results

The proposed second-order ΣΔ modulator has been fabricated in a 0.5 μm 2P3M standard CMOS technology. The chip microphotograph is presented in Fig. 9. The die area including the bonding pads is about 5 mm^2. Great care has been taken not to degrade the modulator performance. The digital and analog circuits are divided into two parts. The digital and analog supply pads are separated in the layout, and the digital and analog ground are isolated in the chip and joined in one place off the chip to avoid the ground loops[15]. The feedback digital signals are separated from the analog circuit and sampling capacitors. The guard rings have been added to ensure the identical border effects, and the metal shields are placed in the sensitive nets to avoid the effects of digital noise coupling. The capacitors are realized with poly$_1$–poly$_2$ structure and fabricated by the unit capacitors arranging in a common centroid array to cancel the 1st order deviation in the oxide thickness.

The chip is packaged in a DIP and fixed on the PCB testboard. A low distortion 14-bit resolution waveform generator is used to generate a single-ended sine wave. The single-ended to differential signal converting circuit is realized in the PCB to provide the input signal for the modulator. The output 1-bit data stream captured by the logic analyzer is transferred to a computer to be analyzed with Matlab routines. The block diagram of the test system is shown in Fig. 10. The measured power spectral density of the proposed ΣΔ modulator is displayed in Fig. 11, which is obtained by fast FFT on 65 536 samples with Hanning window. As shown in Fig. 11, a peak SNDR of 79.7 dB is achieved. The modulator is clocked at 4 MHz and driven by a 6.8 kHz sine-wave input signal with the relative amplitude of −3 dBFS. The spectrum has a flat noise floor. The measured peak SNDR is about 7 dB lower than the result achieved in the simulation. This is due to the additional noise sources such as the noises of the reference voltages and the signal sources as well as the noise coupled through the substrate, which are not taken into account in the simulations. The measured SNDR versus the relative input amplitudes is presented in Fig. 12. An input overload level of around −3 dBFS is indicated by the plot. To measure the dynamic range of the modulator, the relative input signal amplitude should be scanned from about −90 to 0 dBFS. Due to the amplitude limit of the waveform generator, the dynamic range can only be obtained by the fitting method from the data in Fig. 12. By calculation, the SNDR is equal to 0 when V_{in}/V_{ref} is −83 dB, while the SNDR achieves the maximum when V_{in}/V_{ref} is −3 dB. The estimated dynamic range of the modulator is 80 dB. The power dissipation is 9 mW from a single 3 V supply voltage.

The ΣΔ modulator is researched widely in recent years. However the researches are mainly concentrated on the auido ADCs and GSM receivers in the mainland. This paper presents a modulator for the thermal vacuum sensor system. Table 2 shows a performance comparison between the proposed modulator and the recently reported modulators designed for the sensor systems. Due to the different requirements of signal band-

Table 2. Modulator performance comparison.

Reference	Technology	Signal bandwidth (Hz)	Sampling frequency (kHz)	Supply voltage (V)	Power consumption (mW)	SNDR (dB)	Modulator order	FOM*
Ref. [5]	0.6 μm CMOS	400	256	5	50	104.9	4	2.32×10^{-11}
Ref. [6]	0.5 μm CMOS	1	1000	5	12	120	2	1.37×10^{-12}
Ref. [16]	0.8 μm CMOS	500	128	5	11.5	72	2	2.85×10^{-12}
This work	0.5 μm CMOS	7800	4000	3	9	80	2	1.43×10^{-10}

*FOM = $4kT\frac{2^{\mathrm{SNDR}/6.02}\times\mathrm{BW}}{P}$

width and SNDR in the different application environments, the FOM (figure of merit) is used to evaluate the modulator performance. From Table 2, it is clear that this work has a lower power consumption and higher FOM than other designs.

6. Conclusion

A micro-hotplate thermal vacuum sensor system is presented. The manufacture of the sensor is described in detail. The sensor works in constant-current mode, and the amplified differential output signal of the sensor feeds to the $\Sigma\Delta$ modulator. A second-order single-bit switched capacitor $\Sigma\Delta$ modulator for the thermal vacuum sensor is proposed. The feed-forward path is introduced in the modulator to diminish the harmonic distortion and achieve a high resolution. In comparison with other feed-forward structures presented before, the circuit complexity is decreased, and the chip area and power dissipation are saved in the proposed modulator. The correlated double sampling technique is employed to remove the flicker noise. The circuit is fabricated in a 0.5 μm double-poly triple-metal standard CMOS technology. The measured peak SNDR is 79.7 dB at the –3 dBFS relative input signal amplitude, and the estimated dynamic range is 80 dB. The modulator operates under a sampling frequency of 4 MHz and an over-sampling ratio of 256. A resolution of 13-bit is obtained over a bandwidth of 7.8 kHz. The chip has an area of 5 mm^2 and consumes 9 mW static power from a single 3 V supply voltage. The achieved performance satisfies the requirements of the considered application.

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