SBH adjustment characteristic of the dopant segregation process for NiSi/n-Si SJDs

Shang Haiping(尚海平)† and Xu Qiuxia(徐秋霞)

(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

Abstract: By means of analyzing the I–V characteristic curve of NiSi/n-Si Schottky junction diodes (NiSi/n-Si SJDs), abstracting the effective Schottky barrier height ($\phi_{B,\,eff}$) and the ideal factor of NiSi/n-Si SJDs and measuring the sheet resistance of NiSi films (R_{NiSi}), we study the effects of different dopant segregation process parameters, including impurity implantation dose, segregation annealing temperature and segregation annealing time, on the $\phi_{B,\,eff}$ of NiSi/n-Si SJDs and the resistance characteristic of NiSi films. In addition, the changing rules of $\phi_{B,\,eff}$ and R_{NiSi} are discussed.

Key words: NiSi/n-Si SJD; effective Schottky barrier height; dopant segregation process
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1. Introduction

As the feature dimensions of MOSFETs are scaling into the nanometer regime, metal S/D MOSFETs (SB MOSFETs) have been considered as the most promising candidate for conventional MOSFETs with impurity highly doped S/D. However, due to the high $\phi_{B,eff}$ at the source/channel interface, SB MOSFETs still do not achieve the same current characteristics as conventional MOSFETs[1]. So, intensive research on $\phi_{B,eff}$ tuning techniques has been done, in order to enhance SB MOSFET performance.

Among the many $\phi_{B,eff}$ tuning techniques, the post-silicide dopant segregation process[2] is not only compatible with the conventional CMOS technology, but also acquires good adjustment results. In this paper, we will investigate the effects of different dopant segregation process parameters, including impurity implantation dose, segregation annealing temperature and segregation annealing time, on the $\phi_{B,eff}$ of NiSi/n-Si SJDs and the resistance characteristic of NiSi films. Furthermore, by comprehensive consideration of $\phi_{B,eff}$ and R_{NiSi}, an optimization technique for the dopant segregation process is proposed.

2. Experiment

Blanket n-type (2–4 Ω·cm) Si(100) substrates were used in this work. Following oxidation, photolithography and the wet etching process, many circle windows with diameters of 250 μm were formed. Then, TiN/Ni double-layer metal films were prepared on these wafers by alternate sputtering deposition of Ni film and TiN film. The Ni-silicide formation process was carried out *ex situ* by two-step rapid thermal processing (RTP) in high pure nitrogen ambient. The two-step Ni silicide formation process consists of the procedure of low temperature RTP, selective etching and higher temperature RTP[16]. Then the wafers were treated with different process conditions. Finally, Al was metalized on both sides of wafer to form a metal electrode. Figure 1 shows the experimental procedure diagram of this experiment. A four-point probe (FPP) was used to measure the sheet resistance of the formed Ni-silicide films. A Keithley-4200-SCS was used to measure the I–V characteristic of NiSi/n-Si at room temperature (300 K) under the conditions of avoiding light.

3. Abstraction method of $\phi_{B,eff}$

According to one dimension thermionic emission theory[3], the current transport equation for the practical SJD is given by Eq. (1).

$$I = AA^*T^2 \exp\Big(-\frac{\phi_{B,eff}}{V_T}\Big)\Big[\exp\frac{V-IR}{nV_T}-1\Big], \quad (1)$$

where A is the area of SJD, A^* is the effective Richardson constant for thermionic emission, T is the thermodynamic temperature in Kelvin, $V_T = kT/q$ is the thermal voltage, n is the ideality factor, R is the series resistance, and $\phi_{B,eff}$ is $\phi_{Bn,eff}$ or $\phi_{Bp,eff}$, where $\phi_{Bn,eff}$($\phi_{Bp,eff}$) is the effective Schottky barrier height between metal and n-Si (p-Si) substrate. When $V \geqslant V_T$ and $IR \leqslant V$, Equation (1) is reduced to

$$I = AA^*T^2 \exp\Big(-\frac{\phi_{B,eff}}{V_T}\Big)\exp\Big(\frac{V-IR}{nV_T}\Big). \quad (2)$$

Then, taking $\phi_{Bn,eff}$, n and R as parameter variables and substituting all the constants, which are taken from Ref. [3], into Eq. (2) will give the relationship:

$$\exp\left[16.937-\frac{\phi_{B,eff}}{0.026}+\frac{V-J\times 3.14\times 0.000625R}{0.026n}\right] - J = 0, \quad (3)$$

where

$$J = I/A. \quad (4)$$

Using Eq. (3) as the fitting equation and selecting a proper fitting range, we can deduce n and $\phi_{Bn,eff}$, then $\phi_{Bp,eff}$ can be calculated using

$$\phi_{Bn,eff} + \phi_{Bp,eff} = E_g\,[3], \quad (5)$$

where E_g is the band gap of Si[3].

† Corresponding author. Email: erchou0028@163.com
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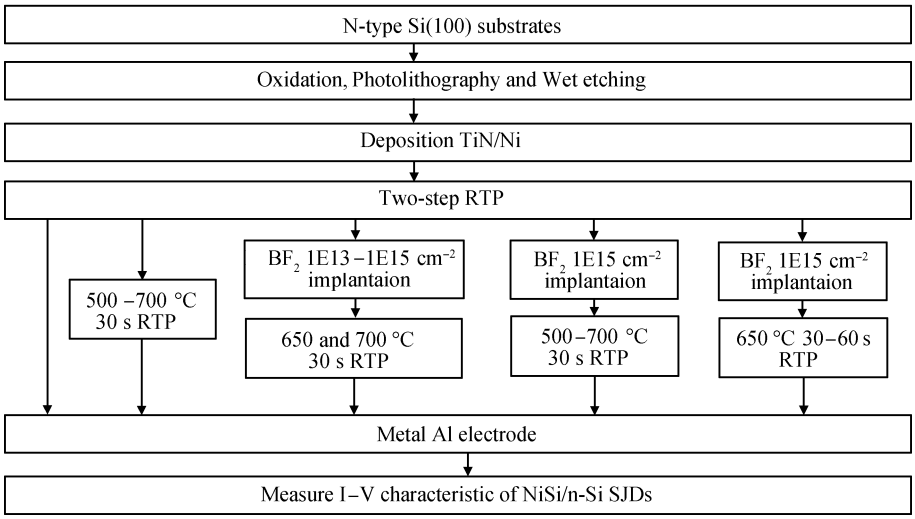

Fig. 1. Experimental procedure diagram.

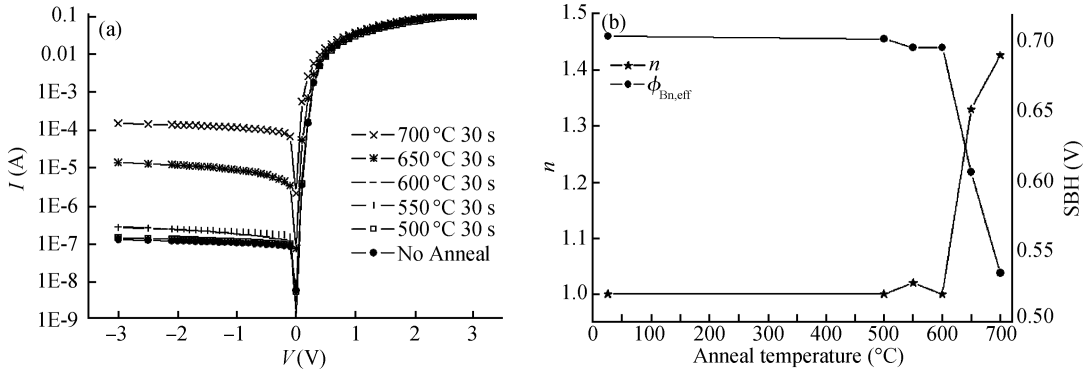

Fig. 2. Without and with various annealing temperatures of RTP for NiSi/n-Si SJDs. (a) I–V characteristic curve. (b) $\phi_{\mathrm{Bn,eff}}$ and n as a function of annealing temperature.

4. Results and analysis

In order to investigate the adjustment mechanism of the dopant segregation process, wafers were dealt with under different process conditions and $\phi_{\mathrm{Bn,eff}}$ and n were abstracted with the above mentioned method.

One group of wafers was treated with various annealing temperatures from 500 to 700 °C for 30 s. When the annealing temperature is lower than 600 °C, compared with the untreated NiSi/n-Si SJD, Figures 2 and 3 show that the reverse current has a little increase, $\phi_{\mathrm{Bn,eff}}$ has a small decrease, R_{NiSi} remains invariant when taking into account measurement error, and n is about 1. According to the measurement result of n and R_{NiSi}, we conclude that the interface characteristic of NiSi/n-Si is good and the NiSi film is stable after 500–600 °C 30 s annealing. $\phi_{\mathrm{Bn,eff}}$ is usually affected by the Fermi level pinning effect, and the interface trap density will decrease after RTP in high purity N_2, resulting in a decrease in $\phi_{\mathrm{Bn,eff}}$ and an increase in the reverse current[4].

However, when the annealing temperature reaches 650 and 700 °C, n and R_{NiSi} show a dramatic increase. These results show that there is a high resistance state Ni-silicide phase formation at the NiSi/n-Si interface[5], which not only results in the increase in R_{NiSi} but also results in NiSi/n-Si interface roughness[6, 7]. The rough NiSi/n-Si interface causes the reverse current to increase and $\phi_{\mathrm{Bn,eff}}$ to decrease, and finally degrades the electrical characteristics of NiSi/n-Si SJDs. These results coincide well with the experimental values as shown in Figs. 2 and 3.

Another group of wafers was treated with various ion implantation doses (1×10^{13}–1×10^{15} cm^{-2}) of BF_2 at the same implantation energy and segregation annealing with 650 °C 30 s and 700 °C 30 s. Figures 4(a) and 4(b) respectively show the I–V characteristic curve and the $\phi_{\mathrm{Bn,eff}}$ and n of NiSi/n-Si SJDs as a function of implantation dose, treated with various implantation doses and 650 °C 30 s segregation annealing. Figure 4 shows that the reverse current is decreased and $\phi_{\mathrm{Bn,eff}}$ is increased with increasing implantation dose, and n still stays at about 1. The main reason for this phenomenon is the impurity segregation effect in the post-silicide process. A mass of B atoms segregates at the NiSi/Si interface, shapes a thin spike with high doping concentration and the concentration increases with increasing implantation dose[8, 12]. This high concentration range of B accumulated at the NiSi/n-Si interface induces the $\phi_{\mathrm{Bn,eff}}$ increase[7, 17]. Furthermore, some of the segregated B atoms replace Si atoms at the Si side of interface, generating an electric dipole layer across the interface. Moreover, the B electric dipole layer is expected to be negatively charged

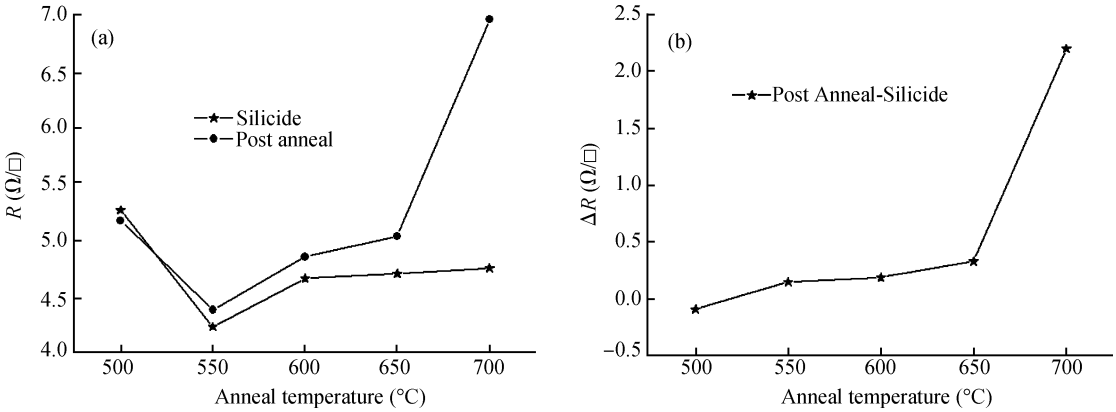

Fig. 3. With various annealing temperatures of RTP for NiSi/n-Si SJDs. (a) R_{NiSi} change curve. (b) NiSi sheet resistance (ΔR_{NiSi}) change curve.

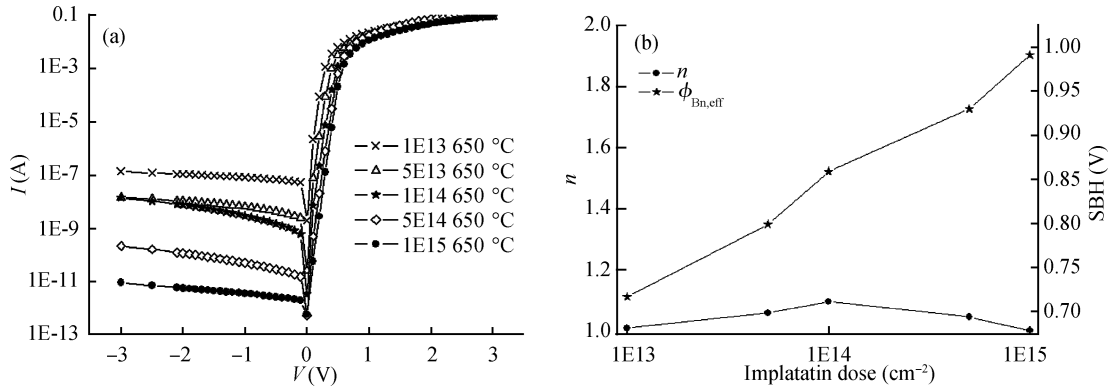

Fig. 4. With various doses of dopant segregation process for NiSi/n-Si SJDs. (a) I–V characteristic curve. (b) $\phi_{\mathrm{Bn,eff}}$ and n as a function of implantation dose.

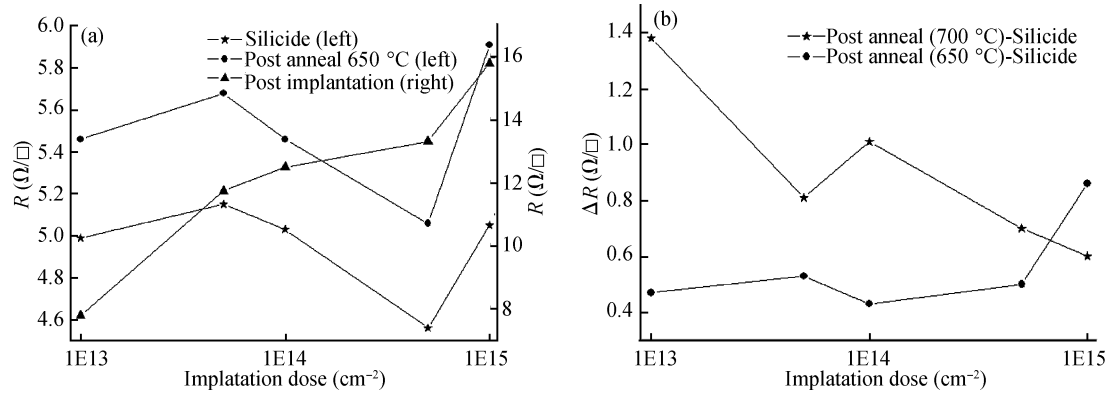

Fig. 5. With various doses of dopant segregation process for NiSi/n-Si SJDs. (a) R_{NiSi} and (b) ΔR_{NiSi} as a function of implantation dose.

and to deform the energy band upward leading to an increased $\phi_{\mathrm{Bn,eff}}$[4, 9−11]. So, the reverse current decreases with increasing $\phi_{\mathrm{Bn,eff}}$. Because the decrement of the reverse current with increasing implantation dose is obvious, changing the implantation dose is more efficient in tuning $\phi_{\mathrm{Bn,eff}}$ when other dopant segregation process parameters remain invariant.

In Fig. 5(a), R_{NiSi} after implantation is increased with increasing implantation dose. Ion implantation damage is an inevitable result of the ion implantation process, which is increased with increasing implantation dose. The ion implantation damage enhances the electron scattering, resulting in increasing resistance. Although segregation annealing can repair part of the implantation damage, because the impurity and the implantation damage are introduced into NiSi films, ΔR_{NiSi} still exists between the pre- and post-segregation processes[13].

In Fig. 5(b), when the segregation annealing is 650 °C 30 s, ΔR_{NiSi} between pre-implantation and the post-segregation process is increased with increasing implantation dose. However, when the segregation annealing is 700 °C 30 s, ΔR_{NiSi} is decreased with increasing implantation dose. In addition, when

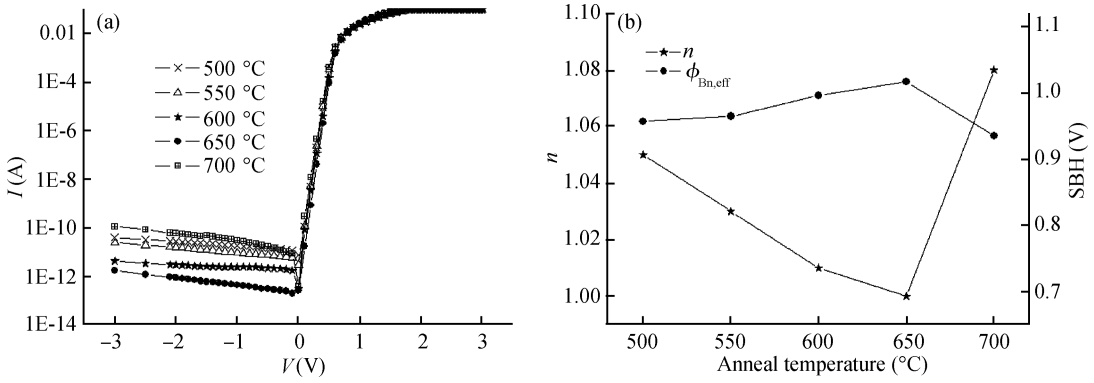

Fig. 6. With various segregation annealing temperatures of dopant segregation process for NiSi/n-Si SJDs with a fixed BF_2 dose of 1×10^{15} cm^{-2}. (a) I–V characteristic curve. (b) $\phi_{Bn,eff}$ and n as a function of annealing temperature.

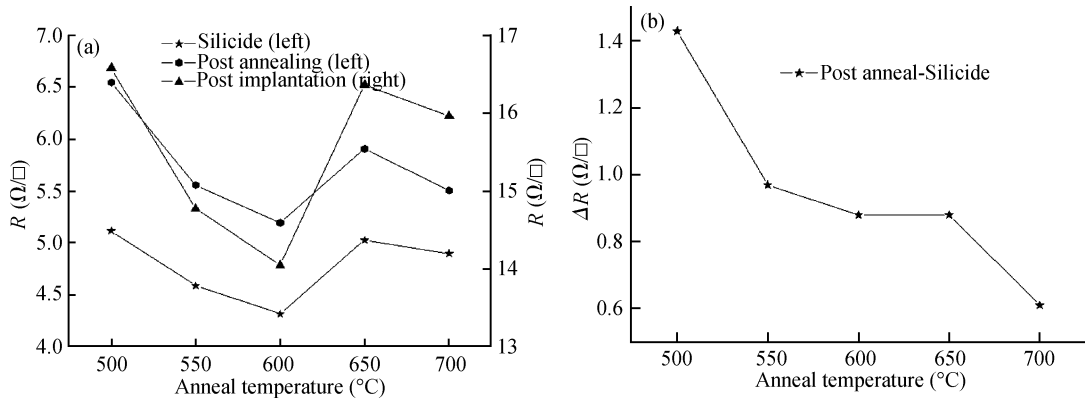

Fig. 7. With various segregation annealing temperatures of dopant segregation process for NiSi/n-Si SJDs. (a) R_{NiSi} and (b) ΔR_{NiSi} as a function of annealing temperature.

the implantation dose is less than 1×10^{15} cm^{-2}, ΔR_{NiSi} after 700 °C 30 s segregation annealing is obviously higher than that after 650 °C 30 s segregation annealing. Comparing Fig. 3(b) with Fig. 5(b) and combining with the value of n in Fig. 4(b), we draw some conclusions as below: One is that B implantation can improve the thermal stability of NiSi films, and this is increased by increasing the implantation dose[13]. So ΔR_{NiSi} after 700 °C 30 s segregation annealing is decreased with increasing implantation dose, and it is obviously lower than that after 700 °C 30 s segregation annealing without B implantation. Another is that, after 650 °C 30 s segregation annealing, the interface characteristic of NiSi/n-Si is good and the NiSi film is stable. So n stays at 1 and ΔR_{NiSi} stays at the same value when the implantation dose is less than 1×10^{15} cm^{-2}. When the implantation dose reaches 1×10^{15} cm^{-2}, even after 650 °C 30 s segregation annealing, there is still much implantation damage in the NiSi film, which results in increasing R_{NiSi}. The other is that there must be a high resistance state Ni-silicide phase formation after 700 °C 30 s segregation annealing[5], and high temperature annealing can enhance the repair of implantation damage. So, when the implantation dose is less than 1×10^{15} cm^{-2}, ΔR_{NiSi} after 700 °C 30 s segregation annealing is obviously higher than that after 650 °C 30 s segregation annealing. When the implantation dose reaches 1×10^{15} cm^{-2}, ΔR_{NiSi} after the segregation process with 700°C 30 s segregation annealing is lower than that after the segregation process with 650 °C 30 s segregation annealing.

Another group of wafers was treated with a dose of 1×10^{15} cm^{-2} BF_2 ion implantation at the same implantation energy and various segregation annealing temperatures (500–700 °C) for 30 s. Figure 6 shows that the reverse current is decreased and $\phi_{Bn,eff}$ is increased with increasing segregation annealing temperature from 500 to 650 °C, and n is about 1. The main reason for this phenomenon is that the concentration of B at the NiSi/n-Si interface increases as the temperature rises[10, 14, 15], which then induces increasing $\phi_{Bn,eff}$ [3, 4, 10, 11, 13] and decreasing reverse current. Because the decrement of the reverse current with increasing segregation annealing temperature is tiny, changing the segregation annealing temperature only can finely adjust $\phi_{Bn,eff}$ when other dopant segregation process parameters remain invariant.

For the wafer after 700 °C 30 s segregation annealing, the previous research told us that there is high resistance state Ni-silicide phase formation at the NiSi/n-Si interface, which results in an abnormal increase of the reverse current and slightly larger n.

In Fig. 7(b), ΔR_{NiSi} decreases with increasing segregation annealing temperature. This phenomenon further illustrates that, even after segregation annealing, there is still much implantation damage in the NiSi film, and high temperature annealing can enhance the repair of implantation damage.

The last group of wafers was treated with a dose of 1×10^{15}

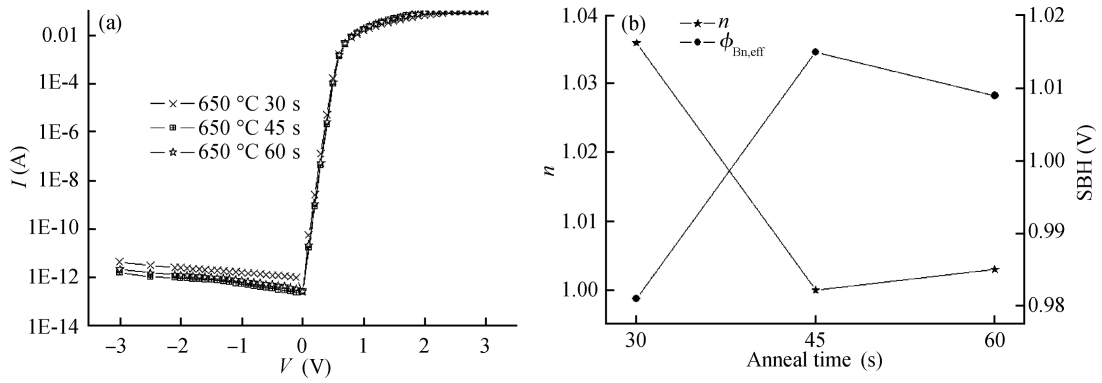

Fig. 8. With various segregation annealing times of dopant segregation process for NiSi/n-Si SJDs. (a) I–V characteristic curve. (b) $\phi_{Bn,eff}$ and n as a function of annealing time.

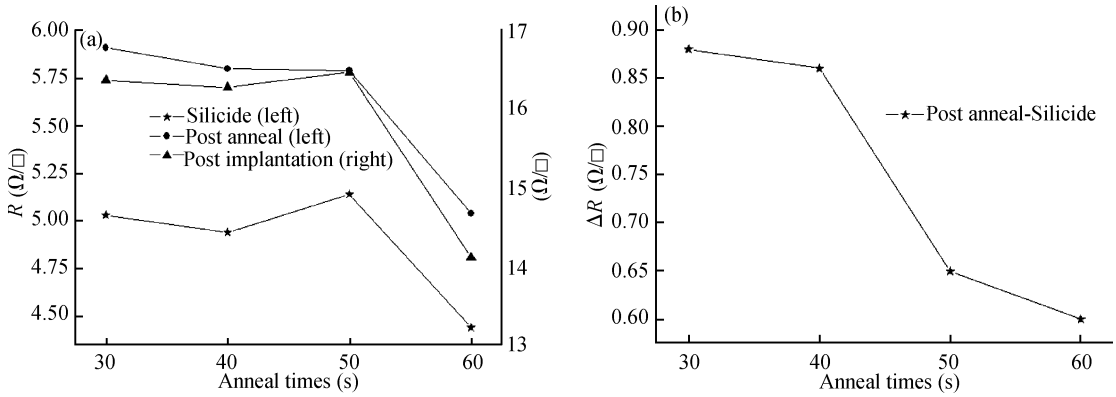

Fig. 9. With various segregation annealing times of dopant segregation process for NiSi/n-Si SJDs. (a) R_{NiSi} and (b) ΔR_{NiSi} as a function of annealing time.

cm^{-2} BF_2 ion implantation at the same implantation energy and the same segregation annealing temperature of 650 °C for various times from 30 to 60 s. Figures 8 and 9 show that the changes of segregation annealing time have a small effect on the electrical characteristics of NiSi/n-Si SJDs, but can obviously decrease R_{NiSi}. Therefore, by optimization of segregation annealing time, the resistance characteristic of NiSi films can be improved.

5. Summary

In this paper, the effects of different dopant segregation process parameters, including impurity implantation dose, segregation annealing temperature and segregation annealing time, on the $\phi_{B,eff}$ of NiSi/n-Si SJDs and the resistance characteristic of NiSi films have been studied. According to the results, we draw some conclusions as below. One is that the implantation dose plays a major role in tuning $\phi_{Bn,eff}$ and the adjustment range increases with increasing implantation dose when the segregation annealing temperature is above 500 °C, but a high implantation dose will cause high R_{NiSi}. Another is that the segregation annealing temperature only can finely adjust $\phi_{Bn,eff}$ when other dopant segregation process parameters remain invariant. The last is that the segregation annealing time has little effect on the electrical characteristics of NiSi/n-Si SJDs, but can obviously optimize the resistance characteristic of NiSi films. So, the optimum process conditions of the dopant segregation process for NiSi/n-Si SJDs are 1×10^{15} cm^{-2} of BF_2 ion implantation and 650 °C, 60 s of segregation annealing.

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